PRELIMINARY

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TFT MONOCHROME LCD MODULE

NL128102BM29-05

48.0 cm (19.0 Type)
SXGA
LVDS interface (2port)

PRELIMINARY DATA SHEET

DOD-PD-0501 (1st edition)

All information is subject to change without notice. Please confirm the sales representative before starting to design your system.

INTRODUCTION

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NEC products are classified into the following three quality grades:
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Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Military systems, aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems (medical equipment, etc.) and any other equipment

The quality grade of this product is ***"Standard"*** unless otherwise specified in this document. If customers intend to use this product for applications other than those specified for ***"Standard"*** quality grade, they should contact NEC sales representative in advance.

CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Monochrome LCD module NL128102BM29-05 is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a monochrome-filter glass substrate.

Grayscale data signals from a host system (e.g. PC, signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Monochrome images are created by regulating the amount of transmitted light through the TFT array.

1.2 APPLICATION

- Monochrome monitor system

1.3 FEATURES

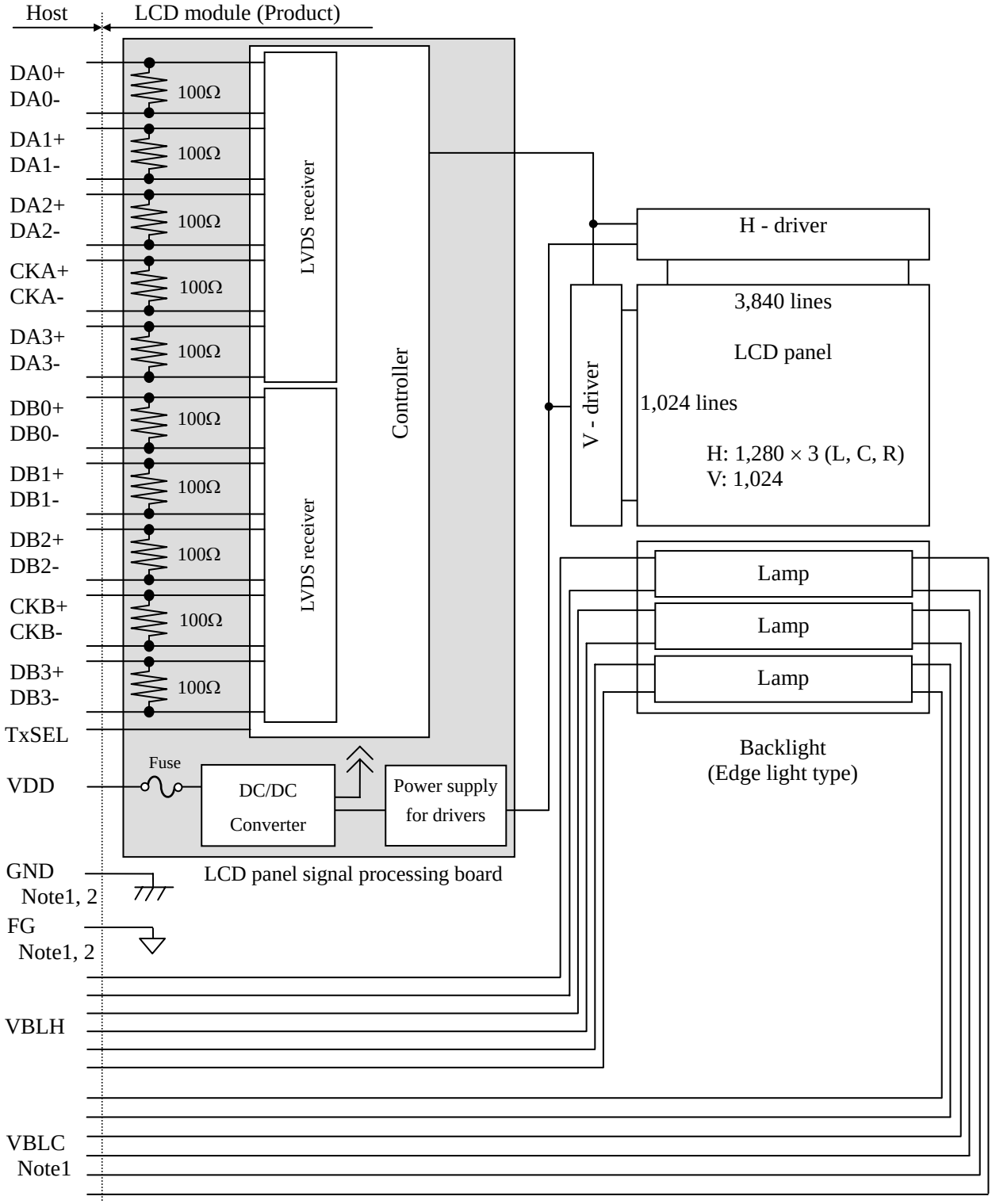
- Ultra-wide viewing angle (Adoption of Super Advanced -Super Fine TFT (SA-SFT))
- High luminance
- High contrast
- High resolution
- 256 gray scales per 1 sub-pixel
- LVDS interface
- Selectable LVDS input map
- Edge light type (without inverter)

2. GENERAL SPECIFICATIONS

Display area	376.32 (H) × 301.056 (V) mm
Diagonal size of display	48.0 cm (19.0 inches)
Drive system	a-Si TFT active matrix
Display grayscale	256 gray scales per 1 sub-pixel (8-bit) (766 gray scales per 1 pixel)
Pixel	1,280 (H) × 1,024 (V) pixels (1 pixel consists of 3 sub-pixels (LCR).)
Pixel arrangement	LCR vertical stripe
Dot pitch	0.098 (H) × 0.294 (V) mm
Pixel pitch	0.294 (H) × 0.294 (V) mm
Module size	404.2 (W) × 330.0 (H) × 22.0 (D) mm (typ.)
Weight	2,900 g (typ.)
Contrast ratio	(700):1 (typ.)
Viewing angle	*At the contrast ratio ≥10:1* • Horizontal: Right side 85° (typ.), Left side 85° (typ.) • Vertical: Up side 85° (typ.), Down side 85° (typ.)
Designed viewing direction	Viewing angle with optimum grayscale (γ=DICOM): normal axis Note1
Polarizer surface	Antiglare
Polarizer pencil-hardness	2H (min.) [by JIS K5400]
Response time	*Ton+Toff (10%←→90%)* (35) ms (typ.)
Luminance	*At IBL=6.0mArms / lamp* (800)cd/m^2 (typ.)
Signal system	LVDS 2 port LCR 8-bit digital signals, Dot clock (CLK), Data enable (DE)
Power supply voltage	LCD panel signal processing board: 5.0V
Backlight	Edge light type: 6 cold cathode fluorescent lamps (without inverter)
Power consumption	*At IBL=6.0mArms / lamp and checkered flag pattern* 26.8 W (typ., Power dissipation of the inverter does not include.)

Note1: When the product luminance is 800cd/m^2, the gamma characteristic is designed to γ=DICOM.

3. BLOCK DIAGRAM



Note1: Connections between GND (Signal ground), FG (Frame ground) and VBLC (Lamp low voltage terminal) in the product

GND - FG	Not connected
GND - VBLC	Not connected
FG - VBLC	Not connected

Note2: GND and FG must be connected to customer equipment's ground, and it is recommended that GND, FG and customer inverter ground are connected together in customer equipment.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	404.2 ± 0.5 (W) × 330.0 ± 0.5 (H) × 22.0 ± 0.3 (D) Note1 Note2	mm
Display area	376.32 (H) × 301.056 (V) Note2	mm
Weight	2,900 (typ.), 3,100 (max.)	g

Note1: Excluding lamp cable and cable clamp.
Note2: See "**7. OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board	VDD	-0.3 to +6.0	V	Ta = 25°C
	Lamp voltage	VBLH	2,000	Vrms	
Input voltage for signals	Display signals Note1	VD	-0.3 to +2.8	V	Ta = 25°C VDD= 5.0V
	Function signal Note2	VF		V	
Storage temperature		Tst	-20 to +60	°C	-
Operating temperature	Front surface	TopF	0 to +55	°C	Note3
	Rear surface	TopR	0 to +60	°C	Note4
Relative humidity Note5		RH	≤ 95	%	Ta ≤ 40°C
			≤ 85	%	40 < Ta ≤ 50°C
			≤ 70	%	50 < Ta ≤ 55°C
Absolute humidity Note5		AH	≤ 73 Note6	g/m^3	Ta > 55°C
Operating altitude		-	≤ 4,850	m	0°C≤ Ta ≤ 55°C
Storage altitude		-	≤ 13,600	m	-20°C≤ Ta ≤ 60°C

Note1: Display signals are DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-
Note2: Function signal is TxSEL.
Note3: Measured at center of LCD panel surface (including self-heat)
Note4: Measured at center of LCD module's rear shield surface (including self-heat)
Note5: No condensation
Note6: Ta = 55°C, RH = 70%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta = 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDD	4.5	5.0	5.5	V	-
Power supply current		IDD	-	(680) Note1	(1,400) Note2	mA	at VDD = 5.0V
Permissible ripple voltage		VRP	-	-	100	mVp-p	for VDD
Differential input threshold voltage for LVDS receiver	High	VTH	-	-	+100	mV	at VCM=1.2V Note3
	Low	VTL	-100	-	-	mV	
Terminating resistance		RT	-	100	-	Ω	-
Input voltage for TxSEL signal	High	VFH	High must be Open.			-	TxSEL Note4
	Low	VFL	-	-	0.5	V	
Input current for TxSEL signal		IFL	-80	-	+10	μA	

Note1: Checkered flag pattern [by EIAJ ED-2522]
Note2: Pattern for maximum current
Note3: Common mode voltage for LVDS receiver
Note4: TxSEL is pulled-up in the product. (Pull-up resistance: 50kΩ)

4.3.2 Backlight lamp

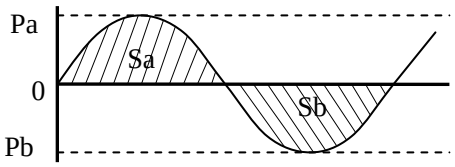
(Ta=25°C, Note1)

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Lamp current	IBL	3.5	6.0	7.0	mArms	at IBL=6.0mArms: (800)cd/m^2 Note3
Lamp voltage	VBLH	-	650	-	Vrms	Note2, Note3
Lamp starting voltage	VS	1,350	-	-	Vrms	Ta = 25°C Note2, Note3
		1,550	-	-	Vrms	Ta = 0°C Note2, Note3
Lamp oscillation frequency	FO	40	48	55	kHz	Note4

Note1: This product consists of 6 backlight lamps, and these specifications are for each lamp.

Note2: The lamp voltage cycle between lamps should be kept on a same phase. "VS" and "VBLH" are the voltage value between low voltage side (Cold) and high voltage side (Hot).

Note3: The asymmetric ratio of working waveform for lamps (Power supply voltage peak ratio, power supply current peak ratio and waveform space ratio) should be less than 5 % (See the following figure.). If the waveform is asymmetric, DC (Direct current) element apply into the lamp. In this case, a lamp lifetime may be shortened, because a distribution of a lamp enclosure substance inclines toward one side between low voltage terminal (Cold terminal) and high voltage terminal (Hot terminal).



$$\frac{|Pa - Pb|}{Pb} \times 100 \leq 5\ \%$$

$$\frac{|Sa - Sb|}{Sb} \times 100 \leq 5\ \%$$

Pa: Supply voltage/current peak for positive, Pb: Supply voltage/current peak for negative
Sa: Waveform space for positive part, Sb: Waveform space for negative part

Note4: In case "FO" is not the recommended value, beat noise may display on the screen, because of interference between "FO" and "1/th". Recommended value of "FO" is as following.

$$FO = \frac{1}{4} \times \frac{1}{th} \times (2n-1)$$

th: Horizontal cycle (See "**4.9.1 Timing characteristics**".)
n: Natural number (1, 2, 3 ·····)

Note5: Method of lamp cable installation may invite fluctuation of lamp current and voltage or asymmetric of lamp working waveform. When designing method of lamp cable installation, evaluate the fluctuation of lamp current, voltage and working waveform sufficiently.

4.3.3 Power supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VDD	5.0V	≤ 100	mVp-p

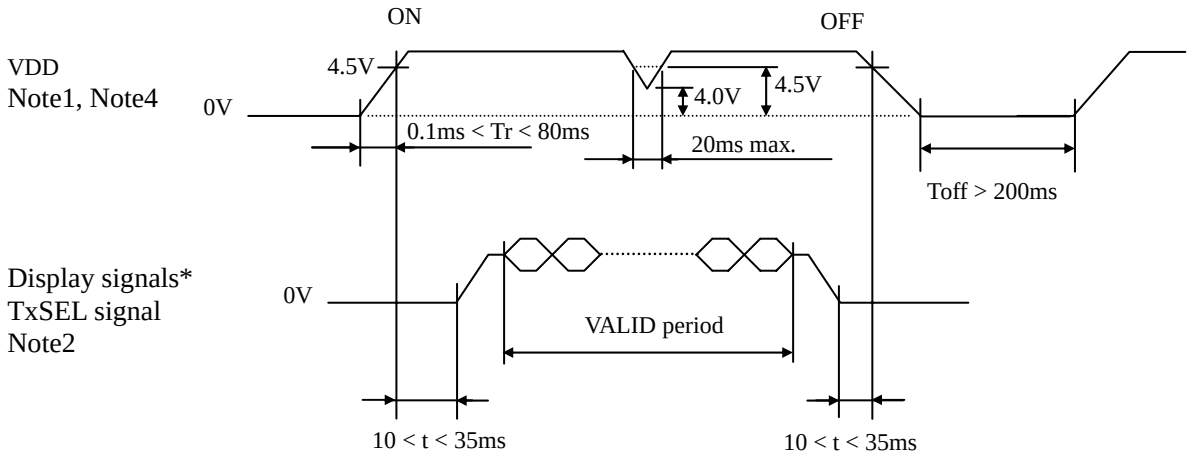
Note1: The permissible ripple voltage includes spike noise.

4.3.4 Fuse

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	KAB2402 402	Matsuo Electric Co., Ltd.	4.0 A 24 V	8 A, 1min. max.	Note1

Note1: The power supply capacity should be more than the fusing current. If the power supply capacity is less than the fusing current, the fuse may not blow for a short time, and then nasty smell, smoking and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE



* These signals should be measured at the terminal of 100Ω resistance.

Note1: In terms of voltage variation (voltage drop) while VDD rising edge is below 4.5V, a protection circuit may work, and then this product may not work.

Note2: Display signals (DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-) and TxSEL signal must be "0" voltage, exclude the VALID period (See above sequence diagram). If these signals are higher than 0.3V, the internal circuit is damaged. If some of display and function signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. If customer stops the display and function signals, they should be cut VDD.

Note3: VDD should be 4.5V or more while VDD ON period.

Note4: The backlight power supply voltage should be inputted within the valid period of display and function signals, in order to avoid unstable data display.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

CN1 socket (LCD module side): FI-X30SL-HF (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: FI-X30C/ FI-30H/ FI-X30M (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	DA0-	Odd pixel data 0	Note1
2	DA0+		
3	DA1-	Odd pixel data 1	Note1
4	DA1+		
5	DA2-	Odd pixel data 2	Note1
6	DA2+		
7	GND	Ground	-
8	CKA-	Odd pixel clock	Note1
9	CKA+		
10	DA3-	Odd pixel data 3	Note1
11	DA3+		
12	DB0-	Even pixel data 0	Note1
13	DB0+		
14	GND	Ground	-
15	DB1-	Even pixel data 1	Note1
16	DB1+		
17	GND	Ground	-
18	DB2-	Even pixel data 2	Note1
19	DB2+		
20	CKB-	Even pixel clock	Note1
21	CKB+		
22	DB3-	Even pixel data 3	Note1
23	DB3+		
24	GND	Ground	-
25	TxSEL	Selection of LVDS input map	High or Open: Mode A Low: Mode B Note2, Note3
26	RSVD	-	Keep this pin Open.
27	N.C.	-	Keep this pin Open.
28	VDD	Power supply	-
29			
30			

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be connected between LCD panel signal processing board and LVDS transmitter.
Note2: TxSEL is pulled-up in the product. (Pull-up resistance: 50kΩ)
Note3: See "**4.6 SELECTION OF LVDS INPUT MAP**".

4.5.2 Backlight lamp

Attention: VBLH and VBLC must be connected correctly. If customer connects wrongly, customer will be hurt and the module will be broken.

CN201 plug (LCD module side): BHSR-02VS-1 (J.S.T Mfg. Co., Ltd.)
Adaptable socket: SM02B-BHSS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: Pink
2	VBLC	Low voltage (Cold)	Cable color: Gray

CN202 plug (LCD module side): BHSR-02VS-1 (J.S.T Mfg. Co., Ltd.)
Adaptable socket: SM02B-BHSS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: White
2	VBLC	Low voltage (Cold)	Cable color: Gray

CN203 plug (LCD module side): BHSR-02VS-1 (J.S.T Mfg. Co., Ltd.)
Adaptable socket: SM02B-BHSS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: Sky blue
2	VBLC	Low voltage (Cold)	Cable color: Gray

CN204 plug (LCD module side): BHSR-02VS-1 (J.S.T Mfg. Co., Ltd.)
Adaptable socket: SM02B-BHSS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: Pink
2	VBLC	Low voltage (Cold)	Cable color: Gray

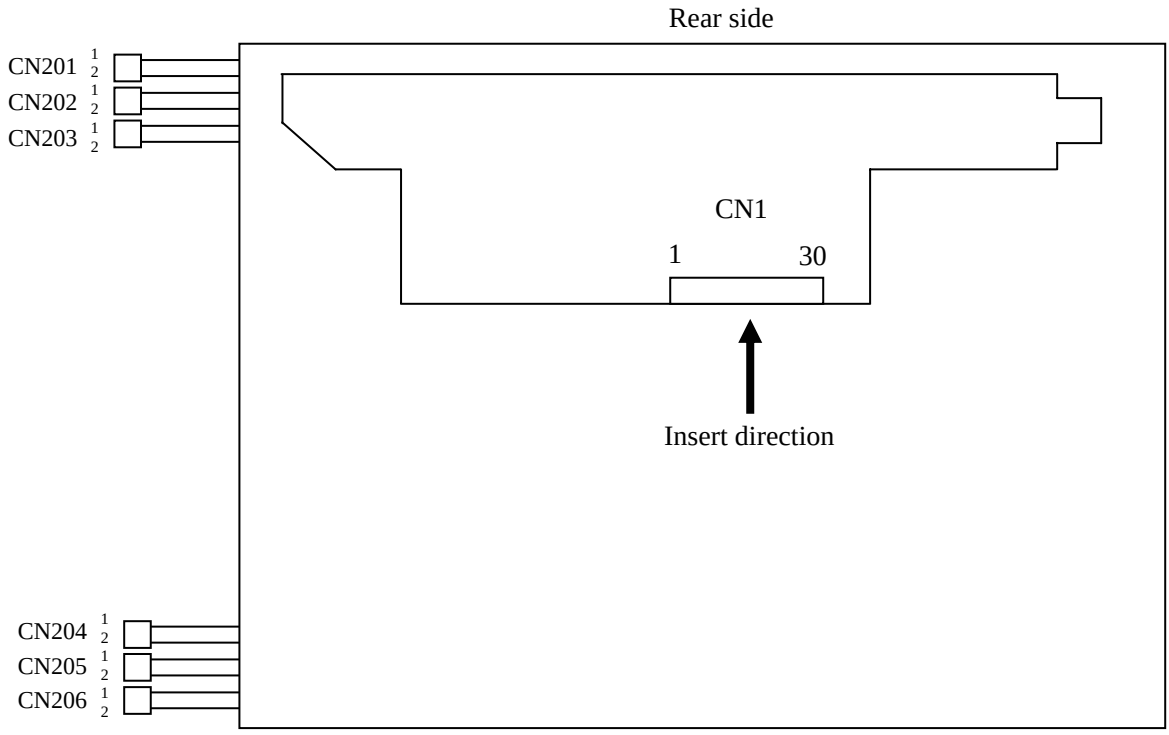
CN205 plug (LCD module side): BHSR-02VS-1 (J.S.T Mfg. Co., Ltd.)
Adaptable socket: SM02B-BHSS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: White
2	VBLC	Low voltage (Cold)	Cable color: Gray

CN206 plug (LCD module side): BHSR-02VS-1 (J.S.T Mfg. Co., Ltd.)
Adaptable socket: SM02B-BHSS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: Sky blue
2	VBLC	Low voltage (Cold)	Cable color: Gray

4.5.3 Positions of plugs and a socket



4.6 SELECTION OF LVDS INPUT MAP

4.6.1 Mode A

Input data		Note1		Transmitter Pin	Transmitter DS90CF383, C385 or equivalent			Note2	CN1 Pin	CN1 Symbol
Odd pixel data and control signal		LA0	→	51	TXIN0					
		LA1	→	52	TXIN1		TA1-	→	1	DA0-
		LA2	→	54	TXIN2		TA1+	→	2	DA0+
		LA3	→	55	TXIN3					
		LA4	→	56	TXIN4		TB1-	→	3	DA1-
		LA5	→	3	TXIN6		TB1+	→	4	DA1+
		CA0	→	4	TXIN7					
		CA1	→	6	TXIN8		TC1-	→	5	DA2-
		CA2	→	7	TXIN9		TC1+	→	6	DA2+
		CA3	→	11	TXIN12				7	GND
		CA4	→	12	TXIN13		TCLK1-	→	8	CKA-
		CA5	→	14	TXIN14		TCLK1+	→	9	CKA+
		RA0	→	15	TXIN15					
		RA1	→	19	TXIN18		TD1-	→	10	DA3-
		RA2	→	20	TXIN19	1st	TD1+	→	11	DA3+
		RA3	→	22	TXIN20					
		RA4	→	23	TXIN21					
		RA5	→	24	TXIN22					
	Note3	RSVD	→	27	TXIN24					
	Note3	RSVD	→	28	TXIN25					
		DE	→	30	TXIN26					
		LA6	→	50	TXIN27					
		LA7	→	2	TXIN5					
		CA6	→	8	TXIN10					
		CA7	→	10	TXIN11					
		RA6	→	16	TXIN16					
		RA7	→	18	TXIN17					
	Note3	RSVD	→	25	TXIN23					
		CLK	→	31	CLKIN					
Even pixel data		LB0	→	51	TXIN0					
		LB1	→	52	TXIN1		TA2-	→	12	DB0-
		LB2	→	54	TXIN2		TA2+	→	13	DB0+
		LB3	→	55	TXIN3				14	GND
		LB4	→	56	TXIN4		TB2-	→	15	DB1-
		LB5	→	3	TXIN6		TB2+	→	16	DB1+
		CB0	→	4	TXIN7				17	GND
		CB1	→	6	TXIN8		TC2-	→	18	DB2-
		CB2	→	7	TXIN9		TC2+	→	19	DB2+
		CB3	→	11	TXIN12					
		CB4	→	12	TXIN13		TCLK2-	→	20	CKB-
		CB5	→	14	TXIN14		TCLK2+	→	21	CKB+
		RB0	→	15	TXIN15					
		RB1	→	19	TXIN18		TD2-	→	22	DB3-
		RB2	→	20	TXIN19	2nd	TD2+	→	23	DB3+
		RB3	→	22	TXIN20				24	GND
		RB4	→	23	TXIN21				25	TxSEL
		RB5	→	24	TXIN22				26	RSVD
	Note3	RSVD	→	27	TXIN24				27	N.C.
	Note3	RSVD	→	28	TXIN25				28	VDD
	Note3	RSVD	→	30	TXIN26				29	VDD
		LB6	→	50	TXIN27				30	VDD
		LB7	→	2	TXIN5					
		CB6	→	8	TXIN10					
		CB7	→	10	TXIN11					
		RB6	→	16	TXIN16					
		RB7	→	18	TXIN18					
	Note3	RSVD	→	25	TXIN23					
		CLK	→	31	CLKIN					

4.6.2 Mode B

	Input data	Note1		Transmitter Pin	THC63LVDF83A/R or equivalent	Pin	THC63LVD823 or equivalent		Note2	CN1 Pin	CN1 Symbol
Odd pixel data and control signal		LA2	→	51	TA0	53	R12				
		LA3	→	52	TA1	54	R13	TA1-	→	1	DA0-
		LA4	→	54	TA2	57	R14	TA1+	→	2	DA0+
		LA5	→	55	TA3	58	R15				
		LA6	→	56	TA4	59	R16	TB1-	→	3	DA1-
		LA7	→	3	TA5	60	R17	TB1+	→	4	DA1+
		CA2	→	4	TA6	63	G12				
		CA3	→	6	TB0	64	G13	TC1-	→	5	DA2-
		CA4	→	7	TB1	65	G14	TC1+	→	6	DA2+
		CA5	→	11	TB2	66	G15			7	GND
		CA6	→	12	TB3	67	G16	TCLK1-	→	8	CKA-
		CA7	→	14	TB4	68	G17	TCLK1+	→	9	CKA+
		RA2	→	15	TB5	73	B12				
		RA3	→	19	TB6	74	B13	TD1-	→	10	DA3-
		RA4	→	20	TC0 1st	75	B14	TD1+	→	11	DA3+
		RA5	→	22	TC1	76	B15				
		RA6	→	23	TC2	77	B16				
		RA7	→	24	TC3	78	B17				
	Note3	RSVD	→	27	TC4	7	RSVD				
	Note3	RSVD	→	28	TC5	8	RSVD				
		DE	→	30	TC6	9	DE				
		LA0	→	50	TD0	51	R10				
		LA1	→	2	TD1	52	R11				
		CA0	→	8	TD2	61	G10				
		CA1	→	10	TD3	62	G11				
		RA0	→	16	TD4	69	B10				
		RA1	→	18	TD5	70	B11				
	Note3	RSVD	→	25	TD6	-					
		CLK	→	31	CLKIN	10	CLK				
Even pixel data		LB2	→	51	TA0	81	R22				
		LB3	→	52	TA1	82	R23	TA2-	→	12	DB0-
		LB4	→	54	TA2	83	R24	TA2+	→	13	DB0+
		LB5	→	55	TA3	84	R25			14	GND
		LB6	→	56	TA4	85	R26	TB2-	→	15	DB1-
		LB7	→	3	TA5	86	R27	TB2+	→	16	DB1+
		CB2	→	4	TA6	91	G22			17	GND
		CB3	→	6	TB0	92	G23	TC2-	→	18	DB2-
		CB4	→	7	TB1	93	G24	TC2+	→	19	DB2+
		CB5	→	11	TB2	94	G25				
		CB6	→	12	TB3	95	G26	TCLK2-	→	20	CKB-
		CB7	→	14	TB4	96	G27	TCLK2+	→	21	CKB+
		RB2	→	15	TB5	99	B22				
		RB3	→	19	TB6	100	B23	TD2-	→	22	DB3-
		RB4	→	20	TC0 2nd	1	B24	TD2+	→	23	DB3+
		RB5	→	22	TC1	2	B25			24	GND
		RB6	→	23	TC2	5	B26			25	TxSEL
		RB7	→	24	TC3	6	B27			26	RSVD
	Note3	RSVD	→	27	TC4	-				27	N.C.
	Note3	RSVD	→	28	TC5	-				28	VDD
	Note3	RSVD	→	30	TC6	-				29	VDD
		LB0	→	50	TD0	79	R20			30	VDD
		LB1	→	2	TD1	80	R21				
		CB0	→	8	TD2	89	G20				
		CB1	→	10	TD3	90	G21				
		RB0	→	16	TD4	97	B20				
		RB1	→	18	TD5	98	B21				
	Note3	RSVD	→	25	TD6	-					
		CLK	→	31	CLKIN	-					

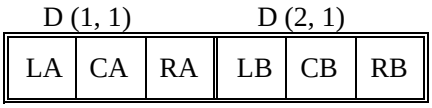
Note1: LSB (Least Significant Bit) – LA0, CA0, RA0, LB0, CB0, RB0
MSB (Most Significant Bit) – LA7, CA7, RA7, LB7, CB7, RB7
Note2: Twist pair wires with 100Ω (Characteristic impedance) should be connected between LCD panel signal processing board and LVDS transmitter.
Note3: Input signal RSVD is not used inside the product, but do not keep this pin open to avoid noise problem.

4.7 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display 256 gray scales in each LCR sub-pixel and 766 gray scales per 1 pixel. Also the relation between display gray scale and input data signals is as the following table.

Display grayscale		Data signal (0: Low level, 1: High level)																									
		LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
		LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
Left dot gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑					:								:								:			
	↓					:								:								:			
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Center dot gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑					:								:								:			
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	White	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Right dot gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑					:								:								:			
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	White	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

4.8 DISPLAY POSITION



D(1, 1)	D(2, 1)	•••	D(1280, 1)
D(1, 2)	D(2, 2)	•••	D(1280, 2)
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
D(1,1024)	D(2, 1024)	•••	D(1280, 1024)

4.9 INPUT SIGNAL TIMINGS

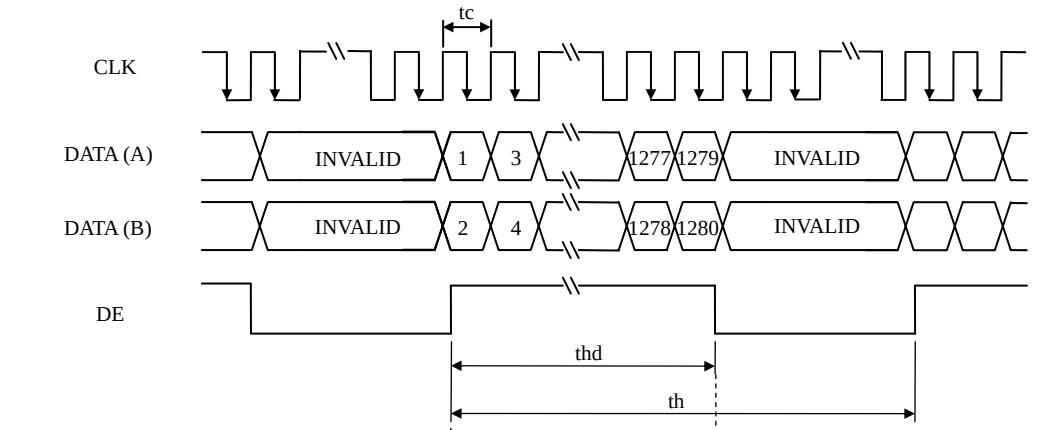
4.9.1 Timing characteristics

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/tc	49	54	59	MHz	18.52 ns (typ.)
	Duty		-		-		-	Note2
	Rise time, Fall time		-				ns	
DATA	CLK-DATA	Setup time	-		-		ns	Note2
		Hold time	-				ns	
	Rise time, Fall time		-				ns	
DE	Horizontal	Cycle	th	12.3	15.63	20.59	µs	64.0 kHz (typ.) Note1, Note2, Note3
				660	844	1,024	CLK	
		Display period	thd		640		CLK	
	Vertical (One frame)	Cycle	tv	13.1	16.6	17.5	ms	60.0 Hz (typ.) Note1
				1,030	1,066	1,422	H	
		Display period	tvd		1,024		H	
	CLK-DE	Setup time	-		-		ns	Note2
		Hold time	-				ns	
	Rise time, Fall time		-				ns	

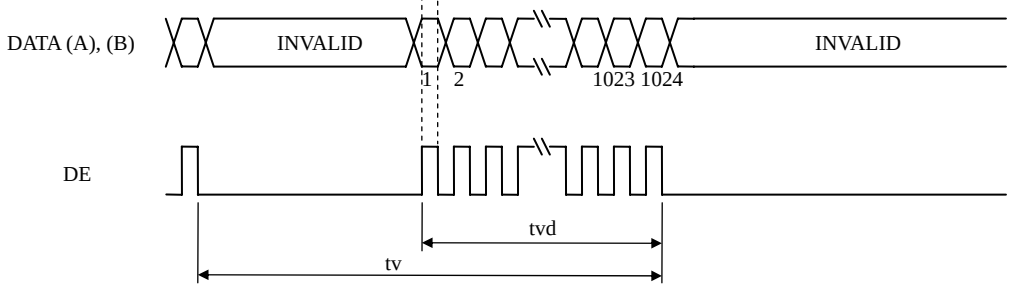
Note1: Definition of parameters is as follows.
tc = 1CLK, th = 1H
Note2: See the data sheet of LVDS transmitter.
Note3: "th" must keep the fluctuation within ±1 CLK, because of avoidance of image sticking.

4.9.2 Input signal timing chart

Horizontal timing



Vertical timing



Note1: DATA (A)= LA0-LA7, CA0-CA7, RA0-RA7
DATA (B)= LB0-LB7, CB0-CB7, RB0-RB7

4.10 OPTICS

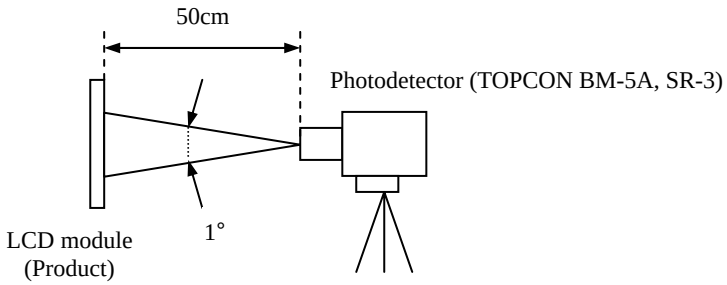
4.10.1 Optical characteristics

(Note1, Note2)

Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks
Luminance		White at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	L	(600)	(800)	-	cd/m^2	BM-5A or SR-3	-
Contrast ratio		White/Black at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	CR	(400)	(700)	-	-	BM-5A or SR-3	Note3
Luminance uniformity		White θR = 0°, θL = 0°, θU = 0°, θD = 0°	LU	-	1.2	1.3	-	BM-5A	Note4
Chromaticity	White	**x** coordinate	Wx	-	0.255	-	-	SR-3	Note5
		y coordinate	Wy	-	0.310	-	-		
Response time		Black to White	Ton	-	(18)	(28)	ms	BM-5A	Note6 Note7
		White to Black	Toff	-	(17)	(27)	ms		
Viewing angle	Right	θU = 0°, θD = 0°, CR ≥ 10	θR	70	85	-	°	BM-5A	Note8
	Left	θU = 0°, θD = 0°, CR ≥ 10	θL	70	85	-	°		
	Up	θR = 0°, θL = 0°, CR ≥ 10	θU	70	85	-	°		
	Down	θR = 0°, θL = 0°, CR ≥ 10	θD	70	85	-	°		

Note1: These are initial characteristics.
Note2: Measurement conditions are as follows.
Ta = 25°C, VDD = 5.0V, IBL = 6.0mArms/lamp, Display mode: SXGA, Horizontal cycle = 64.0kHz, Vertical cycle = 60.0Hz

Optical characteristics are measured after 20minutes from working the product, in the dark room. Also measurement method for luminance is as follows.



Note3: See "**4.10.2 Definition of contrast ratio**".
Note4: See "**4.10.3 Definition of luminance uniformity**".
Note5: These coordinates are found on CIE 1931 chromaticity diagram.
Note6: Product surface temperature: TopF = (35)°C
Note7: See "**4.10.4 Definition of response times**".
Note8: See "**4.10.5 Definition of viewing angles**".

4.10.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

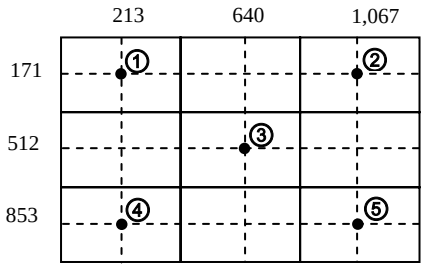
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.10.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

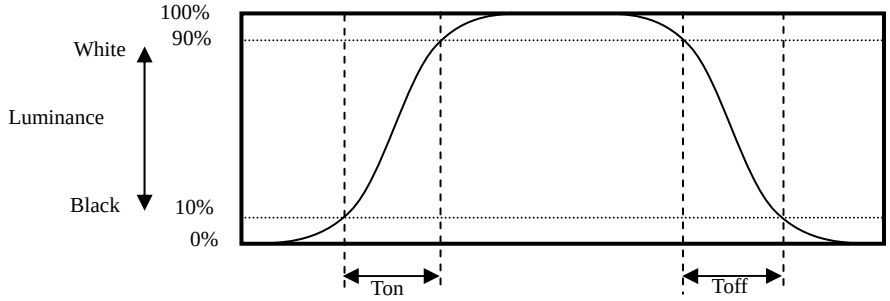
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

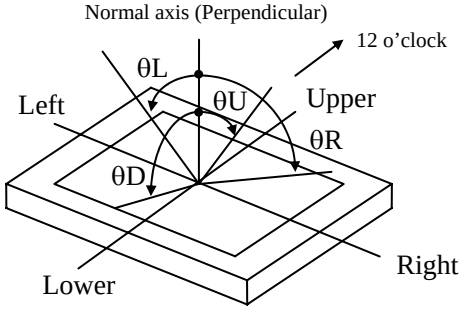


4.10.4 Definition of response times

Response time is measured, the luminance changes from " black " to " white ", or " white " to " black " on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



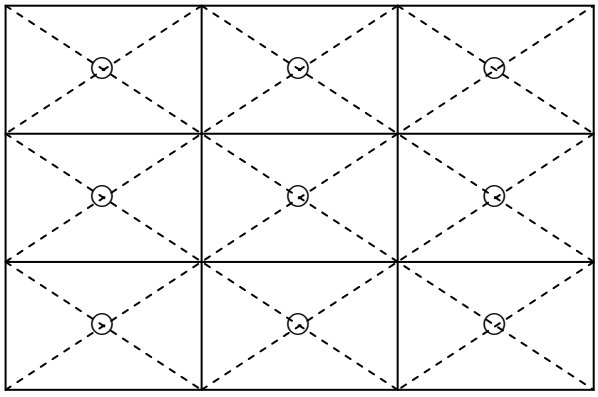
4.10.5 Definition of viewing angles



5. RELIABILITY TESTS

Test item		Condition	Judgment Note1
High temperature and humidity (Operation)		① 60 ± 2°C, RH = 60%, 240hours ② Display data is white.	No display malfunctions
Heat cycle (Operation)		① 0 ± 3°C…1hour 55 ± 3°C…1hour ② 50cycles, 4hours/cycle ③ Display data is white.	
Thermal shock (Non operation)		① -20 ± 3°C…30minutes 60 ± 3°C…30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s^2 ② 1 minute/cycle ③ X, Y, Z direction ④ 10 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)		① (294)m/ s^2, 11ms ② X, Y, Z direction ③ 3 times each directions	
ESD (Operation)		① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	No display malfunctions
Dust (Operation)		① Sample dust: No.15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	
Low pressure	Operation	① 53.3 kPa ② 0°C±3°C…24 hours ③ 55°C±3°C…24 hours	
	Non-operation	① 15 kPa ② -20°C±3°C…24 hours ③ 60°C±3°C…24 hours	

Note1: Display functions are checked under the same conditions as product inspection.
Note2: See the following figure for discharge points



6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding this contents!**

	This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.
	This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.
	This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS

∗ Do not touch the working backlight. Customer will be in danger of an electric shock.

∗ Do not touch the working backlight. Customer will be in danger of burn injury.
∗ Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater (294)m/s^2 and to be not greater 11ms, Pressure: To be not greater 19.6 N)

6.3 ATTENTIONS 

6.3.1 Handling of the product

① Take hold of both ends without touch the circuit board cover when customer pulls out products (LCD modules) from inner packing box. If customer touches it, products may be broken down or out of adjustment, because of stress to mounting parts.
② Do not hook cables nor pull connection cables such as lamp cable and so on, for fear of damage.
③ If customer puts down the product temporarily, the product puts on flat subsoil as a display side turns down.
④ Take the measures of electrostatic discharge such as earth band, ionic shower and so on, when customer deals with the product, because products may be damaged by electrostatic.
⑤ The torque for mounting screws must never exceed 0.67N·m. Higher torque values might result in distortion of the bezel. And the screw length must be 4.0mm to 7.0mm.
⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area) except mounting hole portion.
Bends or twist described above and undue stress to any portion except mounting hole portion may cause display un-uniformity.
⑦ Do not press or rub on the sensitive display surface. If customer clean on the panel surface, NEC recommends using the cloth with ethanolic liquid such as screen cleaner for LCD.
⑧ Do not push-pull the interface connectors while the product is working, because wrong power sequence may break down the product.

⑨ When installing the lamp cable, do not attach the lamp cable on the metal part of the LCD module directly. This may cause leakage high frequency current to the metal part, then the brightness may decrease or the lamp may not light.
⑩ When installing the lamp cable, do not locate the lamp cable on the signal processing board. A noise may occur on the display image.
⑪ When customer deals with the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of panel surface. Adhesive type protection sheet may change color or properties of the polarizer.

6.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in antistatic pouch in room temperature, because of avoidance for dusts and sunlight, if customer stores the product.
② In order to prevent dew condensation occurring by temperature difference, the product packing box must be opened after leave under the environment of an unpacking room temperature enough. Because a situation of dew condensation occurring is changed by the environmental temperature and humidity, evaluate the leaving time sufficiently. (Recommendation leaving time: 6 hour or more with packing state)
③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
④ This product is not designed as radiation hardened.

6.3.3 Characteristics

The following items are neither defects nor failures.

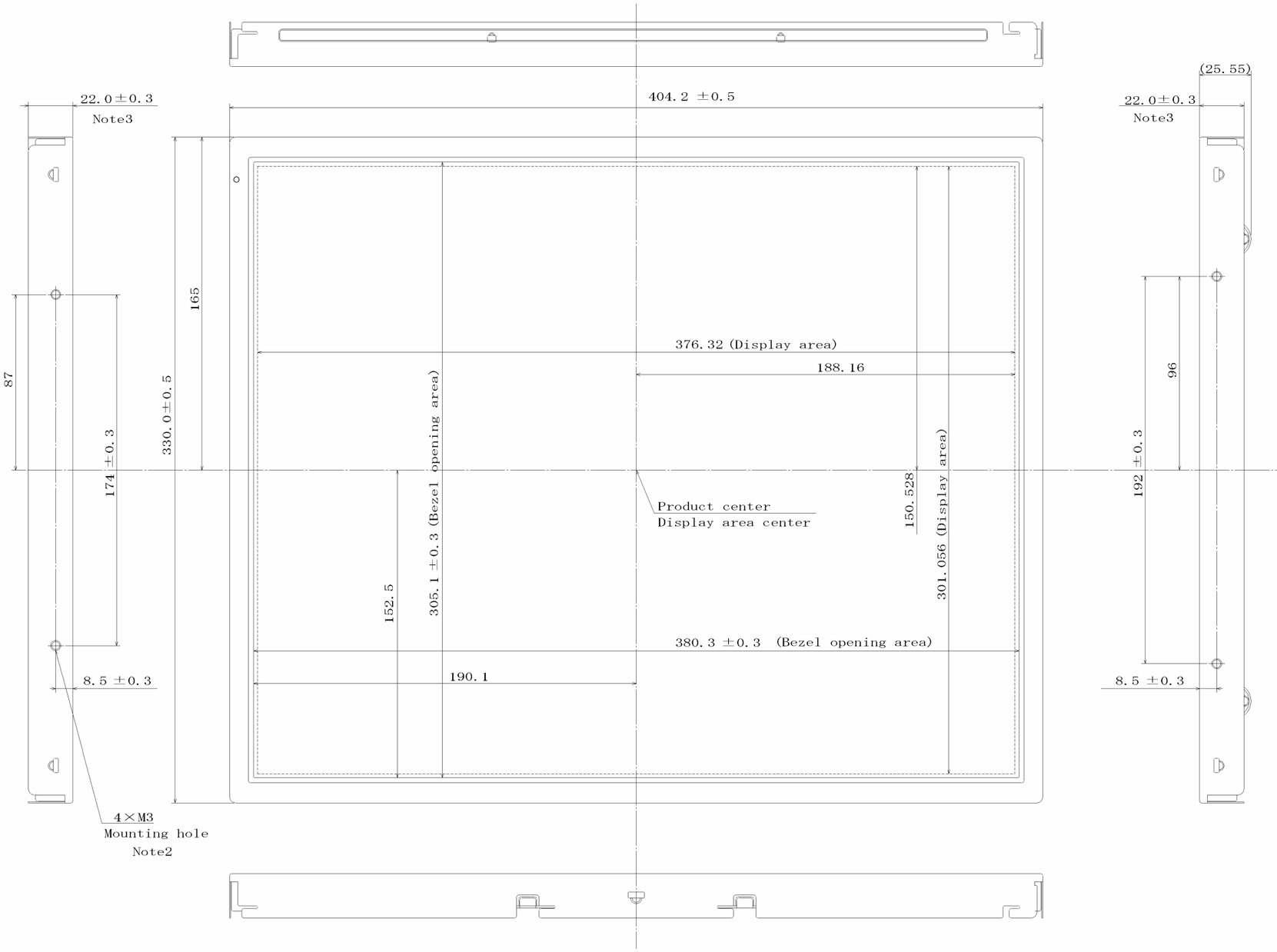
① Response time, luminance and color may be changed by ambient temperature.
② The LCD may be seemed luminance non-uniformity, flicker, vertical seam or small spot by display patterns.
③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
⑤ The display color may be changed by viewing angle because of the use of condenser sheet in the backlight.
⑥ Optical characteristics may be changed by input signal timings.
⑦ The interference noise of input signal frequency for this product's signal processing board and luminance control frequency of customer's backlight inverter may appear on a display. Set up luminance control frequency of backlight inverter so that the interference noise does not appear.

6.3.4 Other

① All GND and VDD terminals should be used without a non-connected line.
② Do not disassemble a product or adjust variable resistors without permission of NEC.
③ Pay attention not to insert waste materials inside of products, if customer uses screwnails.
④ Pack the product with original shipping package, because of avoidance of some damages during transportation, when customer returns it to NEC for repair and so on.
⑤ The LCD module by itself or integrated into end product should be packed and transported with display in the vertically position. Otherwise the display characteristics may be impaired.

7. OUTLINE DRAWINGS

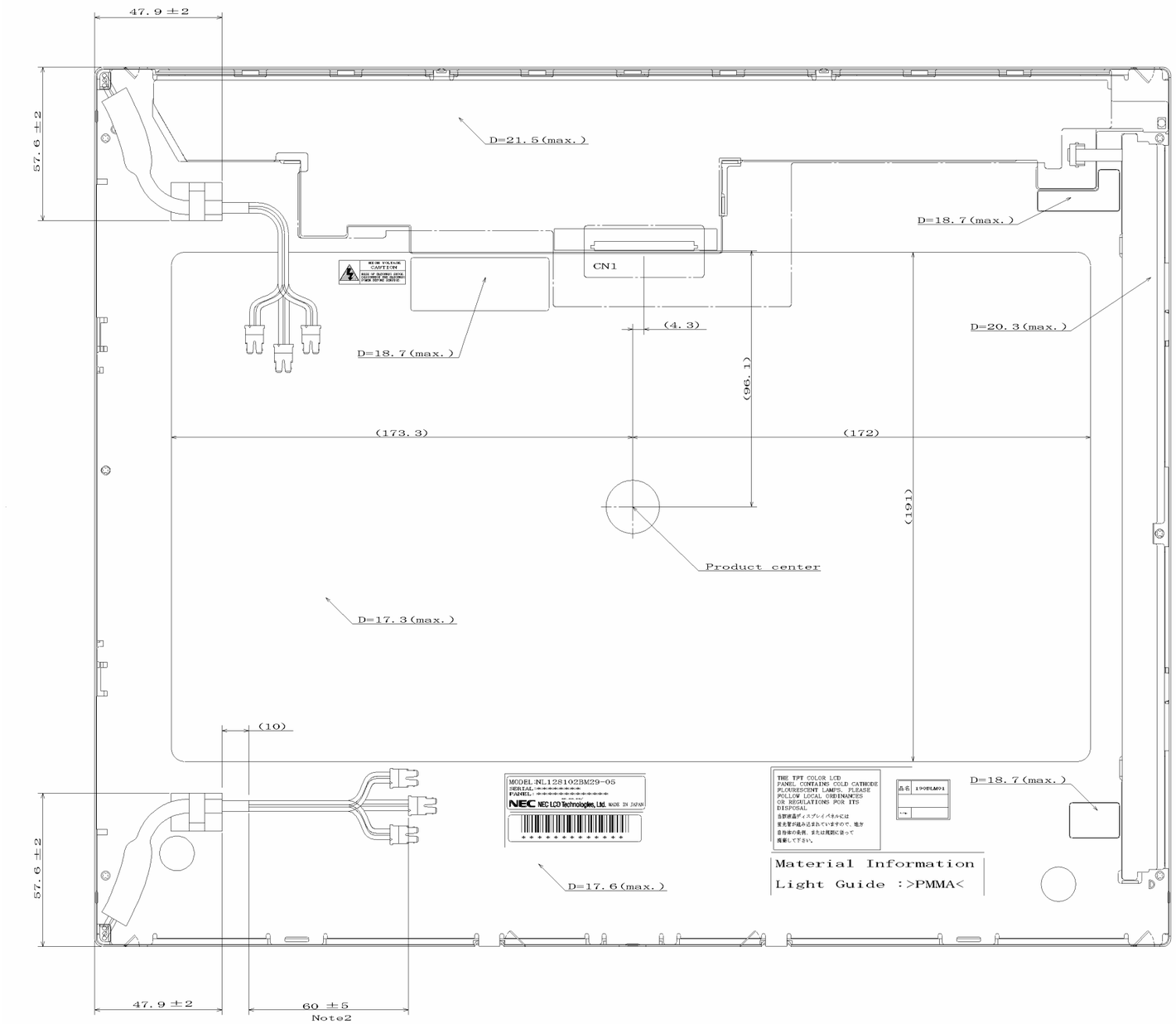
7.1 FRONT VIEW



Note1: Not shown tolerances of the dimensions are TBD.
Note2: The torque for mounting screws must never exceed 0.67N·m. And the screw length must be 4.0mm to 7.0mm.
Note3: Excluding lamp cable and cable clamp.
Note4: The values in parentheses are for reference.

Unit: mm

7.2 REAR VIEW



Note1: Not shown tolerances of the dimensions are TBD.

Note2: The structure of up side and down side lamp cable is the same.

Unit: mm

REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Prepared date	Revision contents and signature
1st edition	May 12, 2004	**Revision contents** New issue **Signature of writer** *Approved by* T. ITO *Checked by* *Prepared by* R. KAWASHIMA