

PRELIMINARY

**NEC** NEC LCD Technologies, Ltd.

# TFT MONOCHROME LCD MODULE

**NL160120AM27-13A**

**54 cm (21.3 Type)**

**UXGA**

**LVDS Interface (2 ports)**

**PRELIMINARY DATA SHEET** 

**DOD-PD-1308 (1st edition)**

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starting to design your system.**

## INTRODUCTION

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Examples: Military systems, aircraft control equipment, aerospace equipment, nuclear reactor control systems, medical equipment/devices/systems for life support, etc.

The quality grade of this product is the "**Standard**" unless otherwise specified in this document.

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## 1. OUTLINE

### 1.1 STRUCTURE AND PRINCIPLE

Monochrome LCD module NL160120AM27-13A is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a monochrome-filter glass substrate.

Grayscale data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Monochrome images are created by regulating the amount of transmitted light through the TFT array.

### 1.2 APPLICATION

- Monochrome monitor system

### 1.3 FEATURES

- Ultra-wide viewing angle (Adoption of Super-Advanced Super Fine TFT (SA-SFT))
- High luminance
- High contrast
- High resolution
- 256 gray scales per 1 sub-pixel (8-bit)
- LVDS interface
- Adjustable gamma characteristics by using built-in 10-bit LUT (look up table)
- Selectable LVDS data input map
- Small foot print
- Incorporated direct light type backlight
- Replaceable inverter

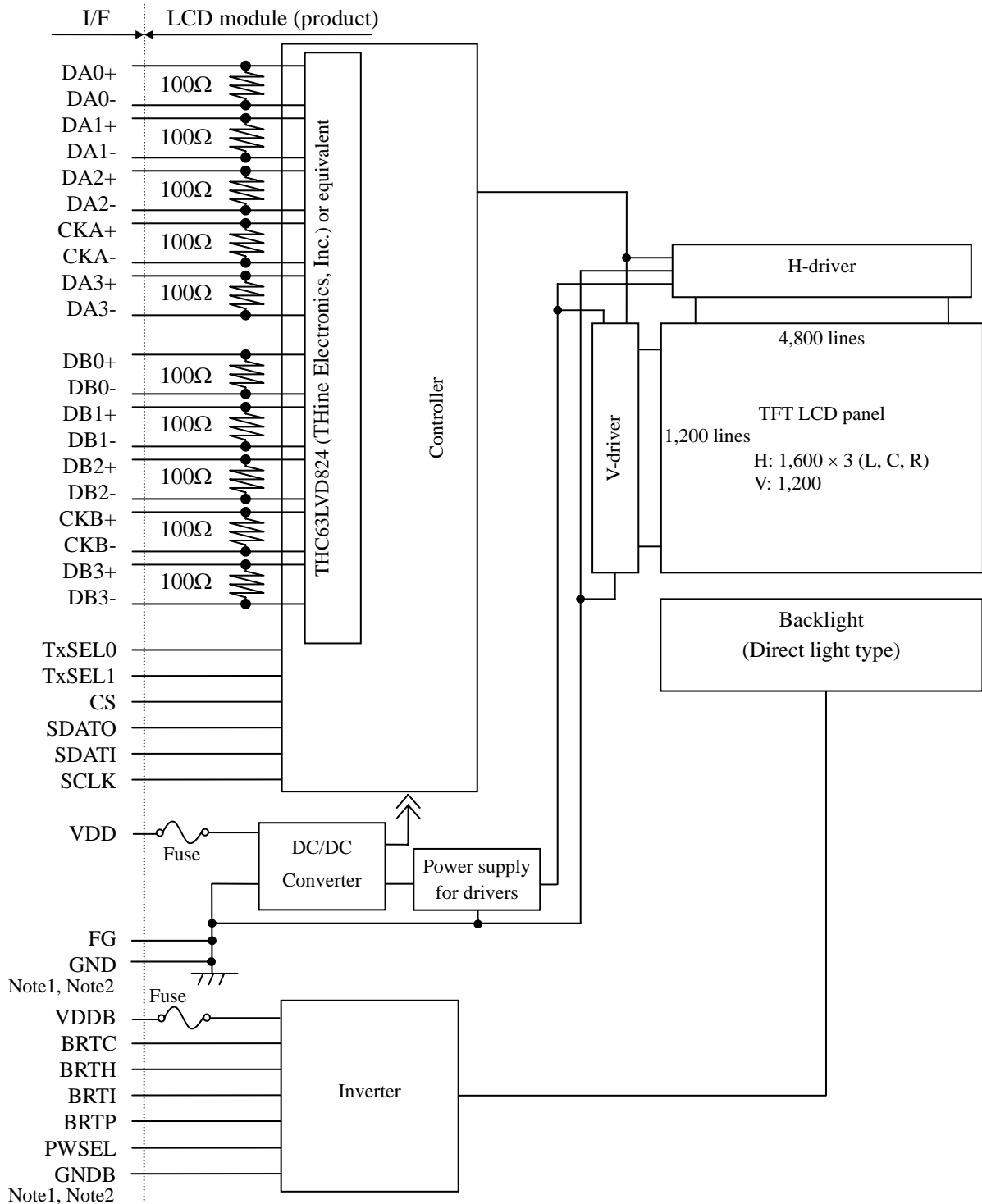
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## 2. GENERAL SPECIFICATIONS

<b>Display area</b>	432.0 (H) × 324.0 (V) mm
<b>Diagonal size of display</b>	54 cm (21.3 inches)
<b>Drive system</b>	a-Si TFT active matrix
<b>Display grayscale</b>	256 gray scales per 1 sub-pixel (8-bit) (766 gray scales per 1 pixel)
<b>Pixel</b>	1,600 (H) × 1,200 (V) pixels (1 pixel consists of 3 sub-pixels (LCR).)
<b>Pixel arrangement</b>	LCR vertical stripe
<b>Dot pitch</b>	0.090 (H) × 0.270 (V) mm
<b>Pixel pitch</b>	0.270 (H) × 0.270 (V) mm
<b>Module size</b>	457.0 (W) × 350.0 (H) × 34.0 (D) mm (typ.)
<b>Weight</b>	2,900 g (typ.)
<b>Contrast ratio</b>	900:1 (typ.)
<b>Viewing angle</b>	At the contrast ratio $\geq 10:1$ <ul style="list-style-type: none"> <li>• Horizontal: Right side 85° (typ.), Left side 85° (typ.)</li> <li>• Vertical: Up side 85° (typ.), Down side 85° (typ.)</li> </ul>
<b>Designed viewing direction</b>	Viewing angle with optimum grayscale ( $\gamma = \text{DICOM}$ ): normal axis (perpendicular) <div style="text-align: right;">Note1</div>
<b>Polarizer surface</b>	Antiglare
<b>Polarizer pencil-hardness</b>	2H (min.) [by JIS K5400]
<b>Response time</b>	$T_{on} + T_{off}$ (10% $\leftrightarrow$ 90%) 45 ms (typ.)
<b>Luminance</b>	At the maximum luminance control 1,800 cd/m <sup>2</sup> (typ.)
<b>Signal system</b>	2 ports LVDS interface (THC63LVD824 THine Electronics, Inc. or equivalent) [LCR 8-bit signals, Data enable signal (DE), Dot clock (CLK)]
<b>Power supply voltage</b>	LCD panel signal processing board: 12.0V Inverter: 12.0V
<b>Backlight</b>	Direct light type: 16 cold cathode fluorescent lamps with an inverter <div style="border-left: 1px solid black; border-right: 1px solid black; border-bottom: 1px solid black; padding: 5px; margin-left: 20px;">                     Replaceable part                      • Inverter: 213PW041                 </div>
<b>Power consumption</b>	At checkered flag pattern, the maximum luminance control 63.7 W (typ.)

Note1: When the product luminance is 500cd/m<sup>2</sup>, the gamma characteristic is designed to  $\gamma = \text{DICOM}$ .

### 3. BLOCK DIAGRAM



Note1: Connections between GND (Signal ground), FG (Frame ground) and GNDB (Inverter ground) in the product

GND - FG	Connected
GND - GNDB	Not connected
FG - GNDB	Not connected

Note2: GND, FG and GNDB must be connected to customer equipment's ground, and it is recommended that these grounds are connected together in customer equipment.

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## 4. DETAILED SPECIFICATIONS

### 4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	457.0 ±0.5 (W) × 350.0 ±0.5 (H) × 34.0 (typ., D) 37.0 (max. D) Note1, Note2	mm
Display area	432.0 (H) × 324.0 (V) Note1	mm
Weight	2,900 (typ.), 3,100 (max.)	g

Note1: Excluding warpage of the signal processing board cover and the connection board cover

Note2: See "7. OUTLINE DRAWINGS".

### 4.2 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit	Remarks	
Power supply voltage	LCD panel signal processing board	VDD	-0.3 to +14.0	V	-	
	Inverter	VDDDB	-0.3 to +15.0	V		
Input voltage for signals	LCD panel signal processing board Note1	V <sub>i</sub>	-0.3 to +2.8	V	VDD= 12.0V	
	Inverter	BRTI signal	VBI	-0.3 to +1.5	V	VDDDB= 12.0V
		BRTP signal	VBP	-0.3 to +5.5	V	
		BRTC signal	VBC	-0.3 to +5.5	V	
	PWSEL signal	VBS	-0.3 to +5.5	V		
Storage temperature		T <sub>st</sub>	-20 to +60	°C	-	
Operating temperature	Front surface	TopF	0 to +55	°C	Note2	
	Rear surface	TopR	0 to +60	°C	Note3	
Relative humidity Note4		RH	≤ 70	%	T <sub>a</sub> ≤ 55°C	
Absolute humidity Note4		AH	≤ 73 Note5	g/m <sup>3</sup>	T <sub>a</sub> > 55°C	
Operating altitude		-	≤ 4,850	m	0°C ≤ T <sub>a</sub> ≤ 55°C	
Storage altitude		-	≤ 13,600	m	-20°C ≤ T <sub>a</sub> ≤ 60°C	

Note1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-  
CS, SDATI, SCLK, TxSEL0, TxSEL1

Note2: Measured at center of LCD panel surface (including self-heat)

Note3: Measured at center of LCD module's rear shield surface (including self-heat)

Note4: No condensation

Note5: Water amount at T<sub>a</sub> = 55°C and RH = 70%

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## 4.3 ELECTRICAL CHARACTERISTICS

### 4.3.1 LCD panel signal processing board

(Ta = 25°C)

Parameter	Symbol	min.	typ.	max.	Unit	Remarks	
Supply voltage	VDD	10.8	12.0	13.2	V	-	
Supply current	IDD	-	310 Note1	700 Note2	mA	at VDD=12.0V	
Ripple voltage	VRP	-	-	100	mVp-p	for VDD	
Differential input Threshold voltage	VTH	-	-	+100	mV	at VCM=1.2V Note3, Note4	
	VTL	-100	-	-	mV		
Input voltage swing	VI	0	-	2.4	V	Note4	
Terminating resistance	RT	-	100	-	Ω	-	
Control signal input threshold voltage	High	VIH	Keep this pin open.			-	Note5
	Low	VIL	0	-	0.5	V	
Control signal input current	Low	IIL	-10	-	10	μA	
Serial communication signal input threshold voltage	High	V+	-	1.4	1.9	V	Note6
	Low	V-	0.4	0.7	-	V	
	Hysteresis	VH	0.3	-	-	V	
Output signal threshold voltage	High	VOH	1.9	-	-	V	Note7
	Low	VOL	-	-	0.4	V	
Output signal current	High	IOH	-4	-	-	mA	
	Low	IOL	-	-	4	mA	

Note1: Checkered flag pattern (by EIAJ ED-2522)

Note2: Pattern for maximum current

Note3: Common mode voltage for LVDS driver

Note4: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-

Note5: TXSEL0, TXSEL1

Note6: CS, SDATI, SCLK

Note7: SDATO

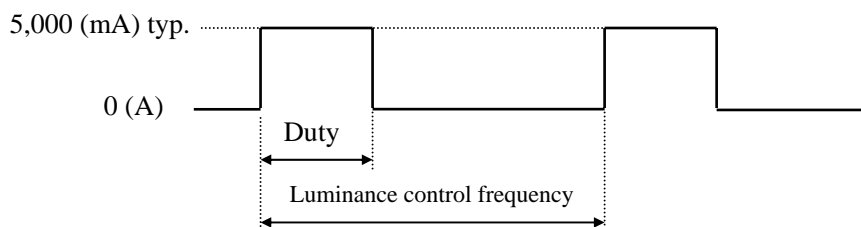


### 4.3.2 Inverter

(Ta = 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDDB	11.4	12.0	12.6	V	-
Power supply current		IDDB	-	5,000	5,700	mA	VDDB = 12.0V, At the maximum luminance control
Input voltage for signals	BRTI signal		VBI	0.25	-	1.0	V
	BRTP signal	High	VBPH	2.0	-	5.25	V
		Low	VBPL	0	-	0.8	V
	BRTC signal	High	VBCH	2.0	-	5.25	V
		Low	VBCL	0	-	0.8	V
	PWSEL signal	High	VBSH	2.0	-	5.25	V
Low		VBSL	0	-	0.8	V	
Input current for signals	BRTI signal		IBI	-200	-	1,000	μA
	BRTP signal	High	IBPH	-	-	1,000	μA
		Low	IBPL	-600	-	-	μA
	BRTC signal	High	IBCH	-	-	400	μA
		Low	IBCL	-600	-	-	μA
	PWSEL signal	High	IBSH	-	-	440	μA
Low		IBSL	-600	-	-	μA	

### 4.3.3 Inverter current wave



Maximum luminance control: 100%  
 Minimum luminance control: 20%  
 Luminance control frequency: 255Hz (typ.)

Note1: Luminance control frequency indicate the input pulse frequency, when select the external pulse control. See "4.6.2 Detail of BRTP timing".

Note2: The power supply lines (VDDB and GNDB) have large ripple voltage (See "4.3.4 Power supply voltage ripple".) during luminance control. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on. Put a capacitor (5,000 to 6,000μF) between the power supply lines (VDDB and GNDB) to reduce the noise, if the noise occurred in the circuit..

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### 4.3.4 Power supply voltage ripple

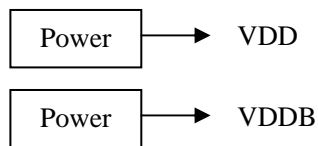
This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage (Measure at input terminal of power supply)	Note1 Unit
VDD	12.0 V	≤ 100	mVp-p
VDDDB	12.0 V	≤ 200	mVp-p

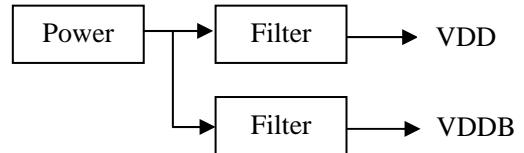
Note1: The permissible ripple voltage includes spike noise.

Example of the power supply connection

a) Separate the power supply



b) Put in the filter



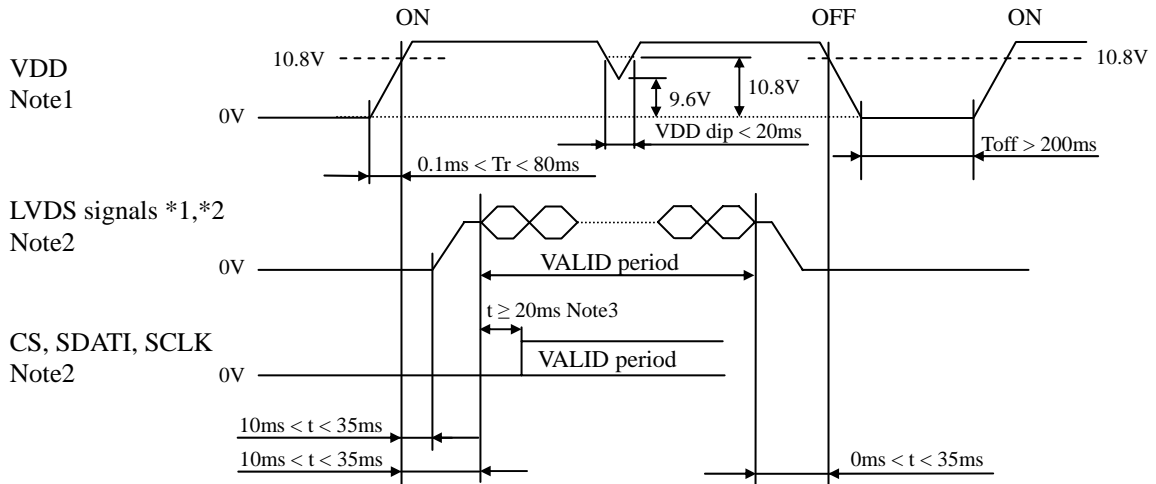
### 4.3.5 Fuse

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	FCC16132AB	KAMAYA ELECTRIC Co., Ltd.	1.25A	2.5A, 5 seconds maximum	Note1
			32V		
VDDDB	0453010	Littelfuse Inc.	10A	20A, 5 seconds maximum	
			125V		

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

## 4.4 POWER SUPPLY VOLTAGE SEQUENCE

### 4.4.1 LCD panel signal processing board



\*1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/- and CKB+/-

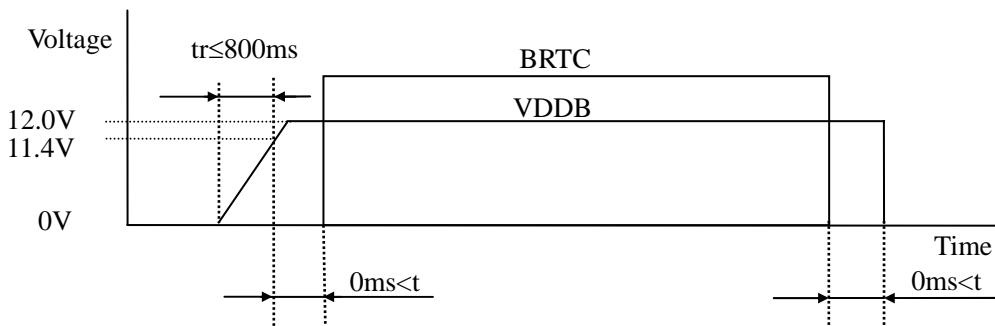
\*2: LVDS signals should be measured at the terminal of 100Ω resistance.

Note1: In terms of voltage variation (voltage drop) while VDD rising edge is below 10.8V, a protection circuit may work, and then this product may not work.

Note2: LVDS signals and CS, SDATI, SCLK must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged. If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. VDD should be cut when the display and function signals are stopped.

Note3: At the beginning of the serial communication mode, take 20ms or more after the LVDS signal input. As writing and reading the LUT data, see “4.11 TEN-bit LOOK UP TABLE FOR GAMMA ADJUSTMENT”.

### 4.4.2 Inverter



Note1: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.

Note2: If  $tr$  is more than 800ms, the backlight will be turned off by a protection circuit for inverter.

Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

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## 4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

### 4.5.1 LCD panel signal processing board

#### (1) CN1

Socket (LCD module side): DF19G-30P-1H (56) (Hirose Electric Co., Ltd. (HRS))

Adaptable plug: DF19-30S-1C (Hirose Electric Co., Ltd. (HRS))

Pin No.	Symbol	Signal	Remarks			
1	DA0-	Pixel data A0	Odd pixel data Input (LVDS differential signal) Note1			
2	DA0+					
3	DA1-	Pixel data A1	Odd pixel data Input (LVDS differential signal) Note1			
4	DA1+					
5	DA2-	Pixel data A2	Odd pixel data Input (LVDS differential signal) Note1			
6	DA2+					
7	GND	Ground	Signal ground Note2			
8	CKA-	Pixel clock	Odd pixel clock Input (LVDS differential signal) Note1			
9	CKA+					
10	DA3-	Pixel data A3	Odd pixel data Input (LVDS differential signal) Note1			
11	DA3+					
12	DB0-	Pixel data B0	Even pixel data Input (LVDS differential signal) Note1			
13	DB0+					
14	GND	Ground	Signal ground Note2			
15	DB1-	Pixel data B1	Even pixel data Input (LVDS differential signal) Note1			
16	DB1+					
17	GND	Ground	Signal ground Note2			
18	DB2-	Pixel data B2	Even pixel data Input (LVDS differential signal) Note1			
19	DB2+					
20	CKB-	Pixel clock	Even pixel clock Input (LVDS differential signal) Note1			
21	CKB+					
22	DB3-	Pixel data B3	Even pixel data Input (LVDS differential signal) Note1			
23	DB3+					
24	GND	Ground	Signal ground Note2			
25	TxSEL0	Selection of LVDS data input map	Note3, Note4	TxSEL1	TxSEL0	Mode
26	TxSEL1			Open	Open	A
				Open	Low	B
				Low	Open	C
		Low	Low	A		
27	GND	Ground	Signal ground Note2			
28	VDD	Power supply	12V Note2			
29	VDD					
30	VDD					

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

Note2: All GND and VDD terminals should be used without any non-connected lines.

Note3: This terminal is pulled-up in the product. (Pull-up resistance: 50kΩ)

Note4: See "**4.7 LVDS DATA INPUT MAP**".

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(2) CN3

Socket (LCD module side): SM10B-SRSS-TB(LF)(SN) (J.S.T. Mfg Co., Ltd.)

Adaptable plug: SHR-10V-S, SHR-10V-S-B or 10SR-3S (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	RSVD	Reserved	Keep this pin Open.
2	RSVD	Reserved	Keep this pin Open.
3	RSVD	Reserved	Keep this pin Open.
4	GND	Ground	Signal ground Note1
5	CS	Chip selection	For LUT communication control Note2
6	SDATO	Serial data output	For LUT output signal
7	SDATI	Serial data input	For LUT communication control Note3
8	SCLK	Serial clock	For LUT communication control Note3
9	GND	Ground	Signal ground Note1
10	RSVD	Reserved	Keep this pin Open.

Note1: All GND terminals should be used without any non-connected lines.

Note2: This terminal is pulled-up in the product. (Pull-up resistance: 50kΩ)

Note3: These terminals are pulled-down in the product. (Pull-down resistance: 50kΩ)

4.5.2 Inverter

CN201 socket (LCD module side): DF3Z-10P-2H (2\*) (HIROSE ELECTRIC Co.,Ltd.)

Adaptable plug: DF3-10S-2C (HIROSE ELECTRIC Co.,Ltd.)

Pin No.	Symbol	Function	Description
1	GNDB	Inverter ground	Note1
2	GNDB		
3	GNDB		
4	GNDB		
5	GNDB		
6	VDDB	Power supply	Note1
7	VDDB		
8	VDDB		
9	VDDB		
10	VDDB		

Note1: All VDDB and GNDB terminals should be used without any non-connected lines.

CN202 socket (LCD module side): IL-Z-9PL-SMTYE (Japan Aviation Electronics Industry Limited (JAE))

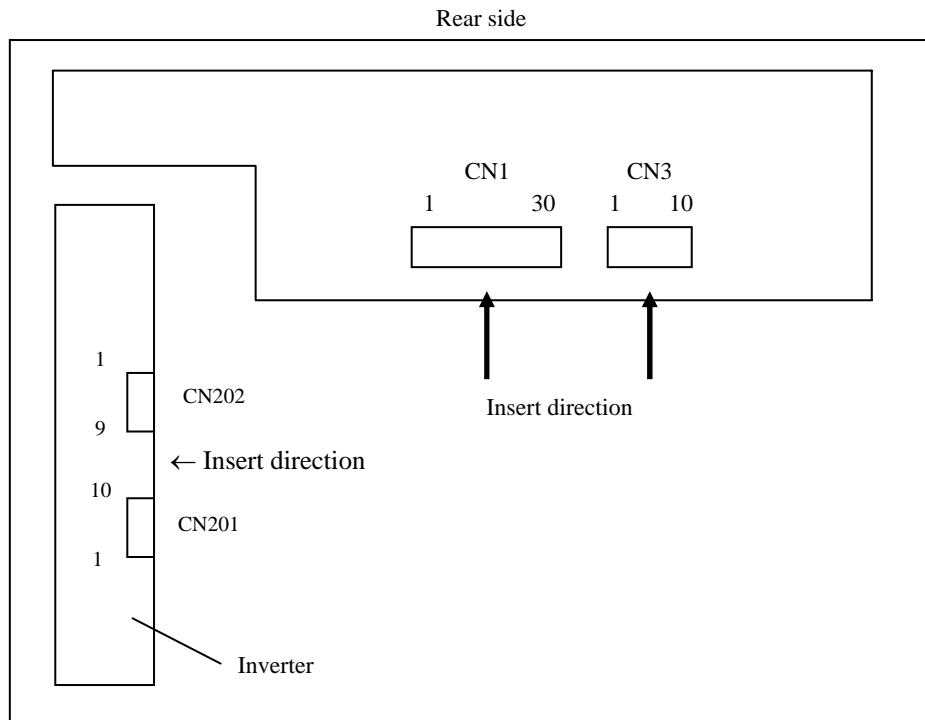
Adaptable plug: IL-Z-9S-S125C3 (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	GNDB	Inverter ground	Note1
2	GNDB		
3	N.C.	-	Keep this pin Open.
4	BRTC	Backlight ON/OFF control signal	High or Open: Backlight ON Low: Backlight OFF
5	BRTH	Luminance control terminal	See "4.6 LUMINANCE CONTROL".
6	BRTI		
7	BRTP		
8	GNDB	Inverter ground	Note1
9	PWSEL	Selection of luminance control signal method	See "4.6 LUMINANCE CONTROL". Note2

Note1: All GNDB terminals should be used without any non-connected lines.

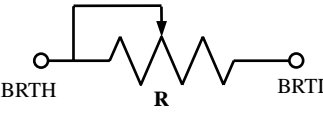
Note2: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

### 4.5.3 Positions of socket



## 4.6 LUMINANCE CONTROL

### 4.6.1 Luminance control methods

Method	Adjustment and luminance ratio	PWSEL terminal	BRTP terminal						
Variable resistor control  Note1	<ul style="list-style-type: none"> <li>• Adjustment</li> </ul> <p>The variable resistor (<b>R</b>) for luminance control should be 10kΩ ±5%, 1/10W. Minimum point of the resistance is the minimum luminance and maximum point of the resistance is the maximum luminance.</p> <p>The resistor (<b>R</b>) must be connected between BRTH-BRTI terminals.</p> <div style="text-align: center;">  </div> <ul style="list-style-type: none"> <li>• Luminance ratio Note3</li> </ul> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Resistance</th> <th>Luminance ratio</th> </tr> </thead> <tbody> <tr> <td>1.5 kΩ Note4</td> <td>20% (Min. Luminance)</td> </tr> <tr> <td>10 kΩ</td> <td>100% (Max. Luminance)</td> </tr> </tbody> </table>	Resistance	Luminance ratio	1.5 kΩ Note4	20% (Min. Luminance)	10 kΩ	100% (Max. Luminance)	High or Open	Open
Resistance	Luminance ratio								
1.5 kΩ Note4	20% (Min. Luminance)								
10 kΩ	100% (Max. Luminance)								
Voltage control  Note1	<ul style="list-style-type: none"> <li>• Adjustment</li> </ul> <p>Voltage control method works, when BRTH terminal is 0V and VBI voltage is input between BRTI-BRTH terminals. This control method can carry out continuation adjustment of luminance.</p> <p>Luminance is the maximum when BRTI terminal is Open.</p> <ul style="list-style-type: none"> <li>• Luminance ratio Note3</li> </ul> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BRTI Voltage (VBI)</th> <th>Luminance ratio</th> </tr> </thead> <tbody> <tr> <td>0.25V Note4</td> <td>20% (Min. Luminance)</td> </tr> <tr> <td>1.0V</td> <td>100% (Max. Luminance)</td> </tr> </tbody> </table>	BRTI Voltage (VBI)	Luminance ratio	0.25V Note4	20% (Min. Luminance)	1.0V	100% (Max. Luminance)		
BRTI Voltage (VBI)	Luminance ratio								
0.25V Note4	20% (Min. Luminance)								
1.0V	100% (Max. Luminance)								
Pulse width modulation  Note1 Note2 Note5	<ul style="list-style-type: none"> <li>• Adjustment</li> </ul> <p>Pulse width modulation (PWM) method works, when PWSEL terminal is Low and PWM signal (BRTP signal) is input into BRTP terminal. The luminance is controlled by duty ratio of BRTP signal.</p> <ul style="list-style-type: none"> <li>• Luminance ratio Note3</li> </ul> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Duty ratio</th> <th>Luminance ratio</th> </tr> </thead> <tbody> <tr> <td>0.2</td> <td>20% (Min. Luminance)</td> </tr> <tr> <td>1.0</td> <td>100% (Max. Luminance)</td> </tr> </tbody> </table>	Duty ratio	Luminance ratio	0.2	20% (Min. Luminance)	1.0	100% (Max. Luminance)	Low	BRTP signal
Duty ratio	Luminance ratio								
0.2	20% (Min. Luminance)								
1.0	100% (Max. Luminance)								

Note1: In case of the variable resistor control method and the voltage control method, noises may appear on the display image depending on the input signals timing for LCD panel signal processing board.

**Use PWM method, if interference noises appear on the display image!**

Note2: The inverter will stop working, if the Low period of BRTP signal is more than 50ms while BRTC signal is High or Open. Then the backlight will not turn on anymore, even if BRTP signal is input again. This is not out of order. The inverter will start to work when power is supplied again.

Note3: These data are the target values.

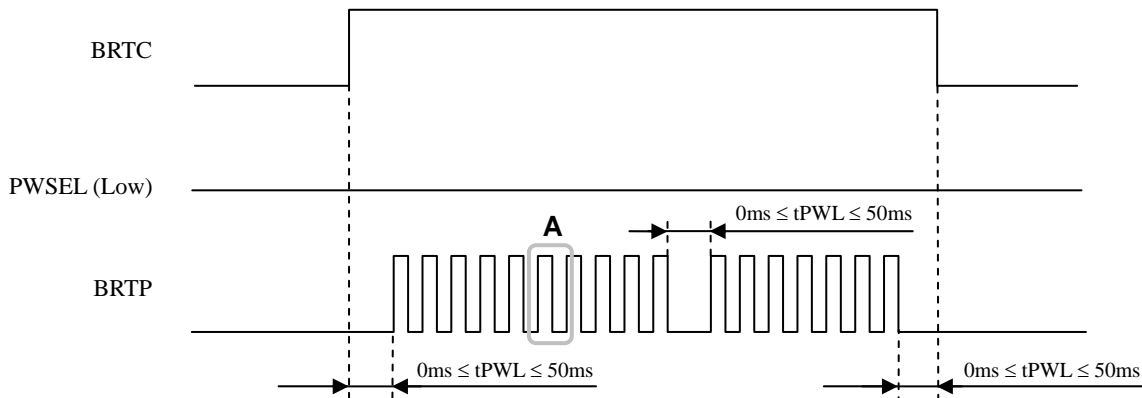
Note4: Do not set the variable resistor and BRTI voltage in less than 1.5kΩ or less than 0.25V. Otherwise flicker or display mura may cause, or the lamp may not be turned on.

Note5: See "4.6.2 Detail of BRTP timing".

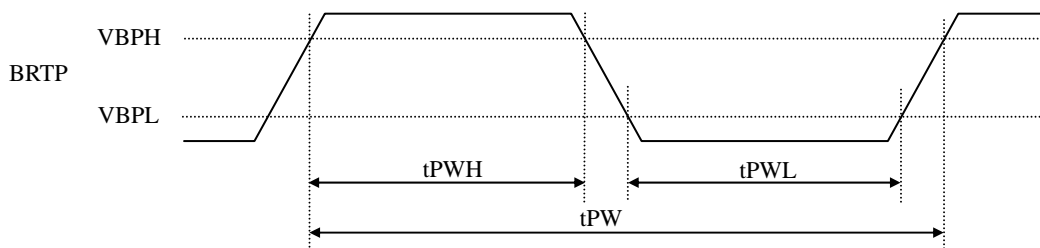
## 4.6.2 Detail of BRTP timing

### (1) Timing diagrams

• Outline chart



• Detail of **A** part



### (2) Each parameter

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Luminance control frequency	FL	185	-	325	Hz	Note1, Note2
Duty ratio	DL	0.2	-	1.0	-	Note1, Note3
Low period	tPWL	0	-	50	ms	Note4

Note1: Definition of parameters is as follows.

$$FL = \frac{1}{tPW} \quad DL = \frac{tPWH}{tPW}$$

Note2: See the following formula for luminance control frequency.

$$\text{Luminance control frequency} = 1/tv \times (n+0.25) \text{ [or } (n + 0.75)]$$

n = 1, 2, 3 . . . . .

tv: Vertical cycle (See "4.9.1 Timing characteristics".)

**The interference noise of luminance control frequency and input signal frequency for LCD panel signal processing board may appear on a display. Set up luminance control frequency so that the interference noise does not appear!**

Note3: See "4.6.1 Luminance control methods".

Note4: If tPWL is more than 50ms, the backlight will be turned off by a protection circuit for inverter. The inverter will start to work when power is supplied again.



# PRELIMINARY

4.7 LVDS DATA INPUT MAP

4.7.1 Mode A

Input data		Note1		Transmitter				CN1		
				Pin	THC63LVDF83A	Pin	THC63LVD823			
Odd pixel data and control signal	LA2	→	51	TA0	53	R12	Note2	Pin	Symbol	
	LA3	→	52	TA1	54	R13		TA1-	1	DA0-
	LA4	→	54	TA2	57	R14	TA1+	2	DA0+	
	LA5	→	55	TA3	58	R15				
	LA6	→	56	TA4	59	R16	TB1-	3	DA1-	
	LA7	→	3	TA5	60	R17	TB1+	4	DA1+	
	CA2	→	4	TA6	63	G12				
	CA3	→	6	TB0	64	G13	TC1-	5	DA2-	
	CA4	→	7	TB1	65	G14	TC1+	6	DA2+	
	CA5	→	11	TB2	66	G15		7	GND	
	CA6	→	12	TB3	67	G16	TCLK1-	8	CKA-	
	CA7	→	14	TB4	68	G17	TCLK1+	9	CKA+	
	RA2	→	15	TB5	73	B12				
	RA3	→	19	TB6	74	B13	TD1-	10	DA3-	
	RA4	→	20	TC0	75	B14	TD1+	11	DA3+	
	RA5	→	22	TC1	76	B15				
	RA6	→	23	TC2	77	B16				
	RA7	→	24	TC3	78	B17				
	Note3	RSVD	→	27	TC4	7	RSVD			
	Note3	RSVD	→	28	TC5	8	RSVD			
		DE	→	30	TC6	9	DE			
		LA0	→	50	TD0	51	R10			
		LA1	→	2	TD1	52	R11			
		CA0	→	8	TD2	61	G10			
		CA1	→	10	TD3	62	G11			
		RA0	→	16	TD4	69	B10			
		RA1	→	18	TD5	70	B11			
	Note3	RSVD	→	25	TD6	-				
		CLK	→	31	CLKIN	10	CLK			
	Even pixel data	LB2	→	51	TA0	81	R22			
		LB3	→	52	TA1	82	R23	TA2-	12	DB0-
LB4		→	54	TA2	83	R24	TA2+	13	DB0+	
LB5		→	55	TA3	84	R25		14	GND	
LB6		→	56	TA4	85	R26	TB2-	15	DB1-	
LB7		→	3	TA5	86	R27	TB2+	16	DB1+	
CB2		→	4	TA6	91	G22		17	GND	
CB3		→	6	TB0	92	G23	TC2-	18	DB2-	
CB4		→	7	TB1	93	G24	TC2+	19	DB2+	
CB5		→	11	TB2	94	G25				
CB6		→	12	TB3	95	G26	TCLK2-	20	CKB-	
CB7		→	14	TB4	96	G27	TCLK2+	21	CKB+	
RB2		→	15	TB5	99	B22				
RB3		→	19	TB6	100	B23	TD2-	22	DB3-	
RB4		→	20	TC0	1	B24	TD2+	23	DB3+	
RB5		→	22	TC1	2	B25		24	GND	
RB6		→	23	TC2	5	B26		25	TxSEL0	
RB7		→	24	TC3	6	B27		26	TxSEL1	
Note3		RSVD	→	27	TC4	-		27	GND	
Note3		RSVD	→	28	TC5	-		28	VDD	
Note3		RSVD	→	30	TC6	-		29	VDD	
		LB0	→	50	TD0	79	R20		30	VDD
		LB1	→	2	TD1	80	R21			
		CB0	→	8	TD2	89	G20			
		CB1	→	10	TD3	90	G21			
		RB0	→	16	TD4	97	B20			
		RB1	→	18	TD5	98	B21			
Note3		RSVD	→	25	TD6	-				
		CLK	→	31	CLKIN	-				

# PRELIMINARY

4.7.2 Mode B

Input data		Transmitter		CN1					
		Pin	DS90CF383, C385						
Odd pixel data and control signal	Note1	LA7	→ 51 TXIN0	1st	Note2	Pin	Symbol		
		LA6	→ 52 TXIN1		TA1-	→ 1	DA0-		
		LA5	→ 54 TXIN2		TA1+	→ 2	DA0+		
		LA4	→ 55 TXIN3						
		LA3	→ 56 TXIN4		TB1-	→ 3	DA1-		
		LA2	→ 3 TXIN6		TB1+	→ 4	DA1+		
		CA7	→ 4 TXIN7						
		CA6	→ 6 TXIN8		TC1-	→ 5	DA2-		
		CA5	→ 7 TXIN9		TC1+	→ 6	DA2+		
		CA4	→ 11 TXIN12						
		CA3	→ 12 TXIN13		TCLK1-	→ 8	CKA-		
		CA2	→ 14 TXIN14		TCLK1+	→ 9	CKA+		
		RA7	→ 15 TXIN15						
		RA6	→ 19 TXIN18		TD1-	→ 10	DA3-		
		RA5	→ 20 TXIN19		TD1+	→ 11	DA3+		
		RA4	→ 22 TXIN20						
		RA3	→ 23 TXIN21						
		RA2	→ 24 TXIN22						
		Note3	RSVD		→ 27 TXIN24				
		Note3	RSVD		→ 28 TXIN25				
			DE		→ 30 TXIN26				
			LA1		→ 50 TXIN27				
			LA0		→ 2 TXIN5				
			CA1		→ 8 TXIN10				
			CA0		→ 10 TXIN11				
			RA1		→ 16 TXIN16				
			RA0		→ 18 TXIN17				
		Note3	RSVD		→ 25 TXIN23				
			CLK		→ 31 CLKIN				
	Even pixel data		LB7		→ 51 TXIN0	2nd			
			LB6		→ 52 TXIN1		TA2-	→ 12	DB0-
		LB5	→ 54 TXIN2	TA2+	→ 13		DB0+		
		LB4	→ 55 TXIN3						
		LB3	→ 56 TXIN4	TB2-	→ 15		DB1-		
		LB2	→ 3 TXIN6	TB2+	→ 16		DB1+		
		CB7	→ 4 TXIN7						
		CB6	→ 6 TXIN8	TC2-	→ 18		DB2-		
		CB5	→ 7 TXIN9	TC2+	→ 19		DB2+		
		CB4	→ 11 TXIN12						
		CB3	→ 12 TXIN13	TCLK2-	→ 20		CKB-		
		CB2	→ 14 TXIN14	TCLK2+	→ 21		CKB+		
		RB7	→ 15 TXIN15						
		RB6	→ 19 TXIN18	TD2-	→ 22		DB3-		
		RB5	→ 20 TXIN19	TD2+	→ 23		DB3+		
		RB4	→ 22 TXIN20						
		RB3	→ 23 TXIN21						
		RB2	→ 24 TXIN22						
		Note3	RSVD	→ 27 TXIN24					
		Note3	RSVD	→ 28 TXIN25					
		Note3	RSVD	→ 30 TXIN26					
			LB1	→ 50 TXIN27					
			LB0	→ 2 TXIN5					
			CB1	→ 8 TXIN10					
			CB0	→ 10 TXIN11					
			RB1	→ 16 TXIN16					
			RB0	→ 18 TXIN17					
		Note3	RSVD	→ 25 TXIN23					
			CLK	→ 31 CLKIN					

# PRELIMINARY

4.7.3 Mode C

Input data		Transmitter		CN1				
		Pin	DS90CF383, C385					
Odd pixel data and control signal	Note1 LA0	→	51 TXIN0	Note2	TA1- →	1 DA0-		
	LA1	→	52 TXIN1		TA1+ →	2 DA0+		
	LA2	→	54 TXIN2					
	LA3	→	55 TXIN3					
	LA4	→	56 TXIN4		TB1- →	3 DA1-		
	LA5	→	3 TXIN6		TB1+ →	4 DA1+		
	CA0	→	4 TXIN7					
	CA1	→	6 TXIN8		TC1- →	5 DA2-		
	CA2	→	7 TXIN9		TC1+ →	6 DA2+		
	CA3	→	11 TXIN12			7 GND		
	CA4	→	12 TXIN13		TCLK1- →	8 CKA-		
	CA5	→	14 TXIN14		TCLK1+ →	9 CKA+		
	RA0	→	15 TXIN15					
	RA1	→	19 TXIN18		TD1- →	10 DA3-		
	RA2	→	20 TXIN19 1st		TD1+ →	11 DA3+		
	RA3	→	22 TXIN20					
	RA4	→	23 TXIN21					
	RA5	→	24 TXIN22					
	Note3 RSVD	→	27 TXIN24					
	Note3 RSVD	→	28 TXIN25					
	DE	→	30 TXIN26					
	LA6	→	50 TXIN27					
	LA7	→	2 TXIN5					
	CA6	→	8 TXIN10					
	CA7	→	10 TXIN11					
	RA6	→	16 TXIN16					
	RA7	→	18 TXIN17					
	Note3 RSVD	→	25 TXIN23					
	CLK	→	31 CLKIN					
	Even pixel data	LB0	→		51 TXIN0	Note2	TA2- →	12 DB0-
		LB1	→		52 TXIN1		TA2+ →	13 DB0+
LB2		→	54 TXIN2		14 GND			
LB3		→	55 TXIN3					
LB4		→	56 TXIN4	TB2- →	15 DB1-			
LB5		→	3 TXIN6	TB2+ →	16 DB1+			
CB0		→	4 TXIN7		17 GND			
CB1		→	6 TXIN8	TC2- →	18 DB2-			
CB2		→	7 TXIN9	TC2+ →	19 DB2+			
CB3		→	11 TXIN12					
CB4		→	12 TXIN13	TCLK2- →	20 CKB-			
CB5		→	14 TXIN14	TCLK2+ →	21 CKB+			
RB0		→	15 TXIN15					
RB1		→	19 TXIN18	TD2- →	22 DB3-			
RB2		→	20 TXIN19 2nd	TD2+ →	23 DB3+			
RB3		→	22 TXIN20		24 GND			
RB4		→	23 TXIN21		25 TxSEL0			
RB5		→	24 TXIN22		26 TxSEL1			
Note3 RSVD		→	27 TXIN24		27 GND			
Note3 RSVD		→	28 TXIN25		28 VDD			
Note3 RSVD		→	30 TXIN26		29 VDD			
LB6		→	50 TXIN27		30 VDD			
LB7		→	2 TXIN5					
CB6		→	8 TXIN10					
CB7		→	10 TXIN11					
RB6		→	16 TXIN16					
RB7		→	18 TXIN17					
Note3 RSVD		→	25 TXIN23					
CLK		→	31 CLKIN					

# PRELIMINARY

Note1: LSB (Least Significant Bit) – LA0, CA0, RA0, LB0, CB0, RB0  
 MSB (Most Significant Bit) – LA7, CA7, RA7, LB7, CB7, RB7

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

Note3: Input signal RSVD is not used inside the product, but do not keep pin open to avoid noise problem.

## 4.8 DISPLAY GRAYSCALE AND INPUT DATA SIGNALS

This product can display 256 gray scales in each LCR sub-pixel and 766 gray scales per 1 pixel. Also the relation between display gray scale and input data signals is as the following table.

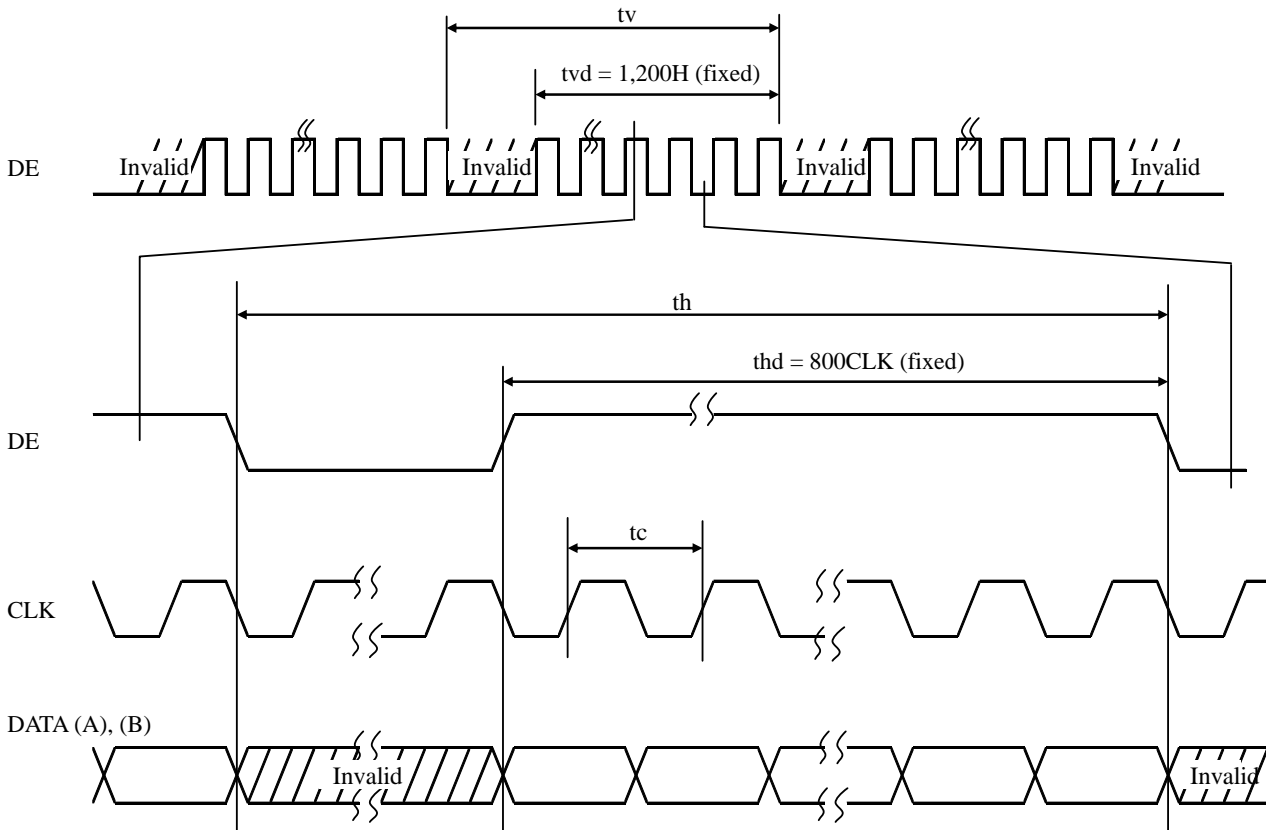
Display grayscale		Data signal (0: Low level, 1: High level)																							
		LA7 LA6 LA5 LA4 LA3 LA2 LA1 LA0								CA7 CA6 CA5 CA4 CA3 CA2 CA1 CA0								RA7 RA6 RA5 RA4 RA3 RA2 RA1 RA0							
		LB7 LB6 LB5 LB4 LB3 LB2 LB1 LB0	CB7 CB6 CB5 CB4 CB3 CB2 CB1 CB0	RB7 RB6 RB5 RB4 RB3 RB2 RB1 RB0																					
Left sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑					:							:								:				
	↓					:							:								:				
bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
White	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Center sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑					:							:								:				
	↓					:							:								:				
bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	
White	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Right sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑					:							:								:				
	↓					:							:								:				
bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	
White	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

## 4.9 INPUT SIGNAL TIMINGS

### 4.9.1 Timing characteristics

Parameter	Symbol	min.	typ.	max.	Unit	Remarks		
CLK	Frequency	1/ tc	60.0	64.5	65.0	MHz	LVDS transmitter input	
	Pulse width	tc	15.38	15.5	-	ns		
	Duty	-	See the data sheet of LVDS transmitter.			-		-
	Rise, fall	-				ns		
Horizontal	Cycle	th	13.1	13.3	19.2	μs	-	
			848	860	1,156	CLK		
	Display period	thd	800			CLK	-	
Vertical	Cycle	1/tv	59	60	61	Hz	-	
		tv	1,206	1,250	-	H		
	Display period	tvd	1,200			H	-	
DE, DATA	Setup time	-	See the data sheet of LVDS transmitter.			ns	-	
	Hold time	-				ns		
	Rise, fall	-				ns		

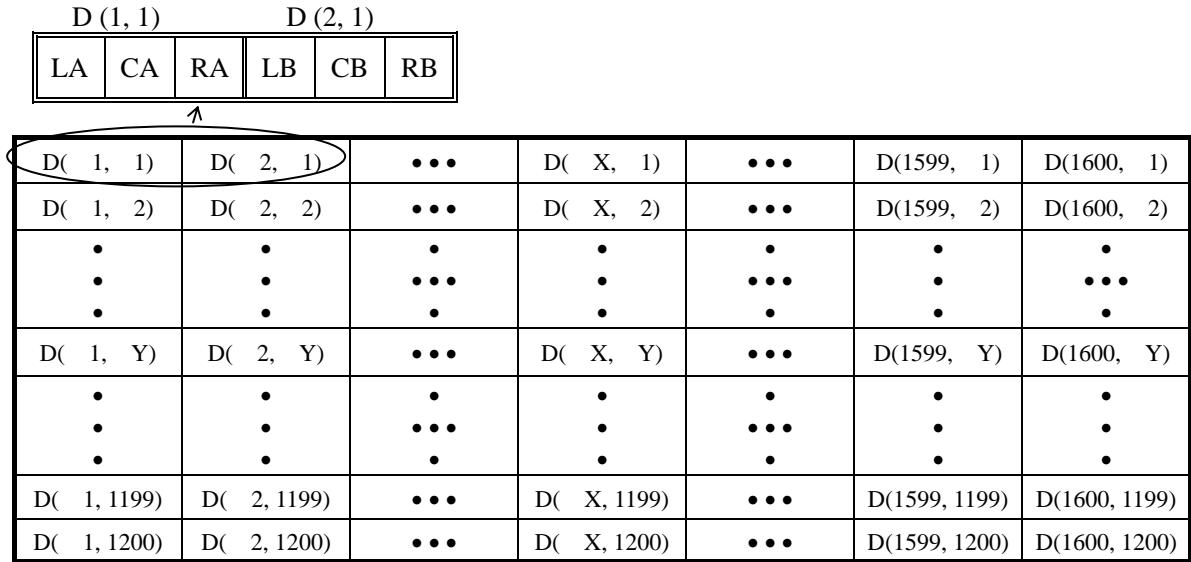
### 4.9.2 Input signal timing chart



# PRELIMINARY

## 4.10 DISPLAY POSITIONS

Odd pixel:    LA= Left data            Even pixel:    LB= Left data  
                  CA= Center data                           CB= Center data  
                  RA= Right data                            RB= Right data



## 4.11 TEN-bit LOOK UP TABLE FOR GAMMA ADJUSTMENT

Adjustment of gamma characteristics for each 8-bit LCR data is possible by using built-in 10-bit LUT (look up table) for Gamma characteristics.

The LUT is set with the serial data. The combination of the control command determines the R/W actions.: READ, Random/Sequential Address WRITE and Individual/Simultaneous LCR setting.

The serial data is composed as Table1.

Table1: Serial data Composition

DATA	DATA name	Function	Remarks
D31	CMD5	Control Command	See Table2 and 3.
D30	CMD4	Control Command	
D29	CMD3	Control Command	
D28	CMD2	Control Command	
D27	CMD1	Control Command	
D26	CMD0	Control Command	
D25	ADD9	LUT Address (MSB)	See Table4.
D24	ADD8	LUT Address	
D23	ADD7	LUT Address	
D22	ADD6	LUT Address	
D21	ADD5	LUT Address	
D20	ADD4	LUT Address	
D19	ADD3	LUT Address	
D18	ADD2	LUT Address	
D17	ADD1	LUT Address	
D16	ADD0	LUT Address (LSB)	See Table5.
D15	Dummy	Dummy Data "0"	
D14	Dummy	Dummy Data "0"	
D13	Dummy	Dummy Data "0"	
D12	Dummy	Dummy Data "0"	
D11	Dummy	Dummy Data "0"	
D10	Dummy	Dummy Data "0"	
D9	DATA9	LUT Data (MSB)	
D8	DATA8	LUT Data	
D7	DATA7	LUT Data	
D6	DATA6	LUT Data	
D5	DATA5	LUT Data	
D4	DATA4	LUT Data	
D3	DATA3	LUT Data	
D2	DATA2	LUT Data	
D1	DATA1	LUT Data	
D0	DATA0	LUT Data (LSB)	

# PRELIMINARY

Table2: Command table (CMD5 to CMD0: 6-bit)

DATA name	Parameter	Remarks
CMD5	Selection of WRITE/READ mode "1": WRITE mode "0": READ mode	In case of "0", must be set as follows. CMD4: "1", CMD3: "0", CMD2: "1" CMD1: "0", CMD0: "0"
CMD4	Must be set to "1".	-
CMD3	Selection of Random/Sequential Address WRITE "1": Random Address WRITE "0": Sequential Address WRITE	-
CMD2	Must be set to "1".	-
CMD1	Selection of Individual/Simultaneous LCR setting "1": Individual LCR setting "0": Simultaneous LCR setting	"1": Select the sub-pixel by using ADD9 and ADD8. (See Table4.) "0": ADD9 and ADD8 are invalid.
CMD0	Must be set to "0".	-

Table3: Command Combination table (CMD5 to CMD0: 6-bit)

CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	Mode
1	1	1	1	1	0	Random Address WRITE, Individual LCR setting
1	1	1	1	0	0	Random Address WRITE, Simultaneous LCR setting
1	1	0	1	1	0	Sequential Address WRITE, Individual LCR setting
1	1	0	1	0	0	Sequential Address WRITE, Simultaneous LCR setting
0	1	0	1	0	0	READ mode

\*Other combinations are prohibited, and may cause function error.

Table4: Address table (ADD9 to ADD0: 10-bit)

DATA name	Parameter	Remarks
ADD9	Sub-pixel selection ADD[9:8]= 0:0 Left sub-pixel 0:1 Center sub-pixel 1:0 Right sub-pixel 1:1 ON/OFF selection of Gamma Correction	When "ADD[9:8]=1:1", ON/OFF of Gamma correction can select according to the GMA[2:0]. (See Table6 and Table7.)
ADD8		
ADD7		
ADD6		
ADD5	LUT Address 256 address = 00h - FFh	When ADD[9:8] = 1:1, ADD[7:0] must be set to 00h.
ADD4		
ADD3		
ADD2		
ADD1		
ADD0		



# PRELIMINARY

Table5: Data table (DATA15 to DATA0: 16-bit)

DATA	DATA name	Parameter	Remarks
DATA15	Dummy	Dummy Data Must be set to "0".	-
DATA14	Dummy		
DATA13	Dummy		
DATA12	Dummy		
DATA11	Dummy		
DATA10	Dummy		
DATA9	DATA9	[MSB]	-
DATA8	DATA8	10-bit LUT Data 000h - 3FFh	
DATA7	DATA7		
DATA6	DATA6		
DATA5	DATA5		
DATA4	DATA4		
DATA3	DATA3		
DATA2	DATA2		
DATA1	DATA1		
DATA0	DATA0	[LSB]	

Table6: Gamma correction table (DATA15 to DATA0: 16bit)

DATA	DATA name	Parameter	Remarks
DATA15	Dummy	Dummy Data Must be set to "0".	-
DATA14	Dummy		
DATA13	Dummy		
DATA12	Dummy		
DATA11	Dummy		
DATA10	Dummy		
DATA9	Dummy		
DATA8	Dummy		
DATA7	Dummy		
DATA6	Dummy		
DATA5	Dummy		
DATA4	Dummy		
DATA3	Dummy	[MSB] GMA Data [LSB]	See Table7.
DATA2	GMA2		
DATA1	GMA1		
DATA0	GMA0		

Table7: Control code GMA[2:0]

GMA2	GMA1	GMA0	Function
0	0	0	No correction (Initial setting)
0	0	1	Correction according to the LUT Data. <span style="float: right;">Note1</span>

\*Other combinations are prohibited, and may cause function error.

Note1: Initial setting of the LUT is undefined data. The LUT should be enabled by setting of the GMA after writing the LUT data in all the 256 addresses, in order to avoid undefined data display.

Note2: Transfer the data every power-on, because the LUT data isn't stored in the LCD module.

Note3: As writing and reading the LUT data, a noise may appear on the display image. In order to prevent the noise appearing on the display, following measures should be performed.

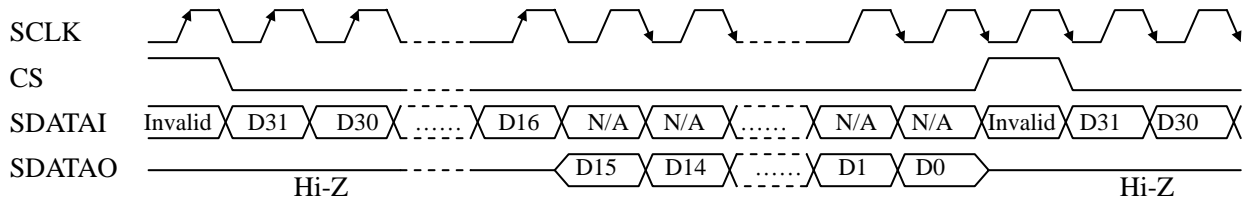
(1)The LUT data should be rewritten during invalid period of pixel data (See "**4.9 INPUT SIGNAL TIMINGS**").).

(2) The LUT data should be rewritten when the Gamma Correction is OFF (GMA[2:0] = 000).

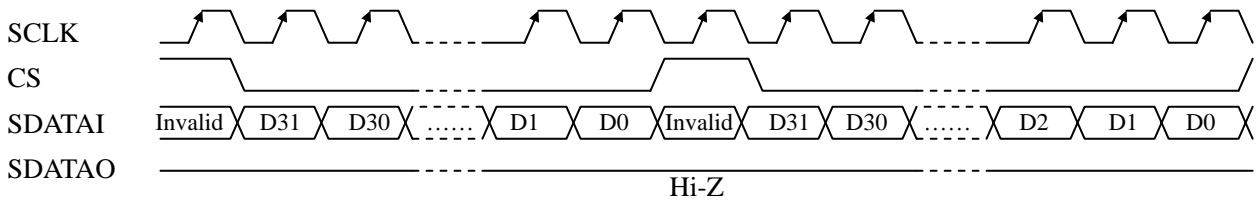
## 4.12 LUT SERIAL COMMUNICATION TIMINGS

### 4.12.1 Timing Chart

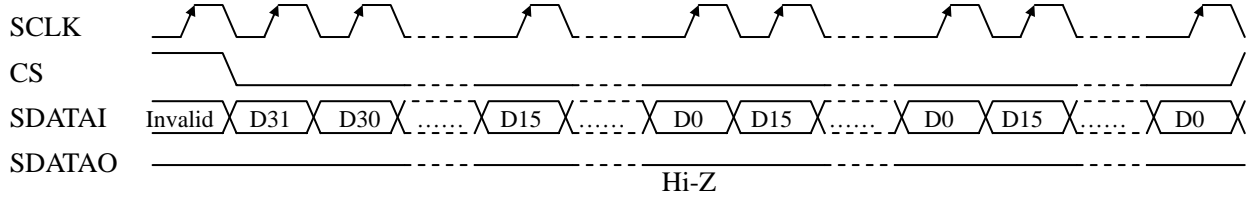
#### (1) READ Timing Chart



#### (2) Random Address WRITE Timing Chart



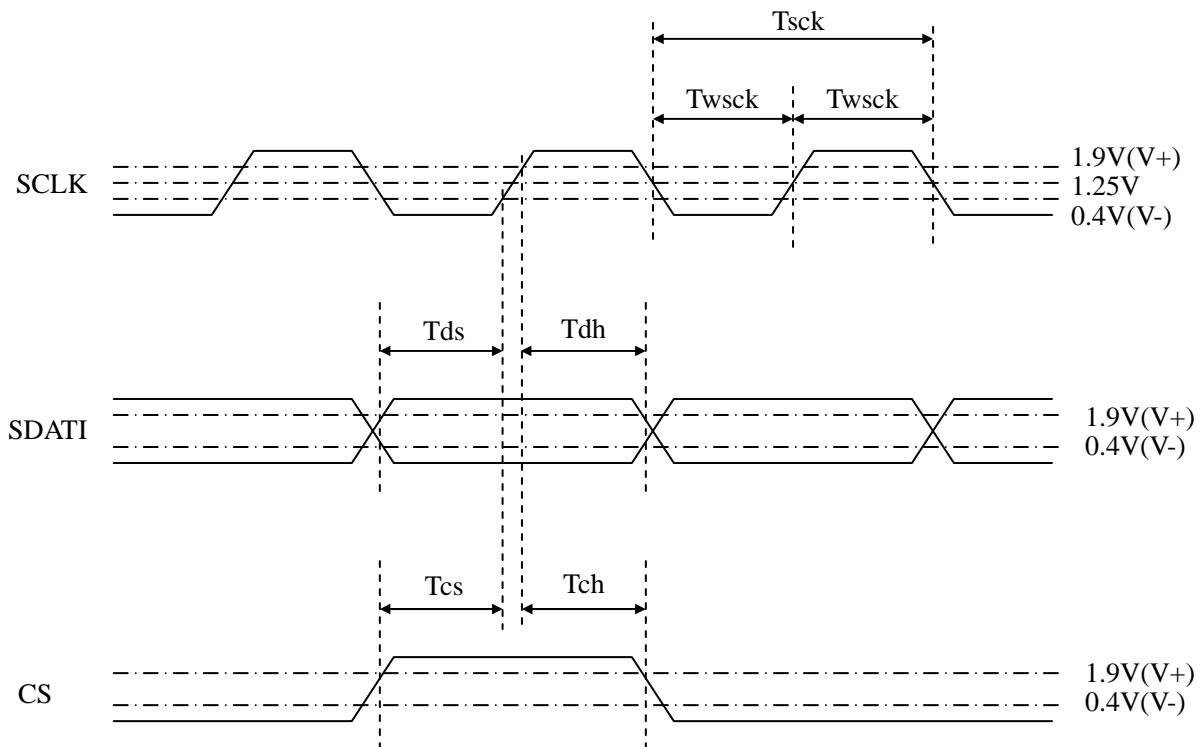
#### (3) Sequential Address WRITE Timing Chart



4.12.2 Timing specifications

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
SCLK Frequency	1/Tsck	-	-	5	MHz	-
SCLK Pulse Width (WRITE)	Twsck	50	-	-	ns	-
SCLK Pulse Width (READ)	Twsck	5	-	-	tc	Note1
SDATI-SCLK Setup Time	Tds	50	-	-	ns	-
SDATI-SCLK Hold Time	Tdh	50	-	-	ns	-
CS-SCLK Setup Time	Tcs	50	-	-	ns	-
CS-SCLK Hold Time	Tch	50	-	-	ns	-

Note1: At the READ of the serial communication mode, the SCLK Pulse Width (Twsck) must be greater than 5CLK (5 tc's). (See "4.9.1 Timing characteristics".)



Note2: During the serial communication mode, the display noise may appear because of rewriting the data. To avoid this, rewrite the LUT data when the pixel data is invalid or the Gamma Correction is OFF (GMA[2:0] = 000). The external noise may cause the data change, refresh the data regularly according to need.

# PRELIMINARY

## 4.13 OPTICS

### 4.13.1 Optical characteristics

(Note1, Note2)

Parameter	Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks	
Luminance	White at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	L	1,200	1,800	-	cd/m <sup>2</sup>	BM-5A or SR-3	-	
Contrast ratio	White/Black at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	CR	600	900	-	-	BM-5A or SR-3	Note3	
Luminance uniformity	White $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	LU	-	1.15	1.25	-	BM-5A	Note4	
Chromaticity	White	x coordinate	Wx	0.269	0.299	0.329	-	SR-3	Note5
		y coordinate	Wy	0.285	0.315	0.345	-		
Response time	Black to White	Ton	-	22	32	ms	BM-5A	Note6 Note7	
	White to Black	Toff	-	23	33	ms			
Viewing angle	Right	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	$\theta R$	70	85	-	BM-5A	Note8	
	Left	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	$\theta L$	70	85	-			
	Up	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	$\theta U$	70	85	-			
	Down	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	$\theta D$	70	85	-			

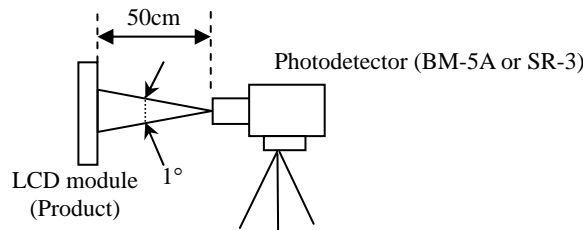
Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.

Ta = 25°C, VDD = 12.0V, VDDB = 12.0V, Luminance control = maximum,

Display mode: UXGA, Horizontal cycle = 1/75.19 kHz, Vertical cycle = 1/60.0Hz

Optical characteristics are measured after 20 minutes from working the product, in the dark room. Also measurement methods are as follows.



Note3: See "4.13.2 Definition of contrast ratio".

Note4: See "4.13.3 Definition of luminance uniformity".

Note5: These coordinates are found on CIE 1931 chromaticity diagram.

Note6: Product surface temperature: TopF = 36°C

Note7: See "4.13.4 Definition of response times".

Note8: See "4.13.5 Definition of viewing angles".

#### 4.13.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

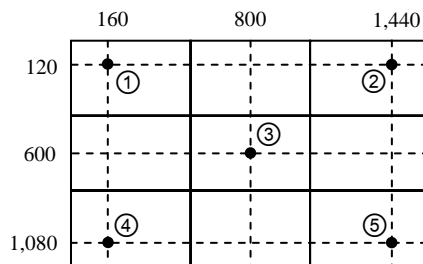
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

#### 4.13.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

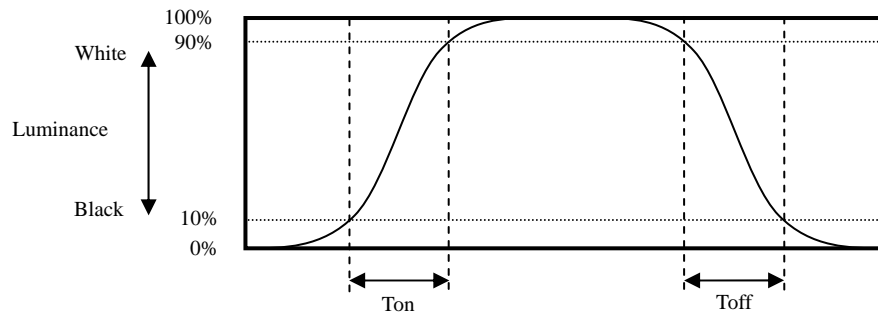
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

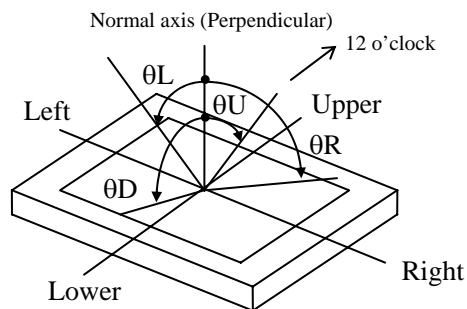


#### 4.13.4 Definition of response times

Response time is measured, the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



#### 4.13.5 Definition of viewing angles



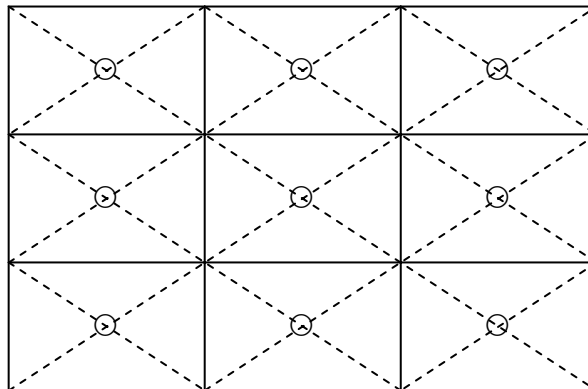
# PRELIMINARY

## 5. RELIABILITY TESTS

Test item	Condition	Judgment Note1
High temperature and humidity (Operation)	① $60 \pm 2^{\circ}\text{C}$ , RH = 60%, 240hours ② Display data is white.	No display malfunctions
Heat cycle (Operation)	① $0 \pm 3^{\circ}\text{C}$ ...1hour $55 \pm 3^{\circ}\text{C}$ ...1hour ② 50cycles, 4hours/cycle ③ Display data is white.	
Thermal shock (Non operation)	① $-20 \pm 3^{\circ}\text{C}$ ...30minutes $60 \pm 3^{\circ}\text{C}$ ...30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
Vibration (Non operation)	① 5 to 100Hz, $11.76\text{m/s}^2$ ② 1 minute/cycle ③ X, Y, Z direction ④ 10 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)	① $294\text{m/s}^2$ , 11ms ② X, Y, Z direction ③ 3 times each directions	
ESD (Operation)	① 150pF, $150\Omega$ , $\pm 10\text{kV}$ ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	No display malfunctions
Dust (Operation)	① Sample dust: No.15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	
Low pressure	Non-operation	No display malfunctions
	Operation	
	① 15 kPa (Equivalent to altitude 13,600m) ② $-20^{\circ}\text{C} \pm 3^{\circ}\text{C}$ ...24 hours ③ $+60^{\circ}\text{C} \pm 3^{\circ}\text{C}$ ...24 hours	
	① 53.3 kPa (Equivalent to altitude 4,850m) ② $0^{\circ}\text{C} \pm 3^{\circ}\text{C}$ ...24 hours ③ $+55^{\circ}\text{C} \pm 3^{\circ}\text{C}$ ...24 hours	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.




Note2: See the following figure for discharge points



## 6. PRECAUTIONS


### 6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding these contents!**

	This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.
	This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.
	This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

### 6.2 CAUTIONS

 **\* Do not touch the working backlight and inverter. There is a danger of an electric shock.**

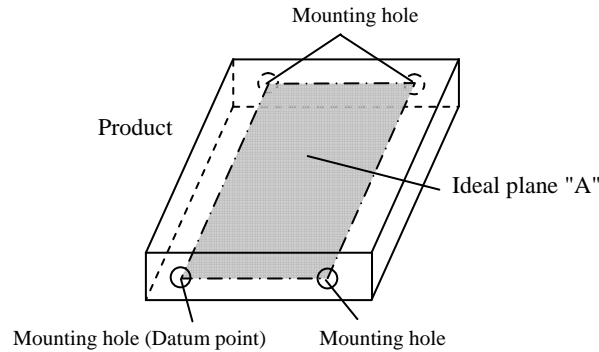
 **\* Do not touch the working backlight and inverter. There is a danger of burn injury.**  
**\* Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s<sup>2</sup> and to be not greater 11ms, Pressure: To be not greater 19.6N (φ16mm jig))**

### 6.3 ATTENTIONS

#### 6.3.1 Handling of the product

- ① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
- ② Do not hook nor pull cables such as lamp cable, and so on, in order to avoid any damage.
- ③ When the product is put on the table temporarily, display surface must be placed downward.
- ④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
- ⑤ The torque for product mounting screws must never exceed 0.735 N·m. Higher torque might result in distortion of the bezel. And the length of product mounting screws must be ≤ 4.7mm.

- ⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura.  
Recommended installing method: Ideal plane "A" is defined by one mounting hole (datum point) and other mounting holes. The ideal plane "A" should be the same plane within  $\pm 0.3$  mm.



- ⑦ Do not press or rub on the sensitive product surface. When cleaning the product surface, use of the cloth with ethanolic liquid such as screen cleaner for LCD is recommended.
- ⑧ Do not push nor pull the interface connectors while the product is working.
- ⑨ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.

### 6.3.2 Environment

- ① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
- ② In order to prevent dew condensation occurring by temperature difference, the product packing box should be opened after enough time being left under the environment of an unpacking room. Evaluate the leaving time sufficiently because a situation of dew condensation occurring is changed by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with packing state)
- ③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
- ④ This product is not designed as radiation hardened.

### 6.3.3 Characteristics

**The following items are neither defects nor failures.**

- ① Response time, luminance and color may be changed by ambient temperature.
- ② Display mura, flicker, vertical seam or small spot may be observed depending on display patterns.
- ③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
- ④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.

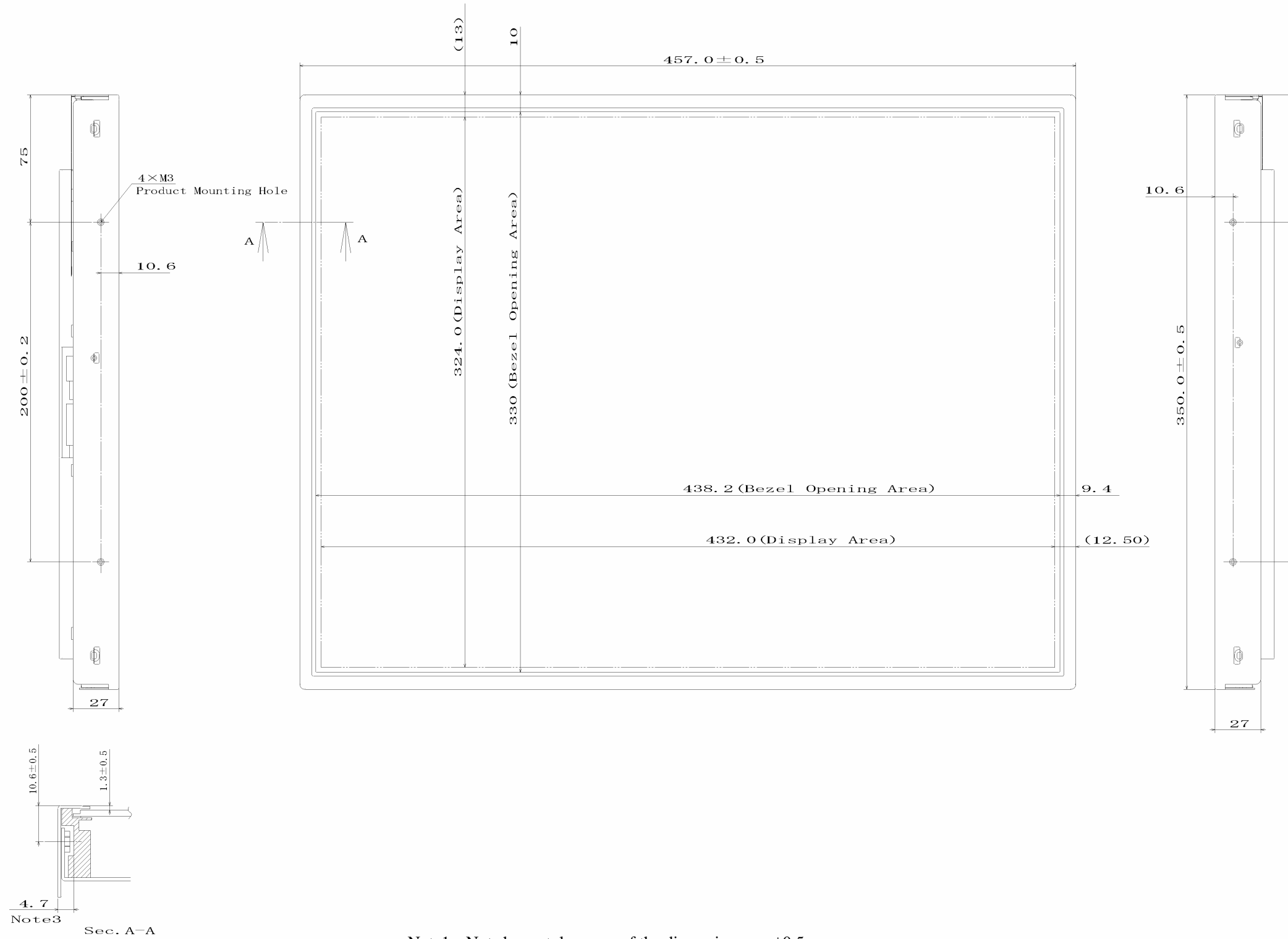


- ⑤ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
- ⑥ Optical characteristics may be changed depending on input signal timings.
- ⑦ The interference noise between input signal frequency for this product's signal processing board and luminance control frequency of the inverter may appear on a display. Set up luminance control frequency of the inverter so that the interference noise does not appear.

#### 6.3.4 Other

- ① All VDD, VDDB, GND and GNDB terminals should be used without any non-connected lines.
- ② Do not disassemble a product or adjust variable resistors.
- ③ See “REPLACEMENT MANUAL FOR INVERTER”, when replacing the inverter.
- ④ Pack the product with original shipping package, in order to avoid any damages during transportation, when returning the product to NEC for repair and so on.
- ⑤ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.

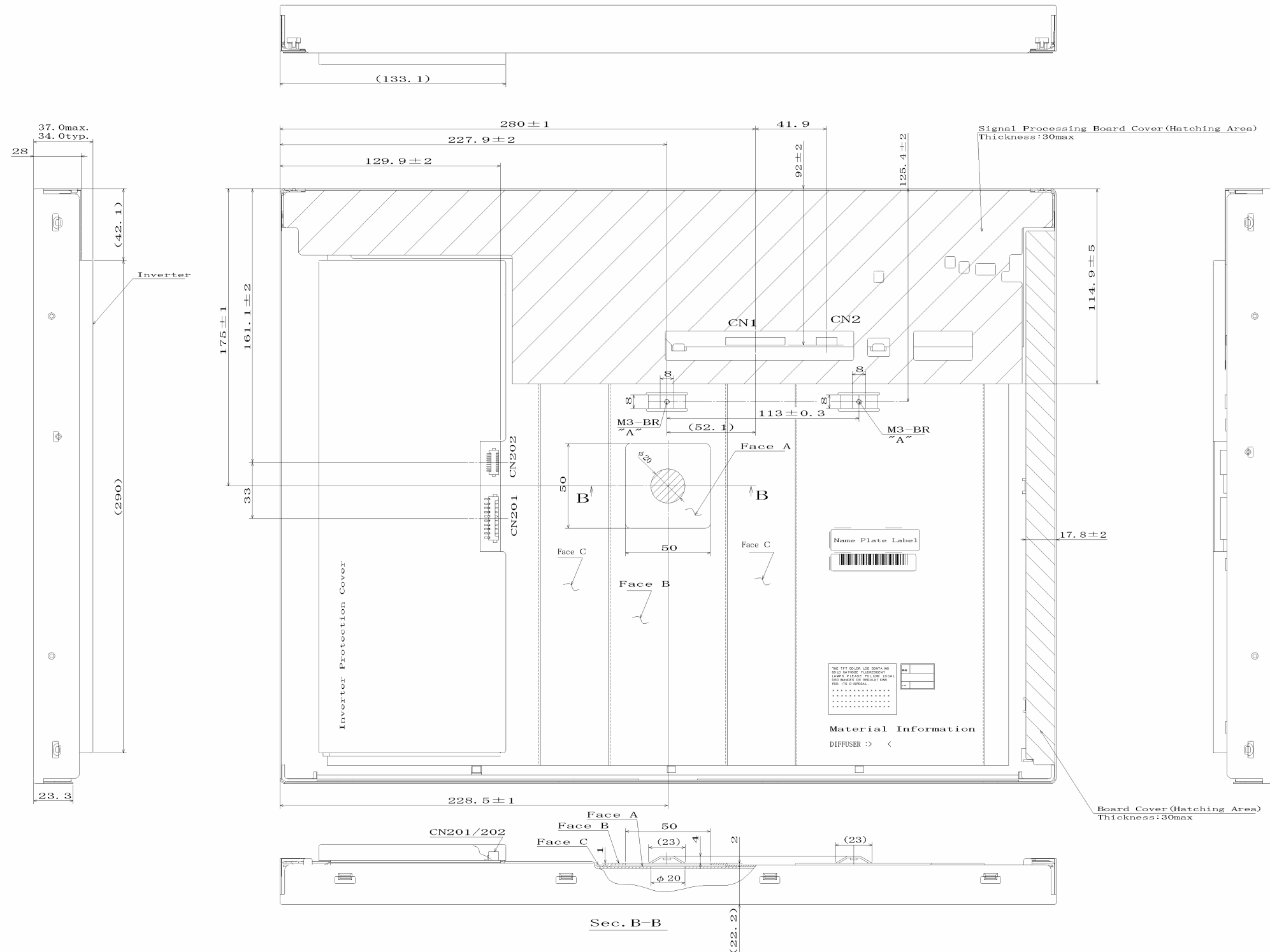
7. OUTLINE DRAWINGS  
7.1 FRONT VIEW



- Note1: Not shown tolerances of the dimensions are  $\pm 0.5$  mm.
- Note2: The torque for product mounting screws must never exceed  $0.735$  N·m.
- Note3: The length of product mounting screws from surface of plate must be  $\leq 4.7$  mm.
- Note4: The values in parentheses are for reference.

Unit: mm

7.2 REAR VIEW












- Note1: Not shown tolerances of the dimensions are  $\pm 0.5\text{mm}$ .
- Note2: The torque for product mounting screws must never exceed  $0.735\text{N}\cdot\text{m}$ .
- Note3: The values in parentheses are for reference.
- Note4: The torque for the holes "A" must never exceed  $0.44\text{N}\cdot\text{m}$ .

Unit: mm

# PRELIMINARY

## REVISION HISTORY

*The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.*

Edition	Document number	Prepared date	Revision contents and signature									
1st edition	DOD-PD-1308	Jan. 31, 2006	<p><b>Revision contents</b></p> <p>New issue</p> <p><b>Signature of writer</b></p> <table data-bbox="555 719 1442 853"><tr><td data-bbox="555 719 826 748"><i>Approved by</i></td><td data-bbox="852 719 1123 748"><i>Checked by</i></td><td data-bbox="1171 719 1442 748"><i>Prepared by</i></td></tr><tr><td data-bbox="555 757 826 808"></td><td data-bbox="852 757 1123 808"></td><td data-bbox="1171 757 1442 808"></td></tr><tr><td data-bbox="555 817 826 853">TOSHIHIDE ITO</td><td data-bbox="852 817 1123 853">R. KAWASHIMA</td><td data-bbox="1171 817 1442 853">N. KANO</td></tr></table>	<i>Approved by</i>	<i>Checked by</i>	<i>Prepared by</i>				TOSHIHIDE ITO	R. KAWASHIMA	N. KANO
<i>Approved by</i>	<i>Checked by</i>	<i>Prepared by</i>										
												
TOSHIHIDE ITO	R. KAWASHIMA	N. KANO										