NLT Technologies, Ltd.

TFT MONOCHROME LCD MODULE

NL160120AM27-33A

54 cm (21.3 Type)
UXGA
LVDS Interface (2 port)

DATA SHEET

DOD-PP-1540 (1st edition)

This DATA SHEET is updated document from PRELIMINARY DATA SHEET DOD-PP-1264(1).

All information is subject to change without notice. Please confirm the sales representative before starting to design your system.

INTRODUCTION

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Examples: Computers, office automation equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment, industrial robots, etc.

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Examples: Military systems, aircraft control equipment, aerospace equipment, nuclear reactor control systems, medical equipment/devices/systems for life support, etc.

The quality grade of this product is the **"Standard"** unless otherwise specified in this document.

CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Monochrome LCD module NL160120AC27-33A is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a monochrome-filter glass substrate.

Grayscale data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Monochrome images are created by regulating the amount of transmitted light through the TFT array .

1.2 APPLICATION

- Monochrome monitor system

1.3 FEATURES

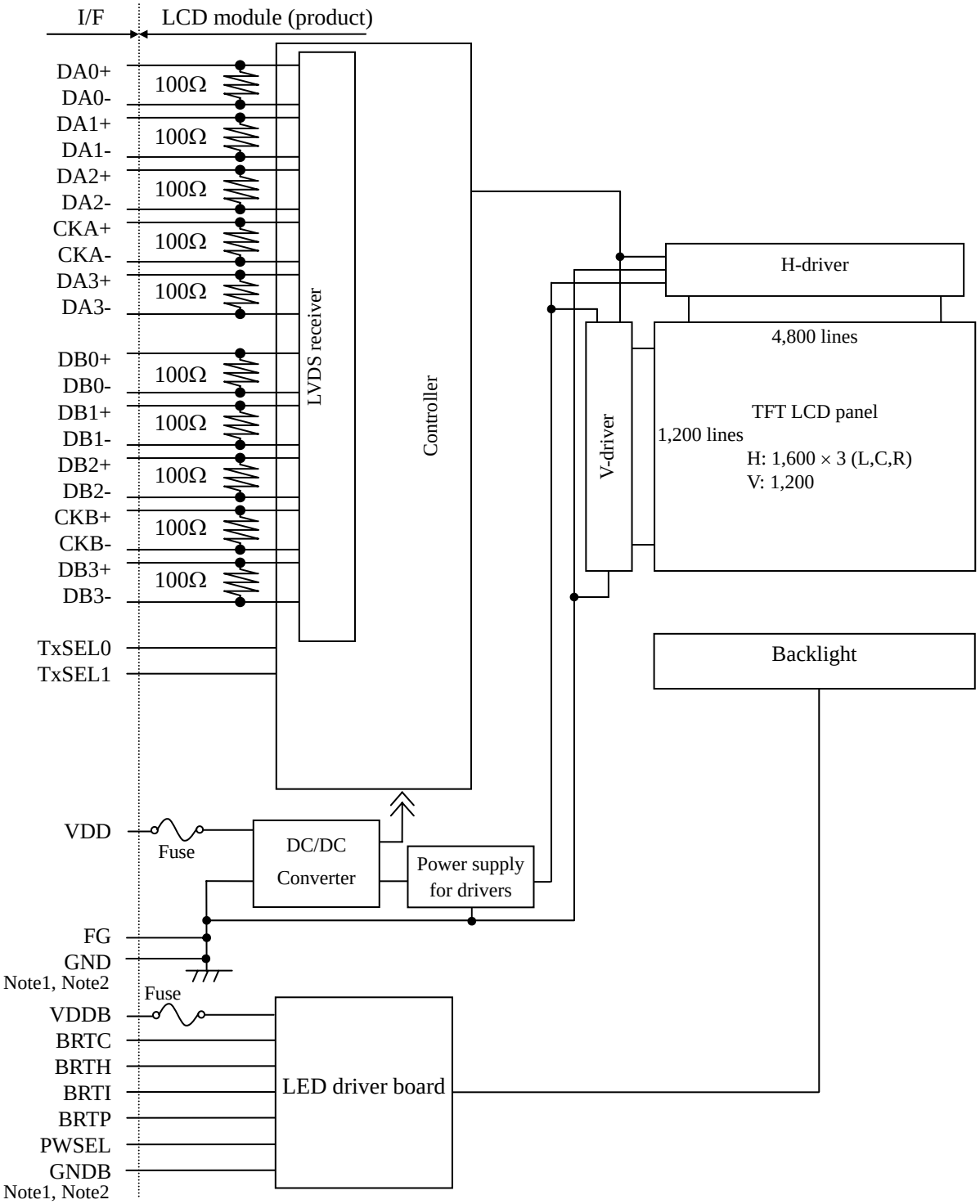
- Ultra-wide viewing angle (Super Fine TFT (SFT))
- High luminance
- High contrast
- High resolution
- Low reflection
- 256 gray scale per 1 sub-pixel (8-bit)
- LVDS interface
- Selectable LVDS data input map
- Small foot print
- Long life LED backlight type with an LED driver board
- Compliant with the European RoHS directive (2011/65/EU) ☆
- Acquisition product for UL60950-1/CSA C22.2 No.60950-1-03 (File number: E170632) ☆

2. GENERAL SPECIFICATIONS

Display area	432.0 (H) × 324.0 (V) mm	
Diagonal size of display	54 cm (21.3 inches)	
Drive system	a-Si TFT active matrix	
Display color	256 gray scales per 1 sub-pixel (8-bit) (766 gray scales per 1 pixel)	
Pixel	1,600 (H) × 1,200 (V) pixels (1 pixel consists of 3 sub-pixels (LCR).)	
Pixel arrangement	LCR vertical stripe	
Dot pitch	0.090 (H) × 0.270 (V) mm	
Pixel pitch	0.270 (H) × 0.270 (V) mm	
Module size	457.0 (W) × 350.0 (H) × 21.5 (D) mm (typ.)	
Weight	2,700 g (typ.)	☆
Contrast ratio	1,400:1 (typ.)	☆
Viewing angle	*At the contrast ratio ≥ 10:1* • Horizontal: Right side 88° (typ.), Left side 88° (typ.) • Vertical: Up side 88° (typ.), Down side 88° (typ.)	
Designed viewing direction	Viewing angle with optimum grayscale (γ≒ DICOM): normal axis (perpendicular) Note1	
Polarizer surface	Antiglare	
Polarizer pencil-hardness	2H (min.) [by JIS K5600]	
Response time	*Ton+Toff (10%←→ 90%)* 40 ms (typ.)	☆
Luminance	*At the maximum luminance* 1,900 cd/m^2 (typ.)	☆
Signal system	2 ports LVDS interface (THC63LVD824A THine Electronics, Inc. or equivalent) [LCR 8-bit signals, Data enable signal (DE), Dot clock (CK)]	
Power supply voltage	LCD panel signal processing board: 12.0V LED driver board: 12.0V	
Backlight	LED backlight type with LED driver board	
Power consumption	*At checkered flag pattern, the maximum luminance* 36.0 W (typ.)	☆

Note1: When the product luminance is 450cd/m^2, the gamma characteristic is designed to γ≒ DICOM.

3. BLOCK DIAGRAM



Note1: Relations between GND (Signal ground), FG (Frame ground) and GNDB (LED driver board ground) in the LCD module are as follows.

GND - FG	Connected
GND - GNDB	Not connected
FG - GNDB	Not connected

Note2: GND, FG and GNDB must be connected to customer equipment's ground, and it is recommended that these grounds be connected together in customer equipment.

Note3 Each pair of the LVDS signal has a 100Ω terminating resistance between D+ and D-. ☆

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification		Unit
Module size	457.0 ±0.5 (W) × 350.0 ±0.5 (H) × 21.5 (typ., D) 23.0 (max. D)	Note1, Note2	mm
Display area	432.0 (H) × 324.0 (V)	Note2	mm
Weight	2,700 (typ.), 2,980 (max.)		g

Note1: Excluding warpage of the cover for LED driver board.
Note2: See "**8. OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter			Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board		VDD	-0.3 to +14.0	V	Ta = 25°C
	LED driver board		VDDB	-0.3 to +15.0	V	
Input voltage for signals	LCD panel signal processing board Note1		Vi	-0.3 to +3.45	V	VDD= 12.0V
	LED driver board	BRTI signal	VBI	-0.3 to +1.5	V	VDDB= 12.0V
		BRTP signal	VBP	-0.3 to +5.5	V	
		BRTC signal	VBC	-0.3 to +5.5	V	
		PWSEL signal	VBS	-0.3 to +5.5	V	
Storage temperature			Tst	-20 to +60	°C	-
Operating temperature	Front surface		TopF	0 to +60	°C	Note2
	Rear surface		TopR	0 to +60	°C	Note3
Relative humidity Note4			RH	≤ 95	%	Ta ≤ 40°C
				≤ 85	%	40°C < Ta ≤ 50°C
				≤ 70	%	50°C < Ta ≤ 55°C
Absolute humidity Note4			AH	≤ 73 Note5	g/m^3	Ta > 55°C
Operating altitude			-	≤ 5,100	m	0°C ≤ Ta ≤ 55°C
Storage altitude			-	≤ 13,600	m	-20°C ≤ Ta ≤ 60°C

Note1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-
Note2: Measured at LCD panel surface (including self-heat)
Note3: Measured at LCD module's rear shield surface (including self-heat)
Note4: No condensation
Note5: Water amount at Ta = 55°C and RH = 70%
Note6: The image quality may cause degradation in case of rapid change humidity and temperature.

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta = 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDD	10.8	12.0	13.2	V	-
Power supply current		IDD	-	500 Note1	700 Note2	mA	at VDD= 12.0V ☆
Permissible ripple voltage		VRP	-	-	100	mVp-p	for VDD
Differential input threshold voltage	High	VTH	-	-	+100	mV	at VCM= 1.2V Note3, Note4
	Low	VTL	-100	-	-	mV	
Input voltage swing		VI	0	-	2.4	V	Note4
Terminating resistance		RT	-	100	-	Ω	-

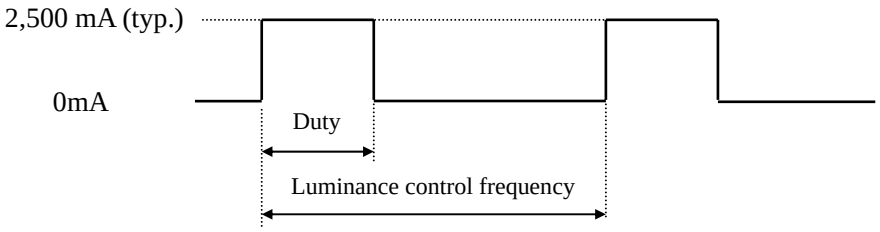
Note1: Checkered flag pattern (by EIAJ ED-2522)
Note2: Pattern for maximum current
Note3: Common mode voltage for LVDS driver
Note4: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-

4.3.2 LED Driver board

(Ta = 25°C)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks	
Power supply voltage			VDDB	11.4	12.0	12.6	V	-	☆
Power supply current			IDDB	-	2,500	3,300	mA	VDDB= 12.0V, At the maximum luminance control	☆
Input voltage for signals	BRTI signal		VBI	0	-	1.0	V	-	
	BRTP signal	High	VBPH	2.0	-	5.25	V		
		Low	VBPL	0	-	0.8	V		
	BRTC signal	High	VBCH	2.0	-	5.25	V		
		Low	VBCL	0	-	0.8	V		
	PWSEL signal	High	VBSH	2.0	-	5.25	V		
		Low	VBSL	0	-	0.8	V		
Input current for signals	BRTI signal		IBI	-200	-	-100	μA		
	BRTP signal	High	IBPH	-	-	1,000	μA		
		Low	IBPL	-600	-	-	μA		
	BRTC signal	High	IBCH	-	-	300	μA		☆
		Low	IBCL	-300	-	-	μA		
	PWSEL signal	High	IPSH	-	-	1,000	μA		
		Low	IPSL	-600	-	-	μA		

4.3.3 LED driver board current wave



☆

Duty: At the maximum luminance control 100% to at the minimum luminance control 1%.
Luminance control frequency: 270Hz (typ.) ☆

Note1: Luminance control frequency indicate the input pulse frequency, when select the external pulse control. See "**4.6.2 Detail of BRTP timing**".

Note2: The power supply lines (VDDB and GNDB) have large ripple voltage during luminance control. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on. Put a capacitor (5,000 to 6,000μF) between the power supply lines (VDDB and GNDB) to reduce the noise, if the noise occurred in the circuit..

4.3.4 Power supply voltage ripple

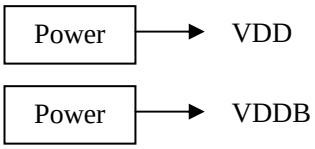
This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VDD	12.0V	≤ 100	mVp-p
VDDB	12.0V	≤ 200	mVp-p

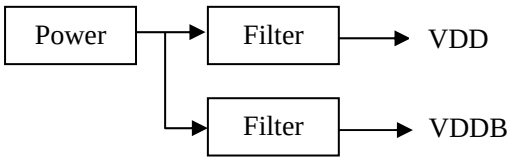
Note1: The permissible ripple voltage includes spike noise.

Example of the power supply connection

a) Separate the power supply



b) Put in the filter



4.3.5 Fuse

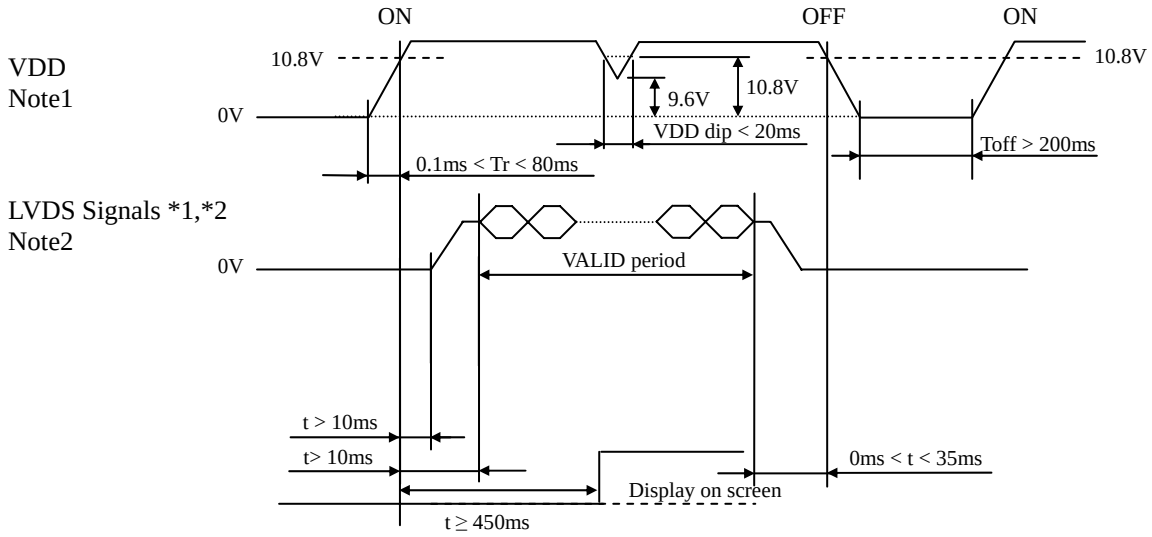
Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	FCC16132AB	KAMAYA ELECTRIC Co., Ltd.	1.25A 32V	2.5A, 5 seconds maximum	Note1
VDDB	CCF1N10	KOA Corporation	10A 60 V	20 A, 1 seconds maximum	
	TF16AT5.00T		5.0A 32V	10 A, 5 seconds maximum	

☆

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 LCD panel signal processing board



*1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/- and CKB+/-

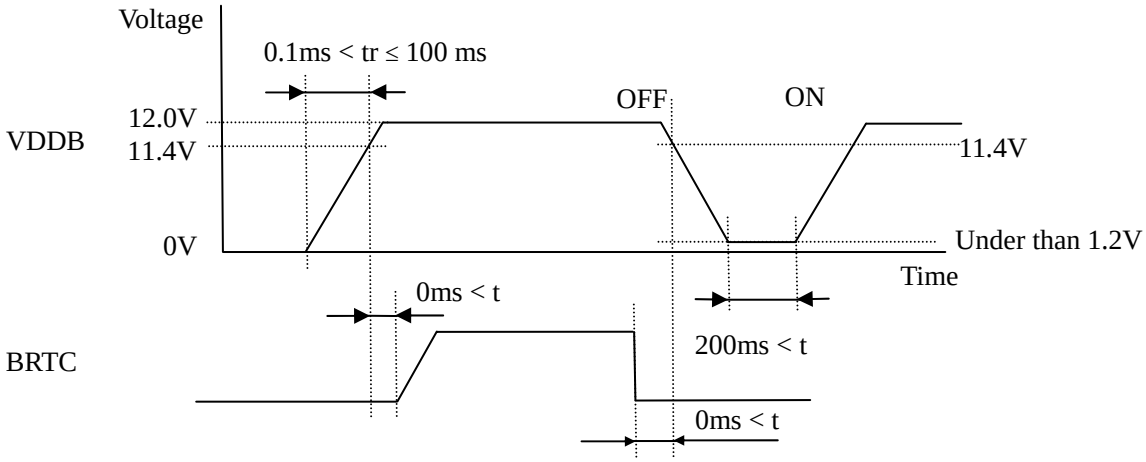
*2: LVDS signals should be measured at the terminal of 100Ω resistance.

Note1: If there is a voltage variation (voltage drop) at the rising edge of VCC below 10.8V, there is a possibility that a product does not work due to a protection circuit.

Note2: LVDS signals must be set to Low or High-impedance, except the VALID period (See above sequence diagram), in order to avoid the circuitry damage.
If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. If a customer stops the display and function signals, VCC also must be shut down.

Note3: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.

4.4.2 LED driver board ☆



Note1: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.

Note2: If tr is more than 100ms, the backlight will be turned off by a protection circuit for LED driver board. ☆

Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

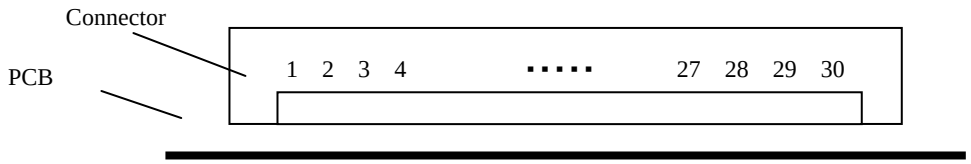
4.5.1 LCD panel signal processing board

CN1 Socket (LCD module side): DF19G-30P-1H (56) (Hirose Electric Co., Ltd. (HRS))
Adaptable plug: DF19-30S-1C (Hirose Electric Co., Ltd. (HRS))

Pin No.	Symbol	Signal	Remarks
1	DA0-	Pixel data A0	Odd pixel data Input (LVDS differential signal) Note1
2	DA0+		
3	DA1-	Pixel data A1	Odd pixel data Input (LVDS differential signal) Note1
4	DA1+		
5	DA2-	Pixel data A2	Odd pixel data Input (LVDS differential signal) Note1
6	DA2+		
7	GND	Ground	Signal ground Note2
8	CKA-	Pixel clock	Odd pixel clock Input (LVDS differential signal) Note1
9	CKA+		
10	DA3-	Pixel data A3	Odd pixel data Input (LVDS differential signal) Note1
11	DA3+		
12	DB0-	Pixel data B0	Even pixel data Input (LVDS differential signal) Note1
13	DB0+		
14	GND	Ground	Signal ground Note2
15	DB1-	Pixel data B1	Even pixel data Input (LVDS differential signal) Note1
16	DB1+		
17	GND	Ground	Signal ground Note2
18	DB2-	Pixel data B2	Even pixel data Input (LVDS differential signal) Note1
19	DB2+		
20	CKB-	Pixel clock	Even pixel clock Input (LVDS differential signal) Note1
21	CKB+		
22	DB3-	Pixel data B3	Even pixel data Input (LVDS differential signal) Note1
23	DB3+		
24	GND	Ground	Signal ground Note2
25	TxSEL0	Selection of LVDS data input map	Note3, Note4
26	TxSEL1		
27	GND	Ground	Signal ground Note2
28	VDD	Power supply	12V Note2
29	VDD		
30	VDD		

TxSEL1	TxSEL0	Mode
Open	Open	A
Open	Low	B
Low	Open	C
Low	Low	A

CN1: Insert surface side ☆



Note1: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.
Note2: All GND and VDD terminals should be used without any non-connected lines.
Note3: This terminal is pulled-up in the product.
Note4: See "**4.7 LVDS DATA INPUT MAP**".

4.5.2 LED driver board

CN201 socket (LCD module side): DF3Z-10P-2H (2*) (HIROSE ELECTRIC Co,. Ltd.)
Adaptable plug: DF3-10S-2C (HIROSE ELECTRIC Co,. Ltd.)

Pin No.	Symbol	Function	Description
1	GNDB	LED driver board ground	Note1
2	GNDB		
3	GNDB		
4	GNDB		
5	GNDB		
6	VDDB	Power supply	Note1
7	VDDB		
8	VDDB		
9	VDDB		
10	VDDB		

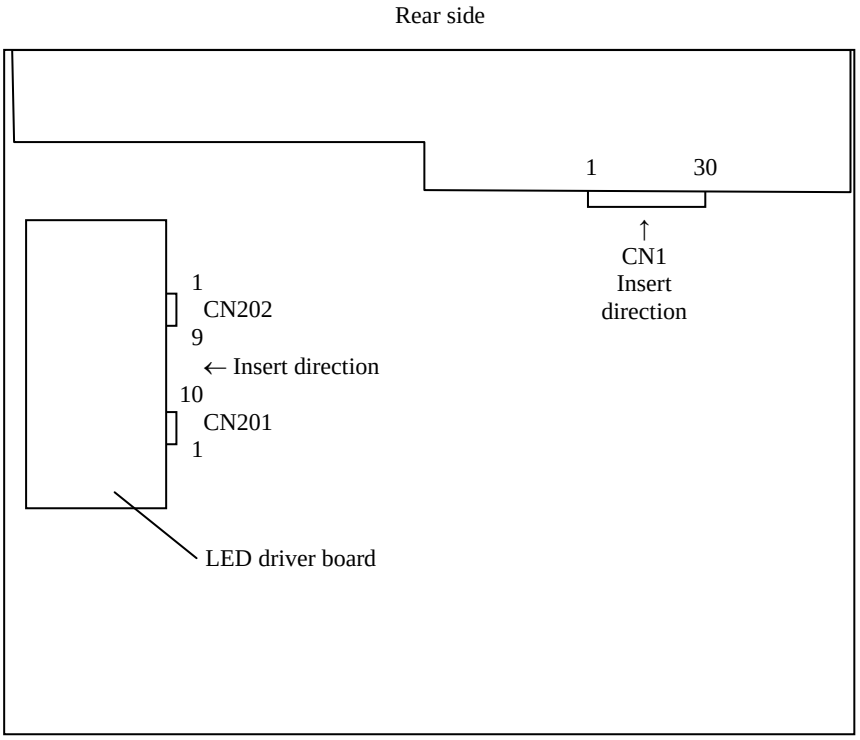
Note1: All VDDB and GNDB terminals should be used without any non-connected lines.

CN202 socket (LCD module side): IL-Z-9PL-SMTYE (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: IL-Z-9S-S125C3 (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	GNDB	LED driver board ground	Note1
2	GNDB		
3	N.C.	-	Keep this pin Open.
4	BRTC	Backlight ON/OFF control signal	High or Open: Backlight ON Low: Backlight OFF
5	BRTH	Luminance control terminal	Note2
6	BRTI		
7	BRTP	BRTP signal	
8	GNDB	LED driver board ground	Note1
9	PWSEL	Selection of luminance control signal method	Note2, Note3

Note1: All GNDB terminals should be used without any non-connected lines.
Note2: See "**4.6 LUMINANCE CONTROL** ".
Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

4.5.3 Positions of socket

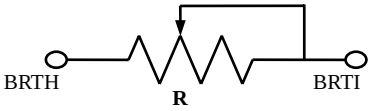


4.6 LUMINANCE CONTROL

4.6.1 Luminance control methods

<table>
<tr><th>Method</th><th>Adjustment and luminance ratio</th><th>PWSEL terminal</th><th>BRTP terminal</th></tr>
<tr><td>Variable resistor control

Note1</td><td>• Adjustment

The variable resistor (R) for luminance control should be 10kΩ ±5%, 1/10W. Minimum point of the resistance is the minimum luminance and maximum point of the resistance is the maximum luminance.
The resistor (R) must be connected between BRTH-BRTI terminals.
 

• Luminance ratio Note3
<table><tr><th>Resistance</th><th>Luminance ratio</th></tr><tr><td>0Ω</td><td>0%(Min. Luminance)</td></tr><tr><td>10 kΩ</td><td>100% (Max. Luminance)</td></tr></table></td><td rowspan="2">High or Open</td><td rowspan="2">Open</td></tr>
<tr><td>Voltage control

Note1</td><td>• Adjustment

Voltage control method works, when BRTH terminal is 0V and VBI voltage is input between BRTI-BRTH terminals. This control method can carry out continuation adjustment of luminance.
Luminance is the maximum when BRTI terminal is Open.

• Luminance ratio Note3
<table><tr><th>BRTI Voltage (VBI)</th><th>Luminance ratio</th></tr><tr><td>0V</td><td>0% (Min. Luminance)</td></tr><tr><td>1.0V</td><td>100% (Max. Luminance)</td></tr></table></td></tr>
<tr><td>Pulse width modulation

Note1
Note2
Note4</td><td>• Adjustment

Pulse width modulation (PWM) method works, when PWSEL terminal is Low and PWM signal (BRTP signal) is input into BRTP terminal. The luminance is controlled by duty ratio of BRTP signal.

• Luminance ratio Note3
<table><tr><th>Duty ratio</th><th>Luminance ratio</th></tr><tr><td>0.01</td><td>1% (Min. Luminance)
(At frequency: 325 Hz)</td></tr><tr><td>1.0</td><td>100% (Max. Luminance)</td></tr></table></td><td>Low</td><td>BRTP signal</td></tr>
</table>

☆

Note1: In case of the variable resistor control method and the voltage control method, noises may appear on the display image depending on the input signals timing for LCD panel signal processing board.

Use PWM method, if interference noises appear on the display image!

Note2: The LED driver board will stop working, if the Low period of BRTP signal is more than 50ms while BRTC signal is High or Open. Then the backlight will not turn on anymore, even if BRTP signal is input again. This is not out of order. The LED driver board will start to work when power is supplied again.

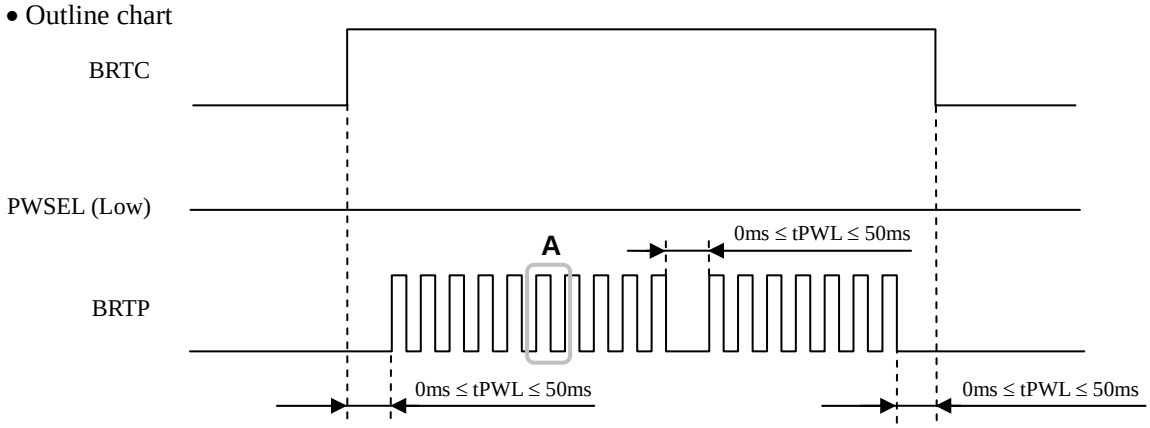
Note3: These data are the target values.

Note4: See "**4.6.2 Detail of BRTP timing**".

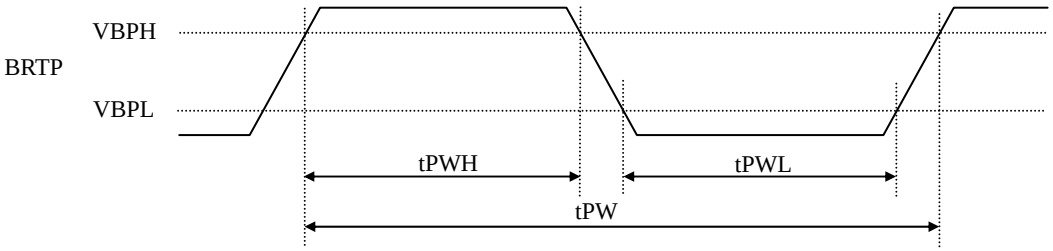
4.6.2 Detail of BRTP timing

(1) Timing diagrams

• Outline chart



• Detail of **A** part



(2) Each parameter

Parameter	Symbol	min.	typ.	max.	Unit	Remarks	
PWM frequency	f_{PWM}	185	-	1,000	Hz	Note1,2,3	☆
PWM duty ratio	DR_{PWM}	1	-	100	%	Note4,5	☆
PWM pulse width	tPWH	30	-	-	μs	Note1,4,5	☆

Note1: Definition of parameters is as follows.

$$f_{PWM} = \frac{1}{tPW} \quad DL = \frac{tPWH}{tPW}$$

Note2: A recommended f_{PWM} value is as follows. ☆

$$f_{PWM} = \frac{2n-1}{4} \times fv$$

(n= integer, fv= frame frequency of LCD module)

Note3: Depending on the frequency used, so noise may appear on the screen, please conduct a thorough evaluation. ☆

Note4: While the BRTC signal is high, do not set the tPWH (PWM pulse width) is less than 30μs. It may cause abnormal working of the backlight. In this case, turn the backlight off and then on again by BRTC signal. ☆

Note5: Regardless of the PWM frequency, both PWM duty ratio and PWM pulse width must be always more than the minimum values. ☆

4.7 LVDS DATA INPUT MAP

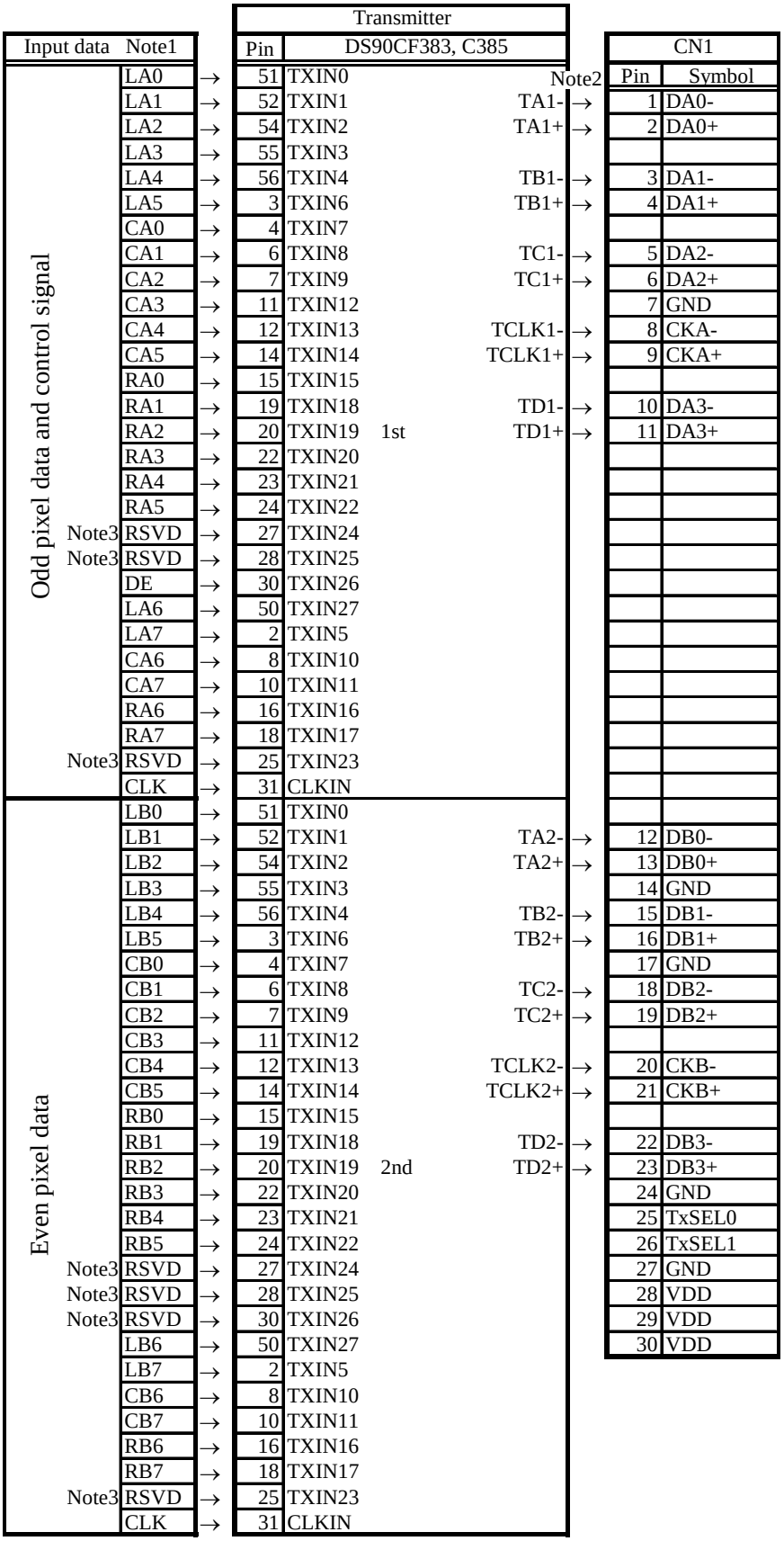
4.7.1 Mode A

Input data	Note1		Transmitter Pin	THC63LVDM83D		Transmitter Pin	THC63LVD823B	Note2	CN1 Pin	CN1 Symbol
Odd pixel data and control signal	LA2	→	51	TA0		53	R12			
	LA3	→	52	TA1		54	R13	TA1- →	1	DA0-
	LA4	→	54	TA2		57	R14	TA1+ →	2	DA0+
	LA5	→	55	TA3		58	R15			
	LA6	→	56	TA4		59	R16	TB1- →	3	DA1-
	LA7	→	3	TA5		60	R17	TB1+ →	4	DA1+
	CA2	→	4	TA6		63	G12			
	CA3	→	6	TB0		64	G13	TC1- →	5	DA2-
	CA4	→	7	TB1		65	G14	TC1+ →	6	DA2+
	CA5	→	11	TB2		66	G15		7	GND
	CA6	→	12	TB3		67	G16	TCLK1- →	8	CKA-
	CA7	→	14	TB4		68	G17	TCLK1+ →	9	CKA+
	RA2	→	15	TB5		73	B12			
	RA3	→	19	TB6		74	B13	TD1- →	10	DA3-
	RA4	→	20	TC0	1st	75	B14	TD1+ →	11	DA3+
	RA5	→	22	TC1		76	B15			
	RA6	→	23	TC2		77	B16			
	RA7	→	24	TC3		78	B17			
Note3	RSVD	→	27	TC4		7	RSVD			
Note3	RSVD	→	28	TC5		8	RSVD			
	DE	→	30	TC6		9	DE			
	LA0	→	50	TD0		51	R10			
	LA1	→	2	TD1		52	R11			
	CA0	→	8	TD2		61	G10			
	CA1	→	10	TD3		62	G11			
	RA0	→	16	TD4		69	B10			
	RA1	→	18	TD5		70	B11			
Note3	RSVD	→	25	TD6		-				
	CLK	→	31	CLKIN		10	CLK			
Even pixel data	LB2	→	51	TA0		81	R22			
	LB3	→	52	TA1		82	R23	TA2- →	12	DB0-
	LB4	→	54	TA2		83	R24	TA2+ →	13	DB0+
	LB5	→	55	TA3		84	R25		14	GND
	LB6	→	56	TA4		85	R26	TB2- →	15	DB1-
	LB7	→	3	TA5		86	R27	TB2+ →	16	DB1+
	CB2	→	4	TA6		91	G22		17	GND
	CB3	→	6	TB0		92	G23	TC2- →	18	DB2-
	CB4	→	7	TB1		93	G24	TC2+ →	19	DB2+
	CB5	→	11	TB2		94	G25			
	CB6	→	12	TB3		95	G26	TCLK2- →	20	CKB-
	CB7	→	14	TB4		96	G27	TCLK2+ →	21	CKB+
	RB2	→	15	TB5		99	B22			
	RB3	→	19	TB6		100	B23	TD2- →	22	DB3-
	RB4	→	20	TC0	2nd	1	B24	TD2+ →	23	DB3+
	RB5	→	22	TC1		2	B25		24	GND
	RB6	→	23	TC2		5	B26		25	TxSEL0
	RB7	→	24	TC3		6	B27		26	TxSEL1
Note3	RSVD	→	27	TC4		-			27	GND
Note3	RSVD	→	28	TC5		-			28	VDD
Note3	RSVD	→	30	TC6		-			29	VDD
	LB0	→	50	TD0		79	R20		30	VDD
	LB1	→	2	TD1		80	R21			
	CB0	→	8	TD2		89	G20			
	CB1	→	10	TD3		90	G21			
	RB0	→	16	TD4		97	B20			
	RB1	→	18	TD5		98	B21			
Note3	RSVD	→	25	TD6		-				
	CLK	→	31	CLKIN		-				

4.7.2 Mode B

Input data		Note1		Transmitter Pin	DS90CF383, C385			CN1 Pin	Symbol
Odd pixel data and control signal		LA7	→	51	TXIN0		Note2		
		LA6	→	52	TXIN1		TA1- →	1	DA0-
		LA5	→	54	TXIN2		TA1+ →	2	DA0+
		LA4	→	55	TXIN3				
		LA3	→	56	TXIN4		TB1- →	3	DA1-
		LA2	→	3	TXIN6		TB1+ →	4	DA1+
		CA7	→	4	TXIN7				
		CA6	→	6	TXIN8		TC1- →	5	DA2-
		CA5	→	7	TXIN9		TC1+ →	6	DA2+
		CA4	→	11	TXIN12			7	GND
		CA3	→	12	TXIN13		TCLK1- →	8	CKA-
		CA2	→	14	TXIN14		TCLK1+ →	9	CKA+
		RA7	→	15	TXIN15				
		RA6	→	19	TXIN18		TD1- →	10	DA3-
		RA5	→	20	TXIN19	1st	TD1+ →	11	DA3+
		RA4	→	22	TXIN20				
		RA3	→	23	TXIN21				
		RA2	→	24	TXIN22				
	Note3	RSVD	→	27	TXIN24				
	Note3	RSVD	→	28	TXIN25				
		DE	→	30	TXIN26				
		LA1	→	50	TXIN27				
		LA0	→	2	TXIN5				
		CA1	→	8	TXIN10				
		CA0	→	10	TXIN11				
		RA1	→	16	TXIN16				
		RA0	→	18	TXIN17				
	Note3	RSVD	→	25	TXIN23				
		CLK	→	31	CLKIN				
Even pixel data		LB7	→	51	TXIN0				
		LB6	→	52	TXIN1		TA2- →	12	DB0-
		LB5	→	54	TXIN2		TA2+ →	13	DB0+
		LB4	→	55	TXIN3			14	GND
		LB3	→	56	TXIN4		TB2- →	15	DB1-
		LB2	→	3	TXIN6		TB2+ →	16	DB1+
		CB7	→	4	TXIN7			17	GND
		CB6	→	6	TXIN8		TC2- →	18	DB2-
		CB5	→	7	TXIN9		TC2+ →	19	DB2+
		CB4	→	11	TXIN12				
		CB3	→	12	TXIN13		TCLK2- →	20	CKB-
		CB2	→	14	TXIN14		TCLK2+ →	21	CKB+
		RB7	→	15	TXIN15				
		RB6	→	19	TXIN18		TD2- →	22	DB3-
		RB5	→	20	TXIN19	2nd	TD2+ →	23	DB3+
		RB4	→	22	TXIN20			24	GND
		RB3	→	23	TXIN21			25	TxSEL0
		RB2	→	24	TXIN22			26	TxSEL1
	Note3	RSVD	→	27	TXIN24			27	GND
	Note3	RSVD	→	28	TXIN25			28	VDD
	Note3	RSVD	→	30	TXIN26			29	VDD
		LB1	→	50	TXIN27			30	VDD
		LB0	→	2	TXIN5				
		CB1	→	8	TXIN10				
		CB0	→	10	TXIN11				
		RB1	→	16	TXIN16				
		RB0	→	18	TXIN17				
	Note3	RSVD	→	25	TXIN23				
		CLK	→	31	CLKIN				

4.7.3 Mode C



Input data	Note1		Transmitter Pin	DS90CF383, C385			CN1 Pin	CN1 Symbol
Odd pixel data and control signal	LA0	→	51	TXIN0		Note2		
	LA1	→	52	TXIN1		TA1- →	1	DA0-
	LA2	→	54	TXIN2		TA1+ →	2	DA0+
	LA3	→	55	TXIN3				
	LA4	→	56	TXIN4		TB1- →	3	DA1-
	LA5	→	3	TXIN6		TB1+ →	4	DA1+
	CA0	→	4	TXIN7				
	CA1	→	6	TXIN8		TC1- →	5	DA2-
	CA2	→	7	TXIN9		TC1+ →	6	DA2+
	CA3	→	11	TXIN12			7	GND
	CA4	→	12	TXIN13		TCLK1- →	8	CKA-
	CA5	→	14	TXIN14		TCLK1+ →	9	CKA+
	RA0	→	15	TXIN15				
	RA1	→	19	TXIN18		TD1- →	10	DA3-
	RA2	→	20	TXIN19	1st	TD1+ →	11	DA3+
	RA3	→	22	TXIN20				
	RA4	→	23	TXIN21				
	RA5	→	24	TXIN22				
Note3	RSVD	→	27	TXIN24				
Note3	RSVD	→	28	TXIN25				
	DE	→	30	TXIN26				
	LA6	→	50	TXIN27				
	LA7	→	2	TXIN5				
	CA6	→	8	TXIN10				
	CA7	→	10	TXIN11				
	RA6	→	16	TXIN16				
	RA7	→	18	TXIN17				
Note3	RSVD	→	25	TXIN23				
	CLK	→	31	CLKIN				
Even pixel data	LB0	→	51	TXIN0				
	LB1	→	52	TXIN1		TA2- →	12	DB0-
	LB2	→	54	TXIN2		TA2+ →	13	DB0+
	LB3	→	55	TXIN3			14	GND
	LB4	→	56	TXIN4		TB2- →	15	DB1-
	LB5	→	3	TXIN6		TB2+ →	16	DB1+
	CB0	→	4	TXIN7			17	GND
	CB1	→	6	TXIN8		TC2- →	18	DB2-
	CB2	→	7	TXIN9		TC2+ →	19	DB2+
	CB3	→	11	TXIN12				
	CB4	→	12	TXIN13		TCLK2- →	20	CKB-
	CB5	→	14	TXIN14		TCLK2+ →	21	CKB+
	RB0	→	15	TXIN15				
	RB1	→	19	TXIN18		TD2- →	22	DB3-
	RB2	→	20	TXIN19	2nd	TD2+ →	23	DB3+
	RB3	→	22	TXIN20			24	GND
	RB4	→	23	TXIN21			25	TxSEL0
	RB5	→	24	TXIN22			26	TxSEL1
Note3	RSVD	→	27	TXIN24			27	GND
Note3	RSVD	→	28	TXIN25			28	VDD
Note3	RSVD	→	30	TXIN26			29	VDD
	LB6	→	50	TXIN27			30	VDD
	LB7	→	2	TXIN5				
	CB6	→	8	TXIN10				
	CB7	→	10	TXIN11				
	RB6	→	16	TXIN16				
	RB7	→	18	TXIN17				
Note3	RSVD	→	25	TXIN23				
	CLK	→	31	CLKIN				

Note1: LSB (Least Significant Bit) – LA0, CA0, RA0, LB0, CB0, RB0
MSB (Most Significant Bit) – LA7, CA7, RA7, LB7, CB7, RB7

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

Note3: Input signal RSVD is not used inside the product, but do not keep pin open to avoid noise problem.

4.8 DISPLAY GRAYSCALE AND INPUT DATA SIGNALS

This product can display 256 gray scales in each LCR sub-pixel and 766 gray scales per 1 pixel. Also the relation between display gray scale and input data signals is as the following table.

Display grayscale		Data signal (0: Low level, 1: High level)																									
		LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
		LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
Left sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑					:								:								:			
	↓					:								:								:			
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Center sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑					:								:								:			
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	White	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Right sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑					:								:								:			
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	White	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

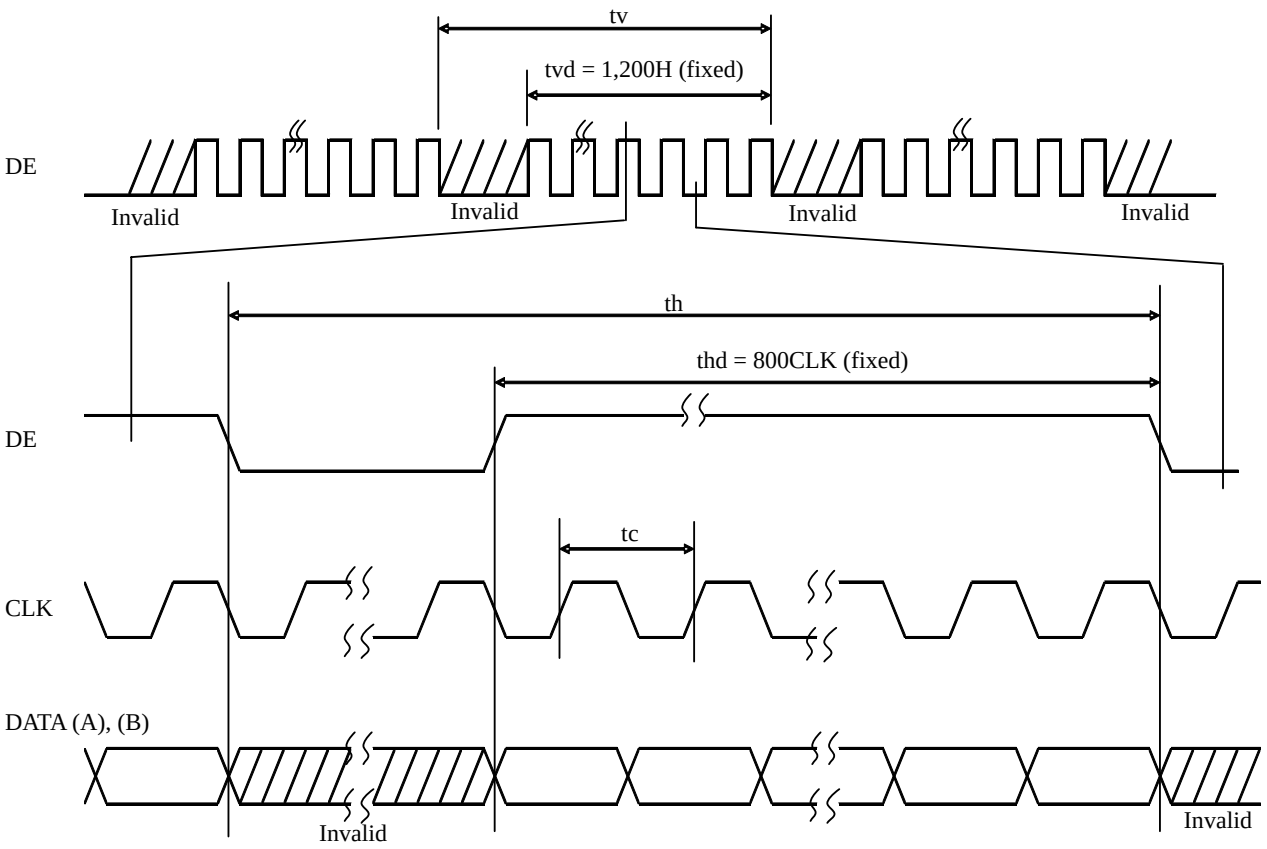
4.9 INPUT SIGNAL TIMINGS

4.9.1 Timing characteristics

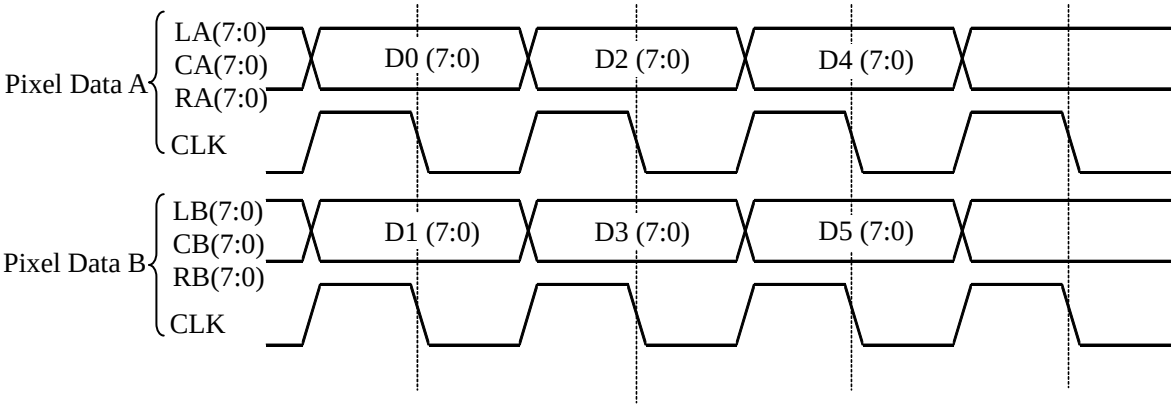
Parameter		Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency	1/ tc	60.0	64.5	65.0	MHz	LVDS transmitter input
	Pulse width	tc	15.38	15.5	-	ns	
	Duty	-	See the data sheet of LVDS transmitter.			-	-
	Rise, fall	-				ns	
Horizontal	Cycle	th	13.1	13.3	19.2	µs	Note1
			848	860	1,156	CLK	
	Display period	thd	800			CLK	-
Vertical	Cycle	1/tv	59	60	61	Hz	-
		tv	1,206	1,250	-	H	
	Display period	tvd	1,200			H	-
DE, DATA	Setup time	-	See the data sheet of LVDS transmitter.			ns	-
	Hold time	-				ns	
	Rise, fall	-				ns	

Note1: During operation, fluctuation of horizontal cycle should be within ±1 CLK.

4.9.2 Input signal timing chart

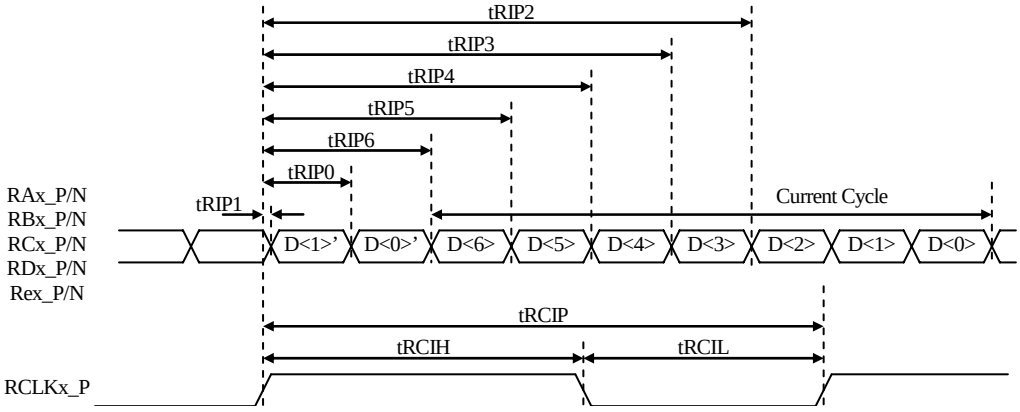


4.10 LVDS DATA TARANSMISSION METHOD



4.11 LVDS Rx AC SPEC ☆

Symbol	Parameter	min.	typ.	max.	Units
t_{RCIP}	RCLKx_P Period	11.76	-	40.0	ns
t_{RCIH}	RCLKx_P High pulse width	-	$\frac{4}{7}t_{RCIP}$	-	ns
t_{RCIL}	RCLKx_P Low pulse width	-	$\frac{3}{7}t_{RCIP}$	-	ns
t_{RMG}	Receiver Data Input Margin fCLKIN= 60MHz	-0.65	-	0.65	ns
	fCLKIN= 65MHz				
	fCLKIN=66MHz				
t_{RIP1}	Input Data Position0	$-\lvert t_{RMG}\rvert$	0.0	$+\lvert t_{RMG}\rvert$	ns
t_{RIP0}	Input Data Position1	$\frac{t_{RCIP}}{7}-\lvert t_{RMG}\rvert$	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7}+\lvert t_{RMG}\rvert$	ns
t_{RIP6}	Input Data Position2	$2\frac{t_{RCIP}}{7}-\lvert t_{RMG}\rvert$	$2\frac{t_{RCIP}}{7}$	$2\frac{t_{RCIP}}{7}+\lvert t_{RMG}\rvert$	ns
t_{RIP5}	Input Data Position3	$3\frac{t_{RCIP}}{7}-\lvert t_{RMG}\rvert$	$3\frac{t_{RCIP}}{7}$	$3\frac{t_{RCIP}}{7}+\lvert t_{RMG}\rvert$	ns
t_{RIP4}	Input Data Position4	$4\frac{t_{RCIP}}{7}-\lvert t_{RMG}\rvert$	$4\frac{t_{RCIP}}{7}$	$4\frac{t_{RCIP}}{7}+\lvert t_{RMG}\rvert$	ns
t_{RIP3}	Input Data Position5	$5\frac{t_{RCIP}}{7}-\lvert t_{RMG}\rvert$	$5\frac{t_{RCIP}}{7}$	$5\frac{t_{RCIP}}{7}+\lvert t_{RMG}\rvert$	ns
t_{RIP2}	Input Data Position6	$6\frac{t_{RCIP}}{7}-\lvert t_{RMG}\rvert$	$6\frac{t_{RCIP}}{7}$	$6\frac{t_{RCIP}}{7}+\lvert t_{RMG}\rvert$	ns



4.12 DISPLAY POSITIONS

Odd pixel: LA= Left data
CA= Center data
RA= Right data

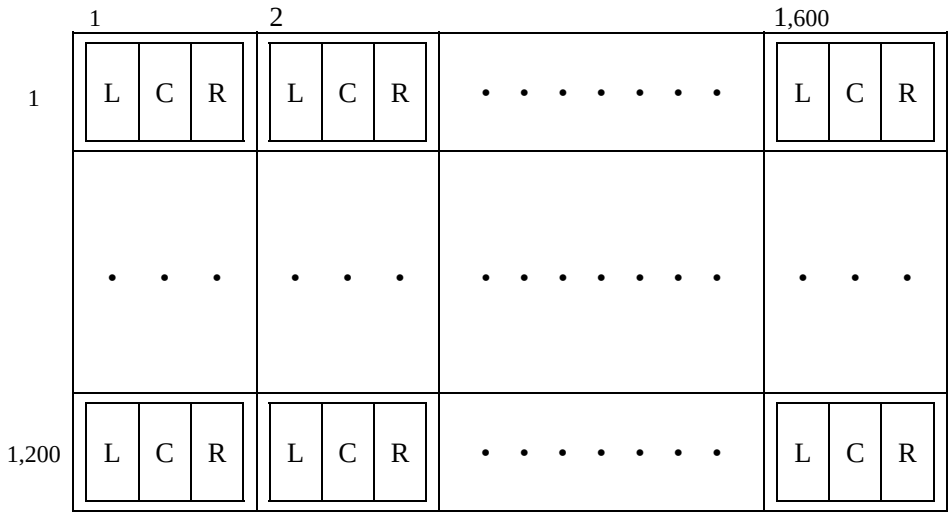
Even pixel: LB= Left data
CB= Center data
RB= Right data

D (1, 1) D (2, 1)

LA	CA	RA	LB	CB	RB

D(1, 1)	D(2, 1)	• • •	D(X, 1)	• • •	D(1599, 1)	D(1600, 1)
D(1, 2)	D(2, 2)	• • •	D(X, 2)	• • •	D(1599, 2)	D(1600, 2)
• • •	• • •	• • •	• • •	• • •	• • •	• • •
D(1, Y)	D(2, Y)	• • •	D(X, Y)	• • •	D(1599, Y)	D(1600, Y)
• • •	• • •	• • •	• • •	• • •	• • •	• • •
D(1, 1199)	D(2, 1199)	• • •	D(X, 1199)	• • •	D(1599, 1199)	D(1600, 1199)
D(1, 1200)	D(2, 1200)	• • •	D(X, 1200)	• • •	D(1599, 1200)	D(1600, 1200)

4.13 PIXEL ARRANGNMENT



4.14 OPTICS

4.14.1 Optical characteristics

(Note1, Note2)

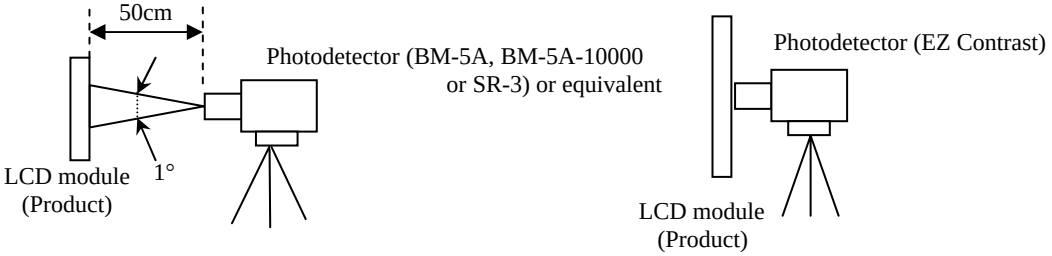
Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks	
Luminance		White at center θR= 0°, θL= 0°, θU= 0°, θD= 0°	L	1,400	1,900	-	cd/m^2	BM-5A or SR-3	Note3	☆
Contrast ratio		White/Black at center θR= 0°, θL= 0°, θU= 0°, θD= 0°	CR	1,000	1,400	-	-	BM-5A or SR-3	Note3 Note5	☆
Luminance uniformity		255/255 gray scale θR = 0°, θL = 0°, θU = 0°, θD = 0°	LU$_{1023}$	80	-	-	%	BM-5A or SR-3	Note4 Note6	☆
Chromaticity	White	**x** coordinate	Wx	0.269	0.299	0.329		SR-3	Note3 Note8	☆
		y coordinate	Wy	0.285	0.315	0.345	-			
Color uniformity		204/255 gray scale θR = 0°, θL = 0°, θU = 0°, θD = 0°	Δu'v'	-	-	0.01	-	SR-3	Note4 Note7	
Response time		Black to White	Ton	-	20	30	ms	BM-5A -10000	Note3 Note9	☆
		White to Black	Toff	-	20	30	ms			
Viewing angle	Right	θU= 0°, θD= 0°, CR≥ 10	θR	70	88	-	°	BM-5A or EZ Contrast	Note3 Note10	
	Left	θU= 0°, θD= 0°, CR≥ 10	θL	70	88	-	°			
	Up	θR= 0°, θL= 0°, CR≥ 10	θU	70	88	-	°			
	Down	θR= 0°, θL= 0°, CR≥ 10	θD	70	88	-	°			

Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.

Ta = 25°C, VDD = 12.0V, VDDB = 12.0V, PWM: Duty 100%, Display mode: UXGA,
Horizontal cycle = 1/75.19 kHz, Vertical cycle = 1/60.0Hz

Optical characteristics are measured at luminance saturation 20minutes after the product works in the dark room. Also measurement methods are as follows.



Note3: Product surface temperature at the maximum luminance control: TopF = 29°C

Note4: Product surface temperature at 450cd/m^2 luminance control: TopF = 27°C
Temperature difference in display area: ΔTBD°C

Note5: See "**4.14.2 Definition of contrast ratio**".
Note6: See "**4.14.3 Definition of luminance uniformity**".
Note7: See "**4.14.4 Definition of color uniformity**".
Note8: These coordinates are found on CIE 1931 chromaticity diagram.
Note9: See "**4.14.5 Definition of response times**".
Note10: See "**4.14.6 Definition of viewing angles**".

4.14.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

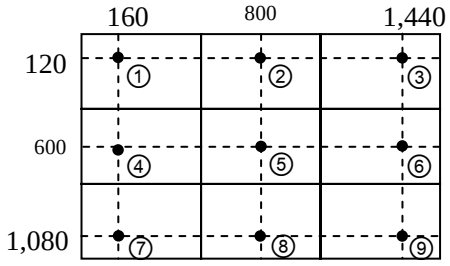
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.14.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

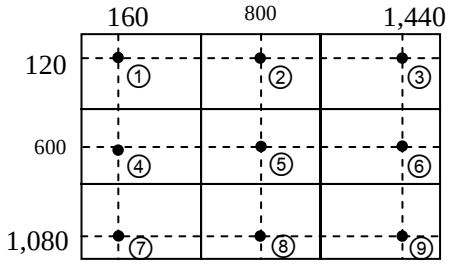
$$\text{Luminance uniformity (LU)} = \frac{\text{Minimum luminance from ① to ⑤}}{\text{Maximum luminance from ① to ⑤}}$$

The luminance is measured at near the 9 points shown below.



4.14.4 Definition of color uniformity

The color (u', v') is measured at near the 9 points shown below.



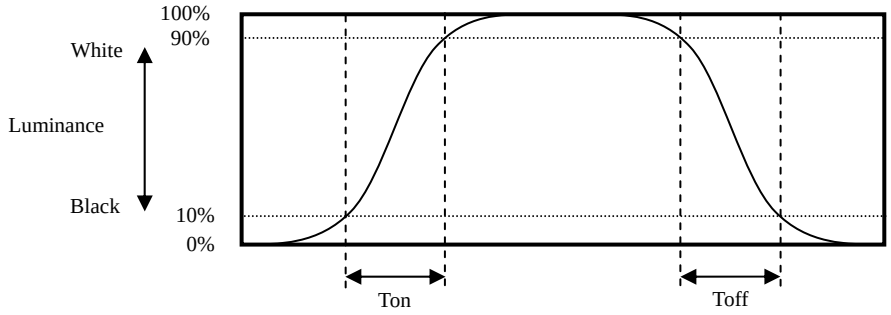
The color uniformity in each measuring point is calculated by using the following formula.

$$\text{Color uniformity}(\Delta u'v') = \sqrt{(u'_x - u'_y)^2 + (v'_x - v'_y)^2}$$

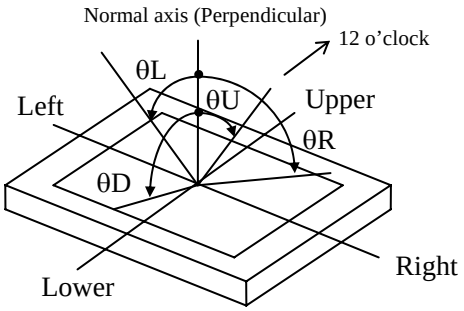
u'_x, v'_x: u', v' value at measuring point x.
u'_y, v'_y: u', v' value at measuring point y.

4.14.5 Definition of response times

Response time is measured at the time when the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time when the luminance changes from 10% up to 90%. Also Toff is the time when the luminance changes from 90% down to 10% (See the following diagram.).



4.14.6 Definition of viewing angles



5. ESTIMATED LUMINANCE LIFETIME

The luminance lifetime is the time from initial luminance to half-luminance.

This lifetime is the estimated value, and is not guarantee value.

Condition		Estimated luminance lifetime (Life time expectancy) Note1, Note2, Note3	Unit
LED elementary substance	25°C (Ambient temperature of the product) Continuous operation, PWM: Duty 100%	70,000	h
	60°C (Surface temperature at screen) Continuous operation, PWM: Duty 100%	60,000	

☆

Note1: Life time expectancy is mean time to half-luminance.
Note2: Estimated luminance lifetime is not the value for an LCD module but the value for LED elementary substance.
Note3: By ambient temperature, the lifetime changes particularly. Especially, in case the product works under high temperature environment, the lifetime becomes short.

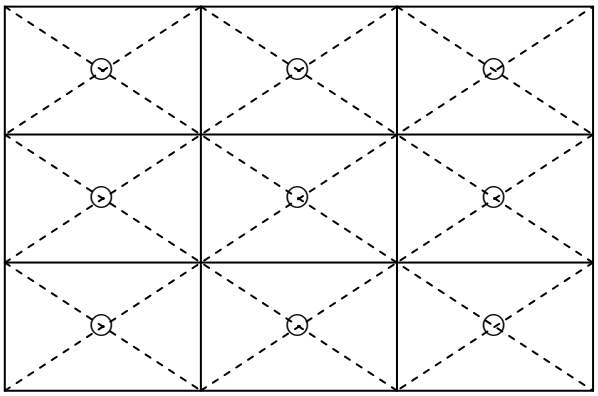
6. RELIABILITY TESTS

Test item		Condition	Judgment Note1
High temperature and humidity (Operation)		① 60 ± 2°C, RH = 60%, 240hours ② Display data is white. Note2	No display malfunctions
Heat cycle (Operation)		① 0 ± 3°C…1hour 60 ± 3°C…1hour ② 50cycles, 4hours/cycle ③ Display data is white. Note2	
Thermal shock (Non operation)		① -20 ± 3°C…30minutes 60 ± 3°C…30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s^2 ② 1 minute/cycle ③ X, Y, Z directions ④ 10 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)		① 294m/s^2, 11ms ② X, Y, Z directions ③ 3 times each directions	
ESD (Operation)		① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note3 ③ 10 times each places at 1 sec interval	No display malfunctions
Low pressure	Non-operation	① 15 kPa (Equivalent to altitude 13,600m) ② -20°C±3°C…24 hours ③ +60°C±3°C…24 hours	No display malfunctions
	Operation	① 53.3 kPa (Equivalent to altitude 5,100m) ② 0°C±3°C…24 hours ③ +60°C±3°C…24 hours Note2	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.

Note2: Luminance: 450cd/m^2 at luminance control.

Note3: See the following figure for discharge points



7. PRECAUTIONS

7.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "7.2 CAUTIONS" and "7.3 ATTENTIONS"!**

This sign has the meaning that a customer will be injured or the product will sustain damage if the customer practices wrong operations.

This sign has the meaning that a customer will be injured if the customer practices wrong operations.

7.2 CAUTIONS

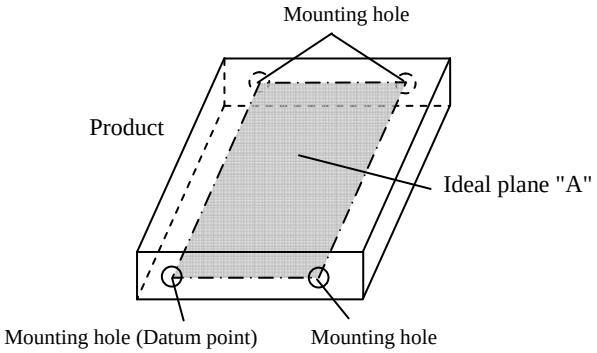
- **Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: Equal to or no greater than 294m/s^2 and equal to or no greater than 11ms, Pressure: Equal to or no greater than 19.6N (ϕ16mm jig))**

7.3 ATTENTIONS

7.3.1 Handling of the product

① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
② Do not hook nor pull cables such as lamp cable, and so on, in order to avoid any damage.
③ When the product is put on the table temporarily, display surface must be placed downward.
④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
⑤ The torque for product mounting screws must never exceed 0.735N·m. Higher torque might result in distortion of the bezel. And the length of product mounting screws must be ≤ 5.0mm.

⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura.
Recommended installing method: Ideal plane "A" is defined by one mounting hole (datum point) and other mounting holes. The ideal plane "A" should be the same plane within ±0.3 mm.



⑦ Do not press or rub on the sensitive product surface. When cleaning the product surface, wipe it with a soft dry cloth.
⑧ Do not push or pull the interface connectors while the product is working.
⑨ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.
⑩ Usually liquid crystals don't leak through the breakage of glasses because of the surface tension of thin layer and the construction of LCD panel. But, if you contact with liquid crystal by any chance, please wash it away with soap and water.

7.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
② In order to prevent dew condensation occurred by temperature difference, the product packing box must be opened after enough time being left under the environment of an unpacking room. Evaluate the storage time sufficiently because dew condensation is affected by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with the original packing state after a customer receives the package)
③ Do not operate in high magnetic field. If not, circuit boards may be broken.
④ This product is not designed as radiation hardened.

7.3.3 Characteristics

The following items are neither defects nor failures.

① Response time, luminance and color may be changed by ambient temperature.
② Display mura, flickering, vertical streams or tiny spots may be observed depending on display patterns.
③ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
④ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
⑤ Optical characteristics may be changed depending on input signal timings.

7.3.4 Others

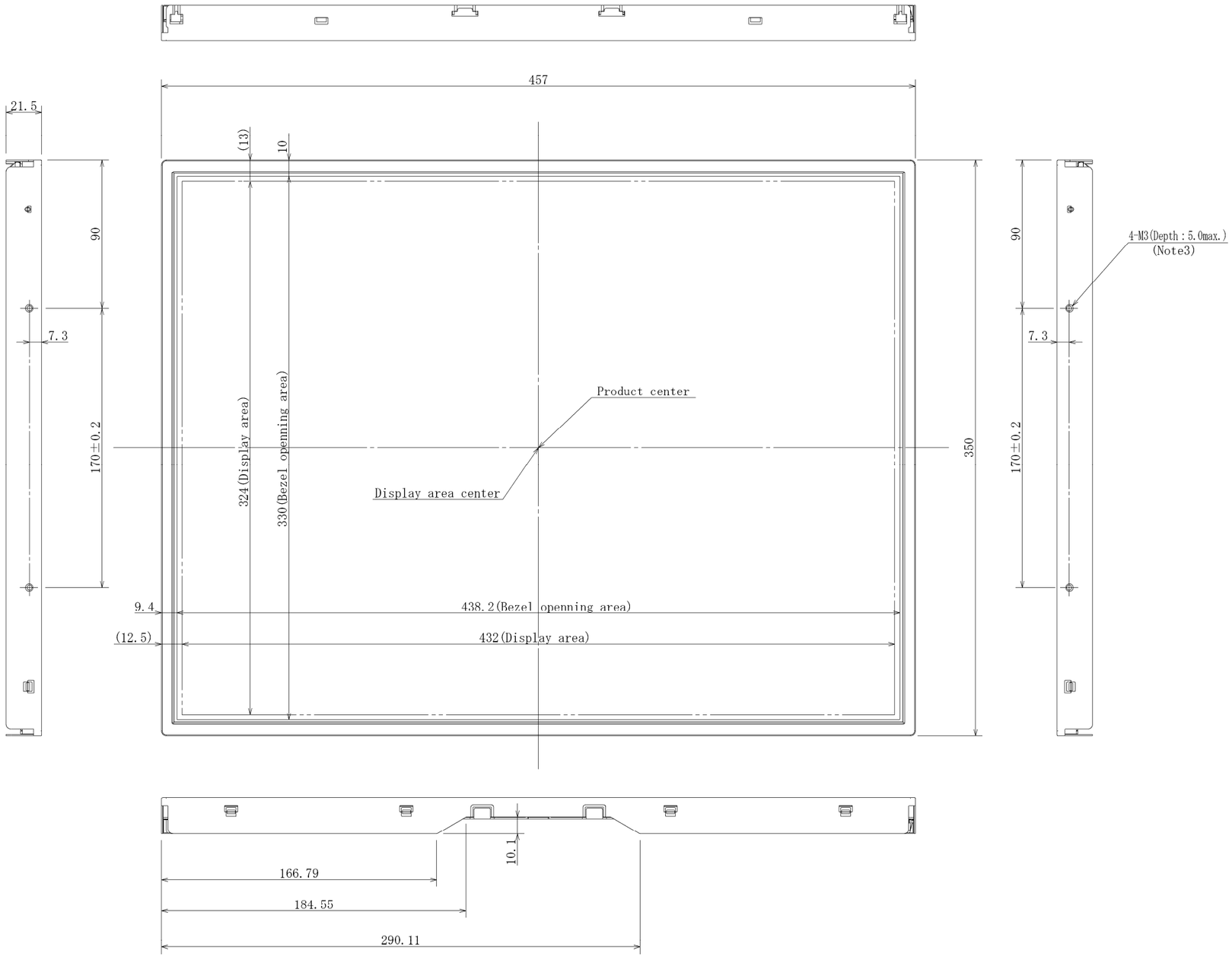
① All GND, GNDB, VDD and VDDB terminals should be used without any non-connected lines.
② Do not disassemble a product or adjust variable resistors.
③ Pack the product with the original shipping package, in order to avoid any damages during transportation, when returning the product to NLT for repairing and so on.
④ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.
⑤ The information of China RoHS directive six hazardous substances or elements in this product is as follows. ☆

China RoHS directive six l hazardous substances or elements					
Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr VI)	Polybrominated Biphenys (PBB)	Polybrominated Biphenyl Ethers (PBDE)
×	○	○	○	○	○

Note1: ○: This indicates that the poisonous or harmful material in all the homogeneous materials for this part is equal or below the limitation level of SJ/T11363-2006 standard regulation.
×: This indicates that the poisonous or harmful material in all the homogeneous materials for this part is above the limitation level of SJ/T11363-2006 standard regulation.

8. OUTLINE DRAWINGS

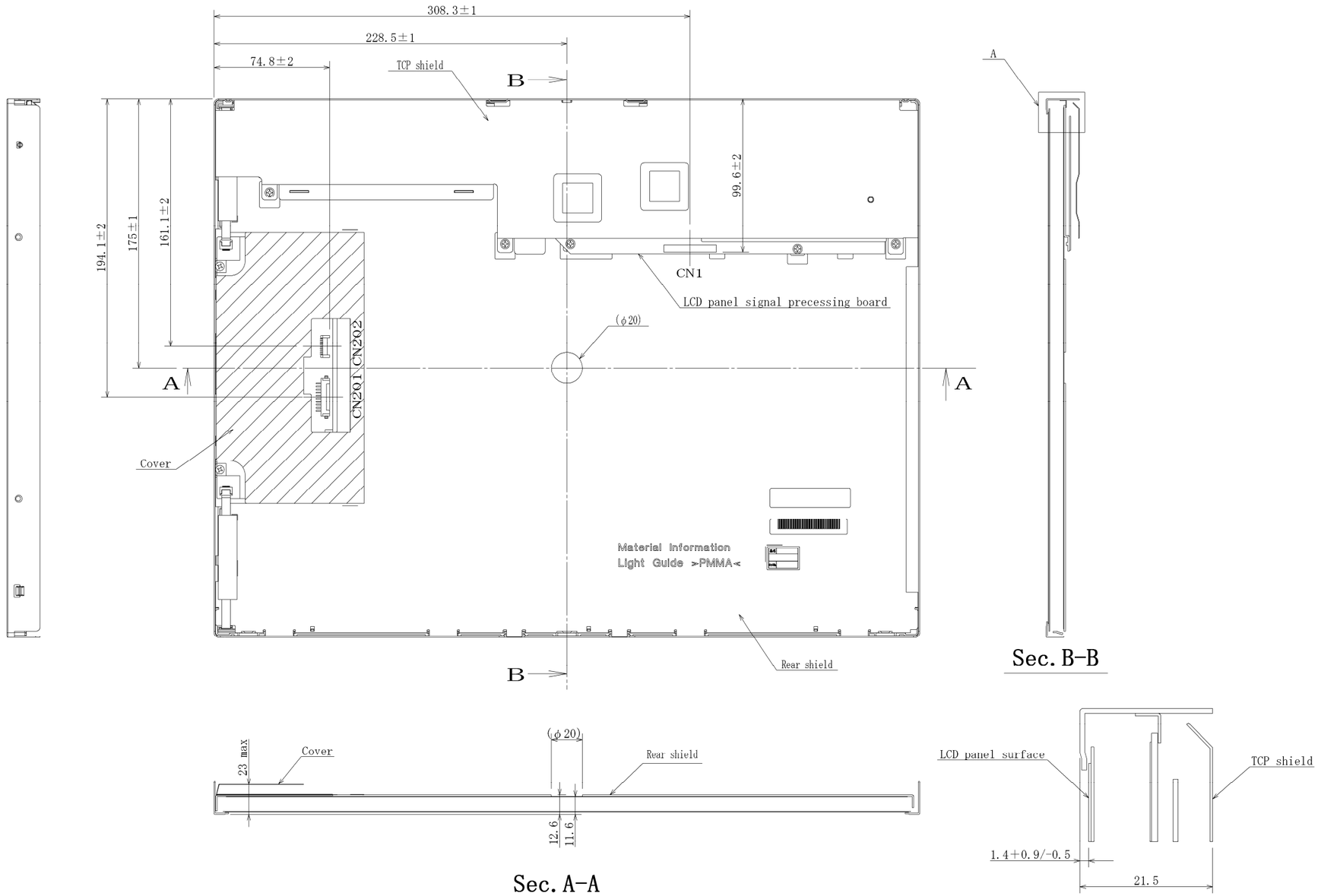
8.1 FRONT VIEW



Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for product mounting screws must never exceed 0.735N·m.
Note3: The length of product mounting screws from surface of plate must be ≤ 5.0mm.
Note4: The values in parentheses are for reference.

Unit: mm

8.2 REAR VIEW



Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for product mounting screws must never exceed 0.735N·m.
Note3: The length of product mounting screws from surface of plate must be ≤ 5.0mm.
Note4: The values in parentheses are for reference.

Unit: mm