NEC

TFT MONOCHROME LCD MODULE

NL160120BM27-xx

54cm (21.3 Type)
UXGA

PRELIMINARY DATA SHEET

(1st edition)

All information is subject to change without notice.
Please confirm the delivery specification before starting to design your system.

INTRODUCTION

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Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Military systems, aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems (medical equipment, etc.) and any other equipment

The quality grade of this product is ***"Standard"*** unless otherwise specified in this document. If customers intend to use this product for applications other than those specified for ***"Standard"*** quality grade, they should contact NEC Corporation sales representative in advance.

Anti-radioactive design is not implemented in this product.

CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

NL160120BM27-xx module is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a monochrome-filter glass substrate.

Grayscale data signals from a host system (e.g. PC, signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Monochrome images are created by regulating the amount of transmitted light through the TFT array.

1.2 APPLICATIONS

- EWS monitors
- Monitors for CAD system
- Monitors for medical system

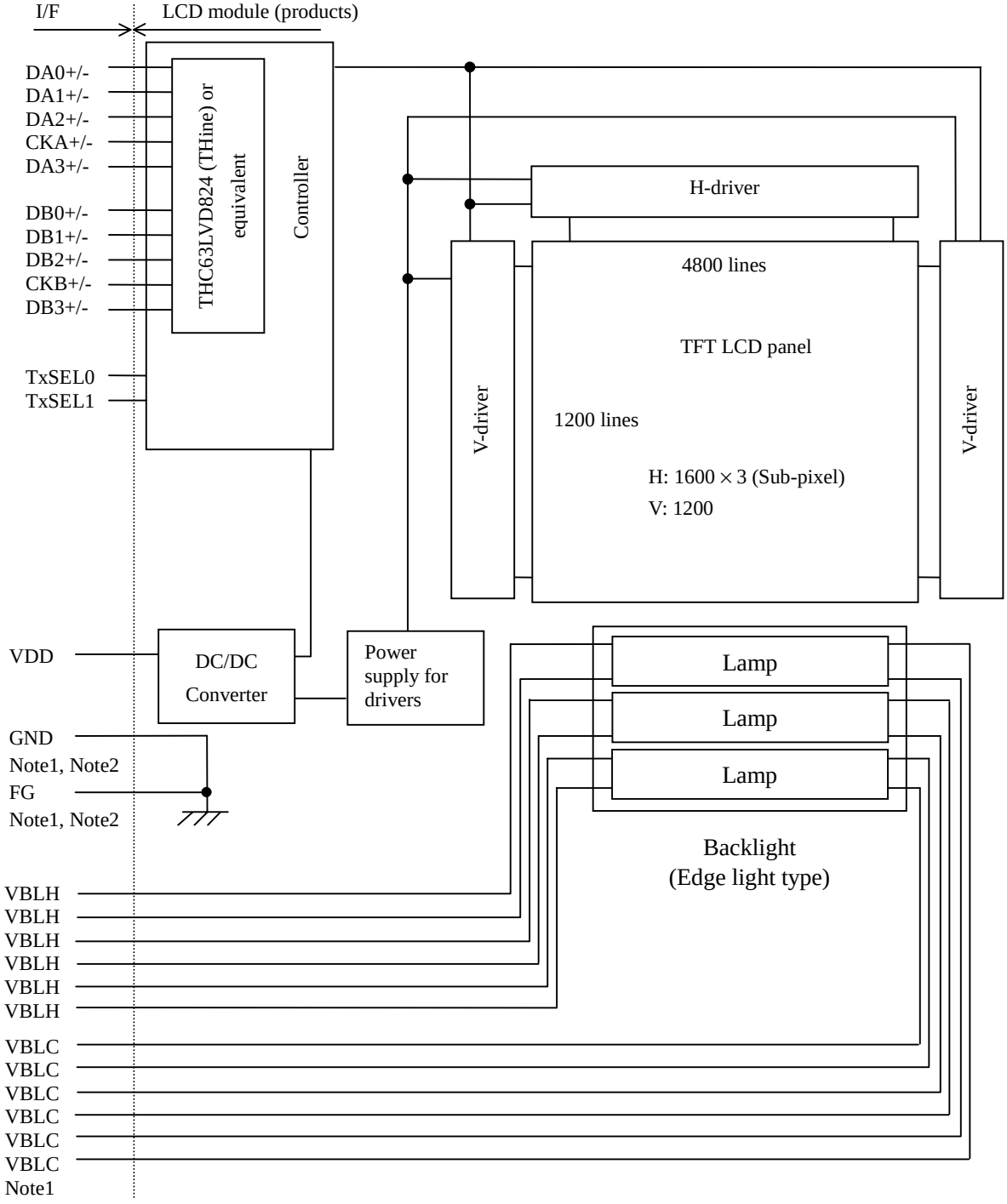
1.3 FEATURES

- Ultra-wide viewing angle (with lateral electric field)
- High resolution
- Low reflection
- LVDS interface
- High luminance
- Small foot print
- Incorporated edge light type backlight

2. GENERAL SPECIFICATIONS

Display area	432.0 (W) × 324.0 (H) mm (typ.)
Diagonal size of display	54 cm (21.3 inches)
Drive system	a-Si TFT active matrix
Display grayscale	256
Pixel	1600 (H) × 1200 (V) pixels
Pixel arrangement	Sub-pixel vertical stripe
Dot pitch	0.090 (W) × 0.270 (H) mm
Pixel pitch	0.270 (W) × 0.270 (H) mm
Module size	457.0 (W) × 350.0 (H) × 25.0 (D) mm (typ.)
Weight	(4000) g (typ.)
Contrast ratio	700:1 (typ.)
Viewing angle	*At the contrast ratio 10:1* • Horizontal: Right side 85° (typ.), Left side 85° (typ.) • Vertical: Up side 85° (typ.), Down side 85° (typ.)
Designed viewing direction	Viewing angle with optimum grayscale (γ=2.2): normal axis
Polarizer surface	TBD
Polarizer pencil-hardness	TBD H (min.) [by JIS K5400]
Response time	*Ton + Toff* (25) ms (typ.)
Luminance	*At IBL= 6.0mArms / lamp* 800 cd/m^2 (typ.)
Signal system	2 ports LVDS interface (THC63LVD824 THine Electronics, Inc.) LCR 8-bit signals, Data enable signal (DE), Dot clock (CLK)
Power supply voltage	LCD panel signal processing board: 12.0V
Backlight	Edge light type: 6 cold cathode fluorescent lamps
Power consumption	*At checkered flag pattern and IBL= 6.0mArms / lamp* TBD W (typ.)

3. BLOCK DIAGRAM



Note1: Connections between GND (Signal ground), FG (Frame ground) and VBLC (Lamp low voltage terminal) in the LCD module

GND - FG	Connected
GND - VBLC	Not connected
FG - VBLC	Not connected

Note2: These grounds should be connected together in customer equipment.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification		Unit
Module size	457.0 ± 1.0 (W) × 350.0 ± 1.0 (H) × 25.0 ± 0.5 (D)	Note1	mm
Display area	432.0 (W) × 324.0 (H)	Note1	mm
Weight	(4000) (typ.), (4200) (max.)		g

Note1: See "**7. OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board	VDD	-0.3 to +14.0	V	Ta = 25°C
	Lamp voltage	VBLH	TBD	Vrms	
Input voltage for signals	Display signals Note1	VD	-0.3 to +3.6	V	Ta = 25°C VDD=12.0V
	Function signals Note2	VF	-0.3 to +3.6	V	
Storage temperature		Tst	-20 to +60	°C	-
Operating temperature	Front surface	TopF	0 to +TBD	°C	Note3
	Rear surface	TopR	0 to + TBD	°C	Note4
Relative humidity Note5		RH	≤ 95	%	Ta ≤ 40°C
			≤ 85	%	40 < Ta ≤ 50°C
			≤ 70	%	50 < Ta ≤ 55°C
Absolute humidity Note5		AH	≤ 73 Note6	g/m^3	Ta > 55°C

Note1: Display signals are DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/- and CKB+/-.
Note2: Function signals are TxSEL0 and TxSEL1.
Note3: Measured at center of LCD panel surface (including self-heat)
Note4: Measured at center of LCD module's rear shield surface (including self-heat)
Note5: No condensation
Note6: Ta = 55°C, RH = 70%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 Driving for LCD panel signal processing board

(Ta = 25°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks
Power supply voltage		VDD	10.8	12.0	13.2	V	-
Power supply current		IDD	-	(550) Note1	TBD Note2	mA	at VDD = 12.0V
Differential input threshold voltage for Display signals	Low	VTL	-100	-	-	mV	at VCM= 1.2V Note3
	High	VTH	-	-	+100	mV	
Terminating resister		RT	-	100	-	Ω	-
Input voltage for Function signals	Low	VFL	-	-	0.5	V	TxSEL0, TxSEL1 Note4
Input current for Function signals	Low	IFL	-10	-	10	μA	

Note1: Checkered flag pattern [by EIAJ ED-2522]
Note2: Pattern for maximum current
Note3: Common mode voltage for LVDS receiver
Note4: High must be Open.

4.3.2 Driving for backlight lamp

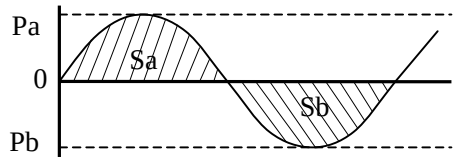
(Ta=25°C Note1)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Lamp current	IBL	TBD	(6.0)	TBD	mArms	at IBL=6.0mArms: 250cd/m^2 Note3
Lamp voltage	VBLH	-	(800)	-	Vrms	Note2, Note3
Lamp starting voltage	VS	(1000)	-	-	Vrms	Ta = 25°C Note2, Note3
		(1300)	-	-	Vrms	Ta = 0°C Note2, Note3
Oscillation frequency	FO	TBD	(56)	TBD	kHz	Note4

Note1: This product consists of 6 backlight lamps, and these specifications are for each lamp.

Note2: The lamp voltage cycle between lamps should be kept on a same phase. "VS" and "VBLH" are the voltage value between low voltage side (Cold) and high voltage side (Hot).

Note3: The asymmetric ratio of working waveform for lamps (Lamp voltage peak ratio, Lamp current peak ratio and waveform space ratio) should be less than 5 % (See the following figure.). If the waveform is asymmetric, DC (Direct current) element apply into the lamp. In this case, a lamp lifetime may be shortened, because a distribution of a lamp enclosure substance inclines toward one side between low voltage terminal (Cold terminal) and high voltage terminal (Hot terminal).



$$\frac{|Pa - Pb|}{Pb} \times 100 \leq 5\ \%$$

$$\frac{|Sa - Sb|}{Sb} \times 100 \leq 5\ \%$$

Pa: Supply voltage/current peak for positive, Pb: Supply voltage/current peak for negative
Sa: Waveform space for positive part, Sb: Waveform space for negative part

Note4: In case "FO" is not the recommended value, beat noise may display on the screen, because of interference between "FO" and "1/th". Recommended value of "FO" is as following.

$$FO = \frac{1}{4} \times \frac{1}{th} \times (2n\text{-}1)$$

th: Horizontal cycle period (See "**4.10.1 Input signal timings**".)
n: Natural number (1, 2, 3 ·····)

Note5: Method of lamp cable installation may invite fluctuation of lamp current and voltage or asymmetric of lamp working waveform. When design the backlight inverter, evaluate the fluctuation of lamp current and voltage or asymmetric of lamp working waveform sufficiently.

4.3.3 Power supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Parameter	Power supply voltage	Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VDD	12.0 V	≤ 100	mVp-p

Note1: The permissible ripple voltage includes spike noise.

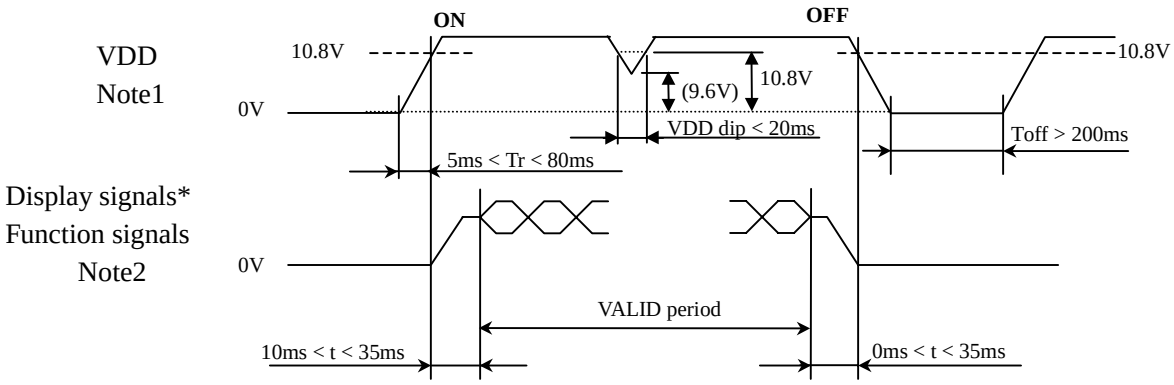
4.3.4 Fuses

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	TBD	TBD	TBD A TBD V	TBD A	Note1

Note1: The power supply capacity should be more than the fusing current. If the power supply capacity is less than the fusing current, the fuse may not blow for a short time, and then nasty smell, smoking and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 Sequence for LCD panel signal processing board



* These signals should be measured at the terminal of 100Ω resistor.

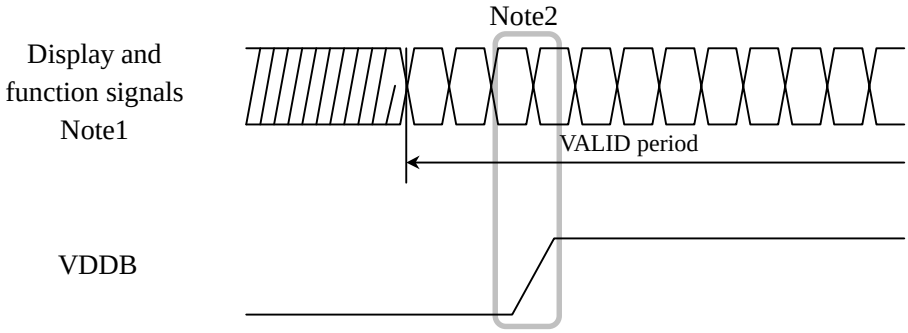
Note1: In terms of voltage variation (voltage drop) while VDD rising edge is below 10.8V, a protection circuit may work, and then this product may not work.

Note2: Display (DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/- and CKB+/-) and function (TxSEL0, TxSEL1) signals must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged.

If some of display and function signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. If customer stops the display and function signals, they should be cut VDD.

Note3: VDD should be (9.6)V or more while VDD ON period.

4.4.2 Sequence for backlight inverter



Note1: These are display and function signals for LCD panel signal processing board.

Note2: The backlight inverter voltage (VDDB) should be inputted within the valid period of display and function signals, in order to avoid unstable data display.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

CN1 socket (LCD module side): DF19G-30P-1H(59) (Hirose Electric Co., Ltd.)
Adaptable plug: DF19-30S-1C (Hirose Electric Co., Ltd.)

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function</th><th colspan="4">Description</th></tr>
<tr><td>1</td><td>DA0-</td><td rowspan="2">Odd pixel data 0</td><td colspan="4" rowspan="6">LVDS differential signal Note1</td></tr>
<tr><td>2</td><td>DA0+</td></tr>
<tr><td>3</td><td>DA1-</td><td rowspan="2">Odd pixel data 1</td></tr>
<tr><td>4</td><td>DA1+</td></tr>
<tr><td>5</td><td>DA2-</td><td rowspan="2">Odd pixel data 2</td></tr>
<tr><td>6</td><td>DA2+</td></tr>
<tr><td>7</td><td>GND</td><td>-</td><td colspan="4">Connect to system ground.</td></tr>
<tr><td>8</td><td>CKA-</td><td rowspan="2">Odd pixel clock</td><td colspan="4" rowspan="6">LVDS differential signal Note1</td></tr>
<tr><td>9</td><td>CKA+</td></tr>
<tr><td>10</td><td>DA3-</td><td rowspan="2">Odd pixel data 3</td></tr>
<tr><td>11</td><td>DA3+</td></tr>
<tr><td>12</td><td>DB0-</td><td rowspan="2">Even pixel data 0</td></tr>
<tr><td>13</td><td>DB0+</td></tr>
<tr><td>14</td><td>GND</td><td>-</td><td colspan="4">Connect to system ground.</td></tr>
<tr><td>15</td><td>DB1-</td><td rowspan="2">Even pixel data 1</td><td colspan="4" rowspan="2">LVDS differential signal Note1</td></tr>
<tr><td>16</td><td>DB1+</td></tr>
<tr><td>17</td><td>GND</td><td>-</td><td colspan="4">Connect to system ground.</td></tr>
<tr><td>18</td><td>DB2-</td><td rowspan="2">Even pixel data 2</td><td colspan="4" rowspan="6">LVDS differential signal Note1</td></tr>
<tr><td>19</td><td>DB2+</td></tr>
<tr><td>20</td><td>CKB-</td><td rowspan="2">Even pixel clock</td></tr>
<tr><td>21</td><td>CKB+</td></tr>
<tr><td>22</td><td>DB3-</td><td rowspan="2">Even pixel data 3</td></tr>
<tr><td>23</td><td>DB3+</td></tr>
<tr><td>24</td><td>GND</td><td>-</td><td colspan="4">Connect to system ground.</td></tr>
<tr><td rowspan="2">25</td><td rowspan="2">TxSEL0</td><td rowspan="4">Selection of LVDS input mode</td><td colspan="4">Note2, Note3</td></tr>
<tr><td>TxSEL0</td><td>TxSEL1</td><td>Mode</td></tr>
<tr><td rowspan="2">26</td><td rowspan="2">TxSEL1</td><td>High</td><td>High</td><td>A</td></tr>
<tr><td>High</td><td>Low</td><td>B</td></tr>
<tr><td>27</td><td>GND</td><td>-</td><td>Low</td><td>High</td><td>C</td></tr>
<tr><td>28</td><td rowspan="3">VDD</td><td rowspan="3">Power supply</td><td>Low</td><td>Low</td><td>A</td></tr>
<tr><td>Connect to system ground.</td><td colspan="3">-</td></tr>
<tr><td>29</td></tr>
<tr><td>30</td></tr>
</table>

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be connected between LCD panel signal processing board and LVDS transmitter.

Note2: This terminal is pulled-up in the product. High must be open.

Note3: See "**4.6 LVDS INPUT MODE**".

4.5.2 Backlight lamp

Attention: VBLH and VBLC must be connected correctly. If customer connects wrongly, customer will be hurt and the module will be broken.

CN201 plug (Module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)
Adaptable socket: SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH1	Upper side lamp, High voltage (Hot)	Cable color: Pink
2	VBLC1	Upper side lamp, Low voltage (Cold)	Cable color: Gray

CN202 plug (Module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)
Adaptable socket: SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH2	Upper side lamp, High voltage (Hot)	Cable color: White
2	VBLC2	Upper side lamp, Low voltage (Cold)	Cable color: Gray

CN203 plug (Module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)
Adaptable socket: SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH3	Upper side lamp, High voltage (Hot)	Cable color: Pink
2	VBLC3	Upper side lamp, Low voltage (Cold)	Cable color: Gray

CN204 plug (Module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)
Adaptable socket: SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH4	Lower side lamp, High voltage (Hot)	Cable color: Pink
2	VBLC4	Lower side lamp, Low voltage (Cold)	Cable color: Gray

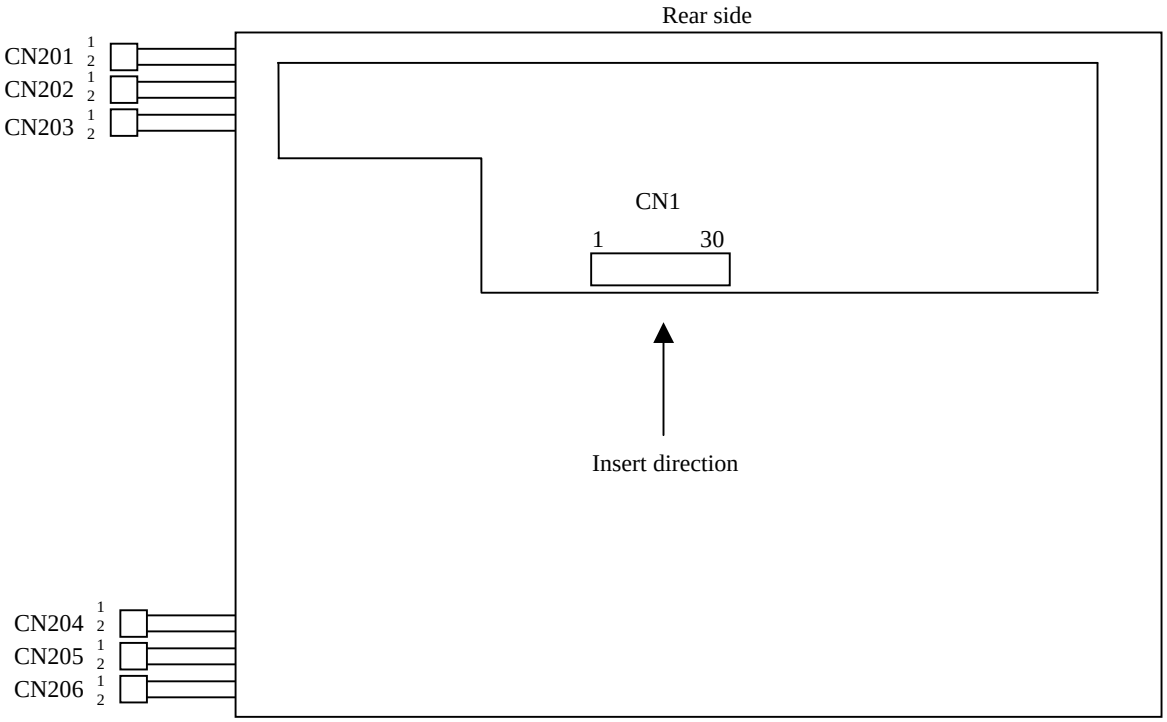
CN205 plug (Module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)
Adaptable socket: SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH5	Lower side lamp, High voltage (Hot)	Cable color: White
2	VBLC5	Lower side lamp, Low voltage (Cold)	Cable color: Gray

CN206 plug (Module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)
Adaptable socket: SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH6	Lower side lamp, High voltage (Hot)	Cable color: Pink
2	VBLC6	Lower side lamp, Low voltage (Cold)	Cable color: Gray

4.5.3 Positions of plug and a socket



4.6 LVDS INPUT MODE

4.6.1 Mode A

Input data			Transmitter Pin	THC63LVDF83A		Transmitter Pin	THC63LVD823			I/F Pin	I/F CN1			THC63LVD824 or equivalent
Odd pixel data and control signal	LA2	→	51	TA0		53	L12							
	LA3	→	52	TA1		54	L13	TA1-	→	1	DA0-	→		RA-1
	LA4	→	54	TA2		57	L14	TA1+	→	2	DA0+	→		RA+1
	LA5	→	55	TA3		58	L15							
	LA6	→	56	TA4		59	L16	TB1-	→	3	DA1-	→		RB-1
	LA7	→	3	TA5		60	L17	TB1+	→	4	DA1+	→		RB+1
	CA2	→	4	TA6		63	C12							
	CA3	→	6	TB0		64	C13	TC1-	→	5	DA2-	→		RC-1
	CA4	→	7	TB1		65	C14	TC1+	→	6	DA2+	→		RC+1
	CA5	→	11	TB2		66	C15			7	GND			
	CA6	→	12	TB3		67	C16	TCLK1-	→	8	CKA-	→		RCLK-1
	CA7	→	14	TB4		68	C17	TCLK1+	→	9	CKA+	→		RCLK+1
	RA2	→	15	TB5		73	R12							
	RA3	→	19	TB6		74	R13	TD1-	→	10	DA3-	→		RD-1
	RA4	→	20	TC0	1st	75	R14	TD1+	→	11	DA3+	→		RD+1
	RA5	→	22	TC1		76	R15							
	RA6	→	23	TC2		77	R16							
	RA7	→	24	TC3		78	R17							
	RSVD	→	27	TC4		7	RSVD							
	RSVD	→	28	TC5		8	RSVD							
	DE	→	30	TC6		9	DE							
	LA0	→	50	TD0		51	L10							
	LA1	→	2	TD1		52	L11							
	CA0	→	8	TD2		61	C10							
	CA1	→	10	TD3		62	C11							
	RA0	→	16	TD4		69	R10							
	RA1	→	18	TD5		70	R11							
	RSVD	→	25	TD6		-								
	CLK	→	31	CLKIN		10	CLK							
Even pixel data	LB2	→	51	TA0		81	L22							
	LB3	→	52	TA1		82	L23	TA2-	→	12	DB0-	→		RA-2
	LB4	→	54	TA2		83	L24	TA2+	→	13	DB0+	→		RA+2
	LB5	→	55	TA3		84	L25			14	GND			
	LB6	→	56	TA4		85	L26	TB2-	→	15	DB1-	→		RB-2
	LB7	→	3	TA5		86	L27	TB2+	→	16	DB1+	→		RB+2
	CB2	→	4	TA6		91	C22			17	GND			
	CB3	→	6	TB0		92	C23	TC2-	→	18	DB2-	→		RC-2
	CB4	→	7	TB1		93	C24	TC2+	→	19	DB2+	→		RC+2
	CB5	→	11	TB2		94	C25							
	CB6	→	12	TB3		95	C26	TCLK2-	→	20	CKB-	→		RCLK-2
	CB7	→	14	TB4		96	C27	TCLK2+	→	21	CKB+	→		RCLK+2
	RB2	→	15	TB5		99	R22							
	RB3	→	19	TB6		100	R23	TD2-	→	22	DB3-	→		RD-2
	RB4	→	20	TC0	2nd	1	R24	TD2+	→	23	DB3+	→		RD+2
	RB5	→	22	TC1		2	R25			24	GND			
	RB6	→	23	TC2		5	R26			25	TxSEL0	→		TxSEL0
	RB7	→	24	TC3		6	R27			26	TxSEL1	→		TxSEL1
	RSVD	→	27	TC4		-				27	GND			
	RSVD	→	28	TC5		-				28	VDD			
	RSVD	→	30	TC6		-				29	VDD			
	LB0	→	50	TD0		79	L20			30	VDD			
	LB1	→	2	TD1		80	L21							
	CB0	→	8	TD2		89	C20							
	CB1	→	10	TD3		90	C21							
	RB0	→	16	TD4		97	R20							
	RB1	→	18	TD5		98	R21							
	RSVD	→	25	TD6		-								
	CLK	→	31	CLKIN		-								

Note1: RSVD must be connected to system ground

4.6.2 Mode B

Input data			Transmitter Pin	DS90CF383, C385			I/F Pin	I/F CN1		THC63LVD824 or equivalent
Odd pixel data and control signal	LA2	→	51	TXIN0						
	LA3	→	52	TXIN1		TA1- →	1	DA0-	→	RA-1
	LA4	→	54	TXIN2		TA1+ →	2	DA0+	→	RA+1
	LA5	→	55	TXIN3						
	LA6	→	56	TXIN4		TB1- →	3	DA1-	→	RB-1
	LA7	→	3	TXIN6		TB1+ →	4	DA1+	→	RB+1
	CA2	→	4	TXIN7						
	CA3	→	6	TXIN8		TC1- →	5	DA2-	→	RC-1
	CA4	→	7	TXIN9		TC1+ →	6	DA2+	→	RC+1
	CA5	→	11	TXIN12			7	GND		
	CA6	→	12	TXIN13		TCLK1- →	8	CKA-	→	RCLK-1
	CA7	→	14	TXIN14		TCLK1+ →	9	CKA+	→	RCLK+1
	RA2	→	15	TXIN15						
	RA3	→	19	TXIN18		TD1- →	10	DA3-	→	RD-1
	RA4	→	20	TXIN19	1st	TD1+ →	11	DA3+	→	RD+1
	RA5	→	22	TXIN20						
	RA6	→	23	TXIN21						
	RA7	→	24	TXIN22						
	RSVD	→	27	TXIN24						
	RSVD	→	28	TXIN25						
	DE	→	30	TXIN26						
	LA0	→	50	TXIN27						
	LA1	→	2	TXIN5						
	CA0	→	8	TXIN10						
	CA1	→	10	TXIN11						
	RA0	→	16	TXIN16						
	RA1	→	18	TXIN17						
	RSVD	→	25	TXIN23						
	CLK	→	31	CLKIN						
Even pixel data	LB2	→	51	TXIN0						
	LB3	→	52	TXIN1		TA2- →	12	DB0-	→	RA-2
	LB4	→	54	TXIN2		TA2+ →	13	DB0+	→	RA+2
	LB5	→	55	TXIN3			14	GND		
	LB6	→	56	TXIN4		TB2- →	15	DB1-	→	RB-2
	LB7	→	3	TXIN6		TB2+ →	16	DB1+	→	RB+2
	CB2	→	4	TXIN7			17	GND		
	CB3	→	6	TXIN8		TC2- →	18	DB2-	→	RC-2
	CB4	→	7	TXIN9		TC2+ →	19	DB2+	→	RC+2
	CB5	→	11	TXIN12						
	CB6	→	12	TXIN13		TCLK2- →	20	CKB-	→	RCLK-2
	CB7	→	14	TXIN14		TCLK2+ →	21	CKB+	→	RCLK+2
	RB2	→	15	TXIN15						
	RB3	→	19	TXIN18		TD2- →	22	DB3-	→	RD-2
	RB4	→	20	TXIN19	2nd	TD2+ →	23	DB3+	→	RD+2
	RB5	→	22	TXIN20			24	GND		
	RB6	→	23	TXIN21			25	TxSEL0	→	TxSEL0
	RB7	→	24	TXIN22			26	TxSEL1	→	TxSEL1
	RSVD	→	27	TXIN24			27	GND		
	RSVD	→	28	TXIN25			28	VDD		
	RSVD	→	30	TXIN26			29	VDD		
	LB0	→	50	TXIN27			30	VDD		
	LB1	→	2	TXIN5						
	CB0	→	8	TXIN10						
	CB1	→	10	TXIN11						
	RB0	→	16	TXIN16						
	RB1	→	18	TXIN18						
	RSVD	→	25	TXIN23						
	CLK	→	31	CLKIN						

Note1: RSVD must be connected to system ground

4.6.3 Mode C

Input data			Transmitter Pin	DS90CF383, C385			I/F Pin	CN1		THC63LVD824 or equivalent
Odd pixel data and control signal	LA2	→	51	TXIN0						
	LA3	→	52	TXIN1		TA1- →	1	DA0-	→	RA-1
	LA4	→	54	TXIN2		TA1+ →	2	DA0+	→	RA+1
	LA5	→	55	TXIN3						
	LA6	→	56	TXIN4		TB1- →	3	DA1-	→	RB-1
	LA7	→	3	TXIN6		TB1+ →	4	DA1+	→	RB+1
	CA2	→	4	TXIN7						
	CA3	→	6	TXIN8		TC1- →	5	DA2-	→	RC-1
	CA4	→	7	TXIN9		TC1+ →	6	DA2+	→	RC+1
	CA5	→	11	TXIN12			7	GND		
	CA6	→	12	TXIN13		TCLK1- →	8	CKA-	→	RCLK-1
	CA7	→	14	TXIN14		TCLK1+ →	9	CKA+	→	RCLK+1
	RA2	→	15	TXIN15						
	RA3	→	19	TXIN18		TD1- →	10	DA3-	→	RD-1
	RA4	→	20	TXIN19	1st	TD1+ →	11	DA3+	→	RD+1
	RA5	→	22	TXIN20						
	RA6	→	23	TXIN21						
	RA7	→	24	TXIN22						
	RSVD	→	27	TXIN24						
	RSVD	→	28	TXIN25						
	DE	→	30	TXIN26						
	LA0	→	50	TXIN27						
	LA1	→	2	TXIN5						
	CA0	→	8	TXIN10						
	CA1	→	10	TXIN11						
	RA0	→	16	TXIN16						
	RA1	→	18	TXIN17						
	RSVD	→	25	TXIN23						
	CLK	→	31	CLKIN						
Even pixel data	LB2	→	51	TXIN0						
	LB3	→	52	TXIN1		TA2- →	12	DB0-	→	RA-2
	LB4	→	54	TXIN2		TA2+ →	13	DB0+	→	RA+2
	LB5	→	55	TXIN3			14	GND		
	LB6	→	56	TXIN4		TB2- →	15	DB1-	→	RB-2
	LB7	→	3	TXIN6		TB2+ →	16	DB1+	→	RB+2
	CB2	→	4	TXIN7			17	GND		
	CB3	→	6	TXIN8		TC2- →	18	DB2-	→	RC-2
	CB4	→	7	TXIN9		TC2+ →	19	DB2+	→	RC+2
	CB5	→	11	TXIN12						
	CB6	→	12	TXIN13		TCLK2- →	20	CKB-	→	RCLK-2
	CB7	→	14	TXIN14		TCLK2+ →	21	CKB+	→	RCLK+2
	RB2	→	15	TXIN15						
	RB3	→	19	TXIN18		TD2- →	22	DB3-	→	RD-2
	RB4	→	20	TXIN19	2nd	TD2+ →	23	DB3+	→	RD+2
	RB5	→	22	TXIN20			24	GND		
	RB6	→	23	TXIN21			25	TxSEL0	→	TxSEL0
	RB7	→	24	TXIN22			26	TxSEL1	→	TxSEL1
	RSVD	→	27	TXIN24			27	GND		
	RSVD	→	28	TXIN25			28	VDD		
	RSVD	→	30	TXIN26			29	VDD		
	LB0	→	50	TXIN27			30	VDD		
	LB1	→	2	TXIN5						
	CB0	→	8	TXIN10						
	CB1	→	10	TXIN11						
	RB0	→	16	TXIN16						
	RB1	→	18	TXIN18						
	RSVD	→	25	TXIN23						
	CLK	→	31	CLKIN						

Note1: RSVD must be connected to system ground

4.7 DISPLAY GRAYSCALE AND INPUT DATA SIGNALS

This product can display in 256 grayscale. Also the relation between grayscale and input data signals is as the following table.

Display grayscale		Data signal (0: Low level, 1: High level)																											
		LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
		LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
Left dot grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑					:								:								:			
	↓					:								:								:			
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Center dot grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑					:								:								:			
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	White	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Right dot grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑					:								:								:			
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	White	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

4.8 DISPLAY POSITIONS

The following table is the coordinates per pixel (See "**4.9 SCANNING DIRECTIONS**".).

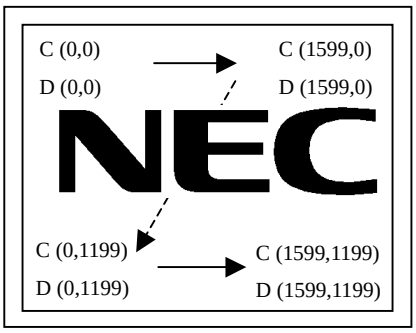
C (0, 0) C (1, 0)

LA	CA	RA	LB	CB	RB

C(0, 0)	C(1, 0)	•••	C(X, 0)	•••	C(1598, 0)	C(1599, 0)
C(0, 1)	C(1, 1)	•••	C(X, 1)	•••	C(1598, 1)	C(1599, 1)
• • •	• • •	• ••• •	• • •	• ••• •	• • •	• ••• •
C(0, Y)	C(1, Y)	•••	C(X, Y)	•••	C(1598, Y)	C(1599, Y)
• • •	• • •	• ••• •	• • •	• ••• •	• • •	• • •
C(0, 1198)	C(1, 1198)	•••	C(X, 1198)	•••	C(1598, 1198)	C(1599, 1198)
C(0, 1199)	C(1, 1199)	•••	C(X, 1199)	•••	C(1598, 1199)	C(1599, 1199)

4.9 SCANNING DIRECTIONS

The following figures are seen from a front view. Also the arrow shows the direction of scan.



Note1

Note1: Meaning of C (X, Y) and D (X, Y)

C (X, Y): The coordinates of the display position (See "**4.8 DISPLAY POSITIONS**".)

D (X, Y): The data number of input signal for LCD panel signal processing board

4.10 INPUT SIGNAL TIMINGS FOR LCD PANEL SIGNAL PROCESSING BOARD

4.10.1 Input signal timings

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency	1/ tc	(60.7) (16.5)	81.0 12.3	82.0 12.2	MHz ns	-
	Duty	tcl / tc	See the data sheet of LVDS transmitter.			-	Note1
	Rise, fall	tcrf				ns	
Horizontal	Cycle period	th	(13.8) (840)	13.3 1080	- -	µs CLK	typ.=75.0kHz Note 2, Note3
	Display period	thd	800			CLK	-
Vertical	Cycle period	tv	- -	16.667 1250	17.24 -	ms H	typ.=60.0Hz
	Display period	tvd	1200			H	-
DATA	DATA-CLK (Set up)	ts	See the data sheet of LVDS transmitter.			ns	Note1
	CLK-DATA (Hold)	th				ns	
	Rise, fall	trf				ns	

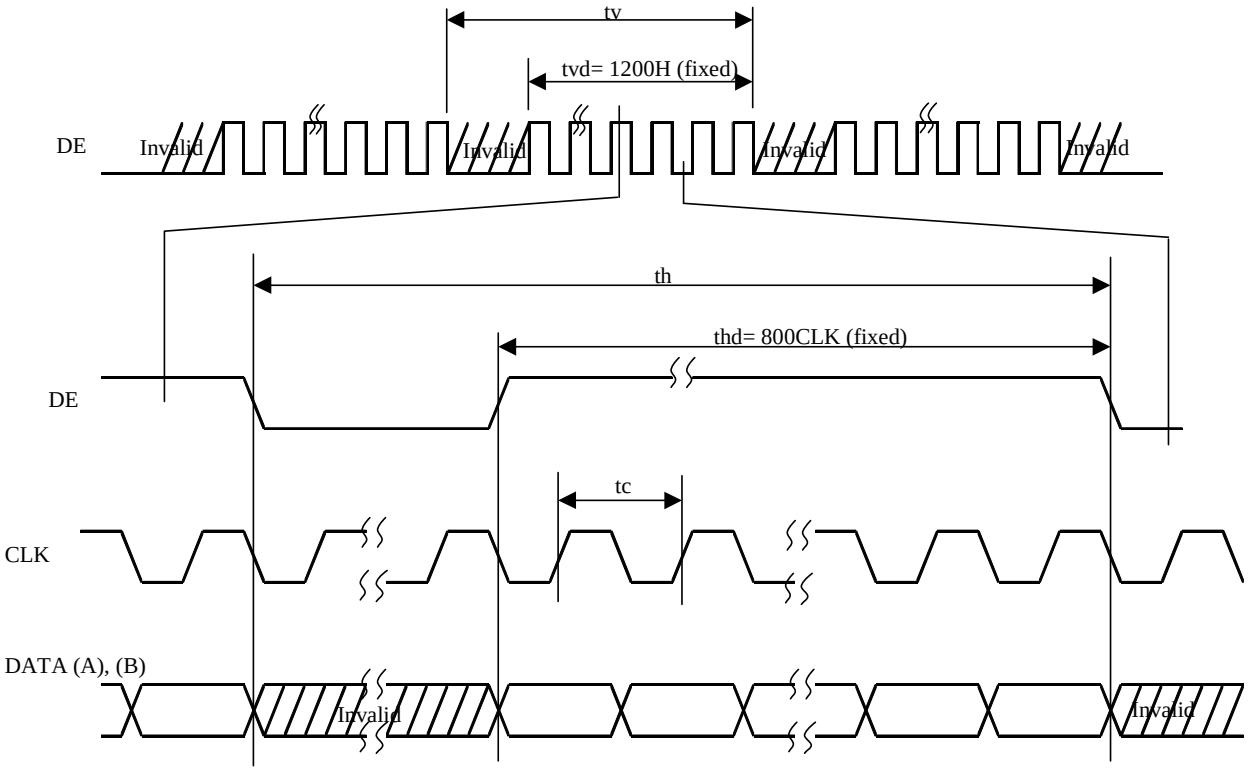
Note1: Timing specifications are defined by the input signals of LVDS transmitter.
THC63LVD824 (THine) or equivalent products are recommended for LVDS transmitter.

Note2: Both of “time” and “CLK number” of the “th” must keep the Minimum value of specification.

Note3: During operation, fluctuation of horizontal cycle period must not exceed ±1 CLK. Otherwise function errors will occur in LCD module.

e.g.: Acceptable fluctuation range is 1079-1081 CLK, when the horizontal cycle period is 1080 CLK.

4.10.2 Input signal timing chart



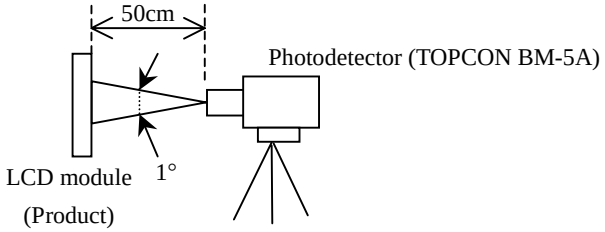
4.11 OPTICS

4.11.1 Optical characteristics

Parameter Note1		Condition	Symbol	Min.	Typ.	Max.	Unit	Remarks
Luminance		White at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	L	TBD	800	-	cd/m^2	-
Contrast ratio		White/Black at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	CR	TBD	700	-	-	Note2
Luminance uniformity		-	LU	-	1.1	1.3	-	Note3
Chromaticity	White	**x** coordinate	Wx	-	TBD	-	-	Note4
		y coordinate	Wy	-	TBD	-	-	
Response time		Black to White	Ton	-	TBD	TBD	ms	Note5 Note6
		White to Black	Toff	-	TBD	TBD	ms	
		Ton + Toff		-	(25)	-	ms	
Viewing angle	Right	θU = 0°, θD = 0°, CR = 10	θR	70	85	-	°	Note7
	Left	θU = 0°, θD = 0°, CR = 10	θL	70	85	-	°	
	Up	θR = 0°, θL = 0°, CR = 10	θU	70	85	-	°	
	Down	θR = 0°, θL = 0°, CR = 10	θD	70	85	-	°	

Note1: Measurement conditions are as follows.
Ta = 25°C, VDD = 12V, IBL = 6.0mArms/lamp, Display mode: UXGA, Horizontal cycle = 75.0kHz, Vertical cycle = 60.0Hz

Optical characteristics are measured at luminance saturation after 20minutes from working the product, in the dark room. Also measurement method for luminance is as follows.



Note2: See "**4.11.2 Definition of contrast ratio**".
Note3: See "**4.11.3 Definition of luminance uniformity**".
Note4: These coordinates are found on CIE 1931 chromaticity diagram.
Note5: Product surface temperature: TopF = TBD°C
Note6: See "**4.11.4 Definition of response times**".
Note7: See "**4.11.5 Definition of viewing angles**".

4.11.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

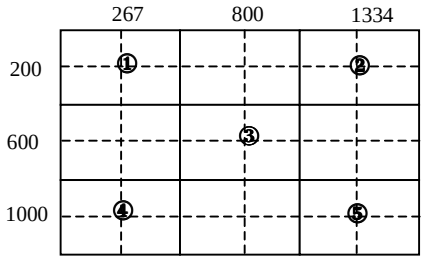
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.11.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

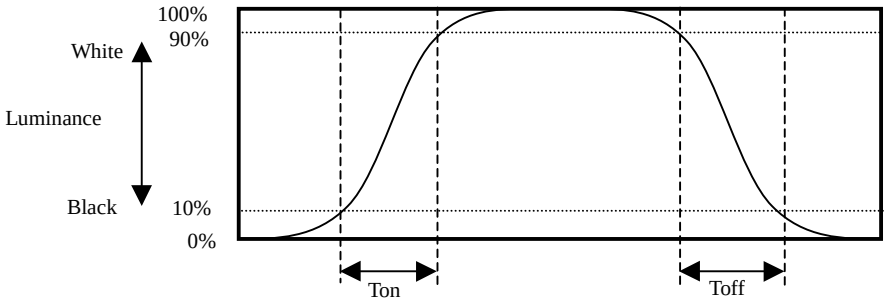
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

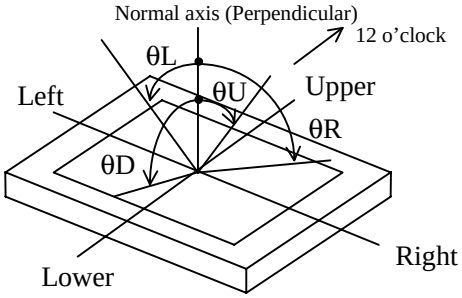


4.11.4 Definition of response times

Response time is measured, the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



4.11.5 Definition of viewing angles

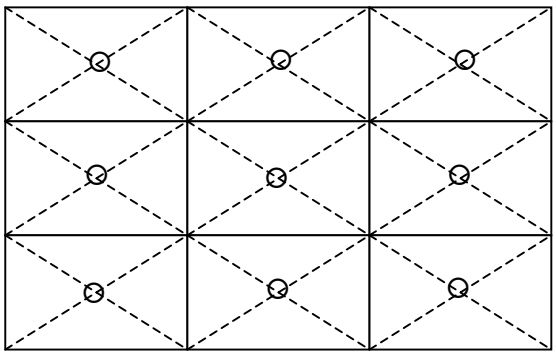


5. RELIABILITY TESTS

Test item		Condition	Judgment
High temperature and humidity (Operation)		① 60 ± 2°C, RH = 60%, 240hours ② Display data is white.	No display malfunctions Note1
Heat cycle (Operation)		① 0 ± 3°C…1hour 55 ± 3°C…1hour ② 50cycles, 4hours/cycle ③ Display data is white.	No display malfunctions Note1
Thermal shock (Non operation)		① -20 ± 3°C…30minutes 60 ± 3°C…30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	No display malfunctions Note1
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s^2 ② 1 minute/cycle ③ X, Y, Z direction ④ 10 times each directions	No display malfunctions Note1 No physical damages
Mechanical shock (Non operation)		① 294m/ s^2, 11ms ② X, Y, Z direction ③ 3 times each directions	No display malfunctions Note1 No physical damages
ESD (Operation)		① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	No display malfunctions Note1
Dust (Operation)		① Sample dust: No.15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	No display malfunctions Note1
Low pressure	operation	① 53.3 kPa ② 0°C±3°C…24 hours ③ +55°C±3°C…24 hours	No display malfunctions Note1
	non-operation	① 15 kPa ② -20°C±3°C…24 hours ③ +60°C±3°C…24 hours	

Note1: Display functions are checked under the same conditions as product inspection.

Note2: See the following figure for discharge points



6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding this contents!**

	This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.
	This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.
	This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS

∗ Do not touch HIGH VOLTAGE PART of the inverter while turn on. Customer will be in danger of an electric shock.

∗ Do not touch the working backlight and IC. Customer will be in danger of burn injury.

∗ Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s^2 and to be not greater 11ms, Pressure: To be not greater 19.6N)

6.3 ATTENTIONS 

6.3.1 Handling of the product

① Take hold of both ends without touch the circuit board cover when customer pulls out products (LCD modules) from inner packing box. If customer touches it, products may be broken down or out of adjustment, because of stress to mounting parts.

② Do not hook cables nor pull connection cables such as lamp cable and so on, for fear of damage.

③ If customer puts down the product temporarily, the product puts on flat subsoil as a display side turns down.

④ Take the measures of electrostatic discharge such as earth band, ionic shower and so on, when customer deals with the product, because products may be damaged by electrostatic.

⑤ The torque for mounting screws must never exceed TBD N·m. Higher torque values might result in distortion of the bezel.

⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area) except mounting hole portion.
Bends or twist described above and undue stress to any portion except mounting hole portion may cause display un-uniformity.

⑦ Do not press or rub on the sensitive display surface. If customer clean on the panel surface, NEC Corporation recommends using the cloth with ethanolic liquid such as screen cleaner for LCD.

⑧ Do not push-pull the interface connectors while the product is working, because wrong power sequence may break down the product.

⑨ Do not bend or unbend the lamp cable at the near part of the lamp holding rubber, to avoid the damage for high voltage side of the lamp. This damage may cause a lamp breaking and abnormal operation of high voltage circuit.

6.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in antistatic pouch in room temperature, because of avoidance for dusts and sunlight, if customer stores the product.
② In order to prevent dew condensation occurring by temperature difference, the product packing box must be opened after leave under the environment of an unpacking room temperature enough. Because a situation of dew condensation occurring is changed by the environmental temperature and humidity, evaluate the leaving time sufficiently. (Recommendation leaving time: 6 hour or more with packing state)
③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
④ Use an original protection sheet on the product surface (polarizer). Adhesive type protection sheet should be avoided, because it may change color or properties of the polarizer.

6.3.3 Characteristics

The following items are neither defects nor failures.

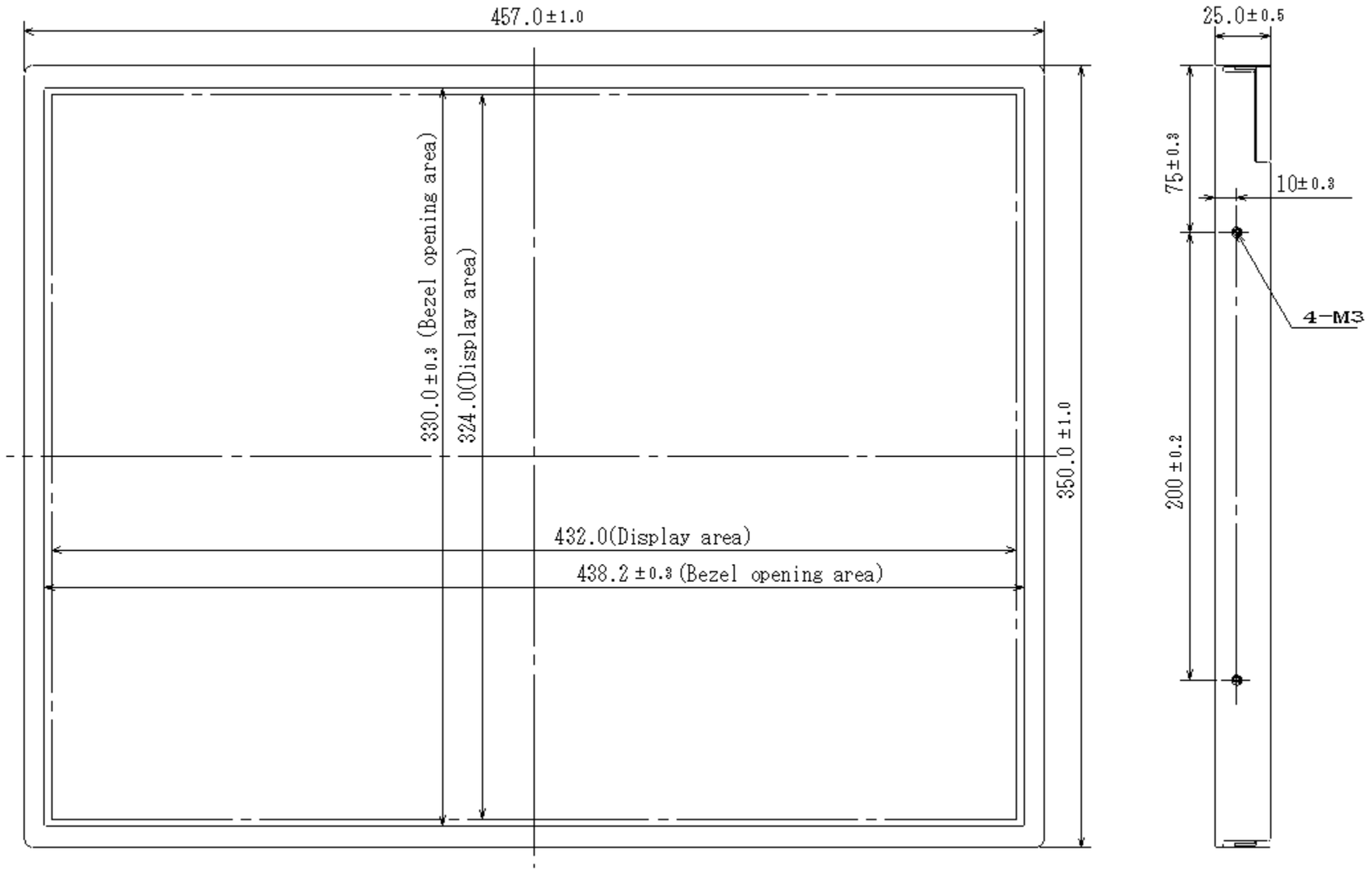
① Response time and luminance may be changed by ambient temperature.
② The LCD may be seemed luminance non-uniformity, flicker, vertical seam or small spot by display patterns.
③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
⑤ Optical characteristics may be changed by input signal timings.
⑥ The interference noise of input signal frequency for this product's signal processing board and luminance control frequency of customer's backlight inverter may appear on a display. Set up luminance control frequency of backlight inverter so that the interference noise does not appear.
⑦ The product may be changed of luminance by voltage variation, even if power source applies recommended voltage to backlight inverter.
⑧ Optical characteristics may be changed by input signal timings.

6.3.4 Other

① All GND, backlight inverter ground (GNDB), VDD and backlight inverter power supply voltage (VDDB) terminals should be used without a non-connected line.
② Do not disassemble a product or adjust volume without permission of NEC Corporation.
③ See "REPLACEMENT MANUAL FOR BACKLIGHT UNIT", if customer would like to replace backlight lamps.
④ Pay attention not to insert waste materials inside of products, if customer uses screwnails.
⑤ Pack the product with original shipping package, because of avoidance of some damages during transportation, when customer returns it to NEC Corporation for repair and so on.
⑥ Not only the module but also the equipment that used the module should be packed and transported as the module becomes vertical. Otherwise, there is the fear that a display dignity decreases by an impact or vibrations."

7. OUTLINE DRAWINGS

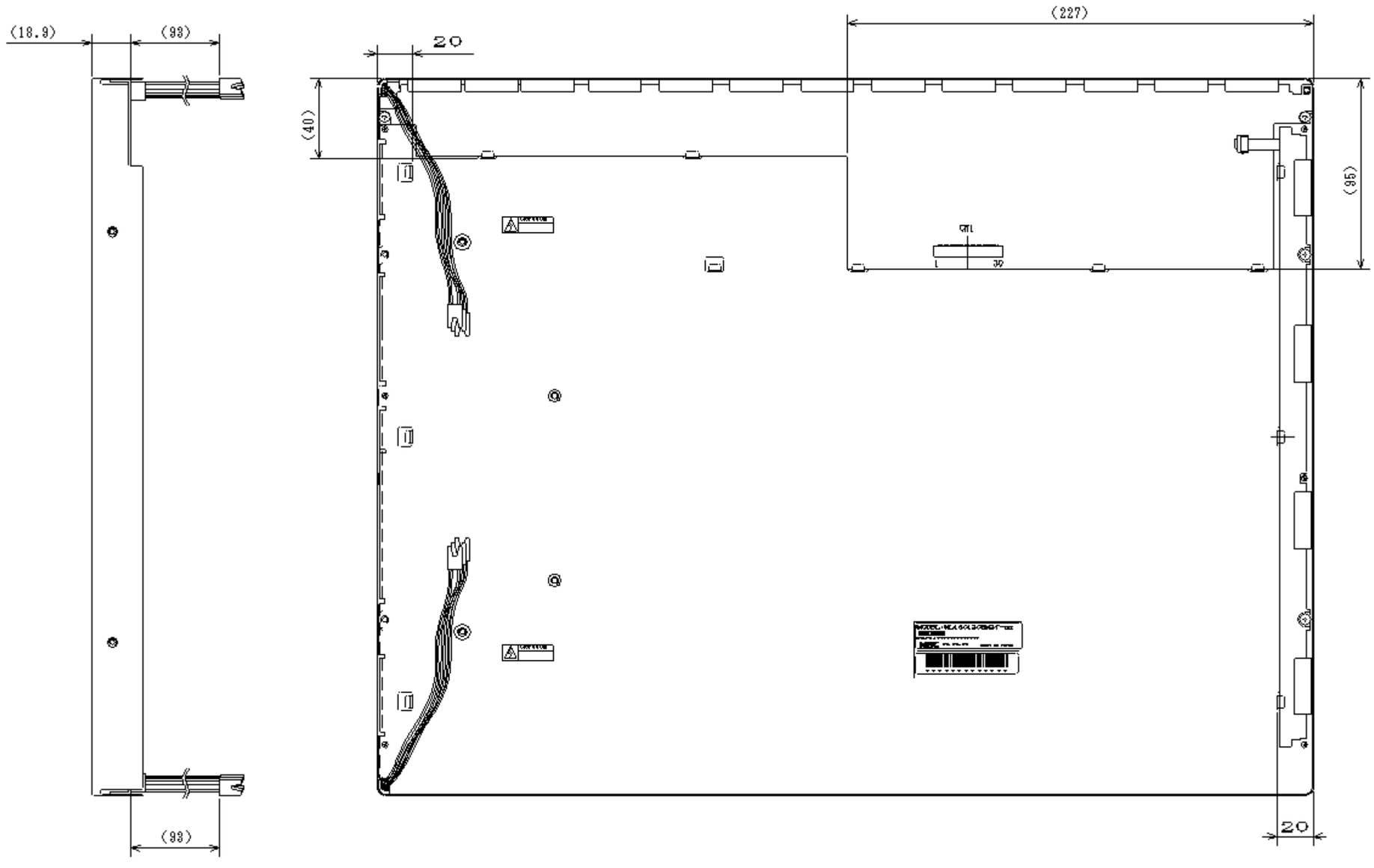
7.1 FRONT VIEW



Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The dimensions in parenthesis are for reference.
Note3: The torque for mounting screw should never exceed TBD N·m.
Note4: The right side and left side are symmetric figure for vertical axis.

Unit: mm

7.2 REAR VIEW



Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The dimensions in parenthesis are for reference.
Note3: The torque for mounting screw should never exceed TBD N·m.

Unit: mm

REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Document number	Prepared date	Revision contents and signature
1st edition	DOD-M-1316	Feb. 4, 2003	**Revision contents** New issue **Signature of writer** *Approved by* T. ITO; *Checked by*; *Prepared by* R. KAWASHIMA