

# NL17SG07E

## Buffer with Open Drain Output

The NL17SG07E MiniGate™ is an advanced high-speed CMOS Buffer with Open Drain Output in ultra-small footprint.

The NL17SG07E input and output structures provide protection when voltages up to 3.6 V are applied regardless of the supply voltage.

### Features

- Wide Operating  $V_{CC}$  Range: 0.9 V to 3.6 V
- High Speed:  $t_{PD} = 2.5$  ns (Typ) at  $V_{CC} = 3.0$  V,  $C_L = 15$  pF
- Low Power Dissipation:  $I_{CC} = 0.5$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- 3.6 V Overvoltage Tolerant (OVT) Input and Output Pins
- Ultra-Small Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

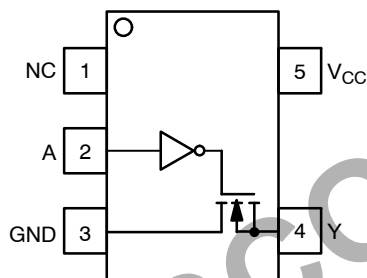


Figure 1. SC-88A  
(Top View)

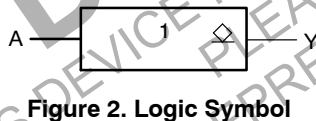
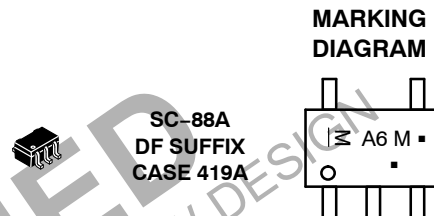


Figure 2. Logic Symbol



ON Semiconductor®

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M = Date Code\*

▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

### PIN ASSIGNMENT

PIN	NAME
1	NC
2	A
3	GND
4	Y
5	$V_{CC}$

### FUNCTION TABLE

Input A	Output Y
L	L
H	Z

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage	-0.5 to +4.6	V
$V_{IN}$	DC Input Voltage	-0.5 to +4.6	V
$V_{OUT}$	DC Output Voltage Active Mode, LOW State Tri-State Mode, Output at Hi-Z State Power-Down Mode ( $V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +4.6 -0.5 to +4.6	V
$I_{IK}$	DC Input Diode Current $V_{IN} < GND$	-20	mA
$I_{OK}$	DC Output Diode Current $V_{OUT} < GND$	-20	mA
$I_{OUT}$	DC Output Source/Sink Current	$\pm 20$	mA
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 20$	mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 20$	mA
$T_{STG}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
$T_J$	Junction Temperature Under Bias	+150	°C
MSL	Moisture Sensitivity	Level 1	
$F_R$	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
$V_{ESD}$	ESD Withstand Voltage Human Body Model (Note 2)	>2000	V
$I_{LATCHUP}$	Latch-up Performance above $V_{CC}$ and below GND at 125°C (Note 3)	$\pm 75$	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
$V_{CC}$	Positive DC Supply Voltage	0.9	3.6	V
$V_{IN}$	Digital Input Voltage	0.0	3.6	V
$V_{OUT}$	Output Voltage Output at Low State Tri-State Mode, Output at Hi-Z State Power-Down Mode ( $V_{CC} = 0$ V)	0.0 0.0 0.0	$V_{CC}$ 3.6 3.6	V
$T_A$	Operating Temperature Range	-55	+125	°C
$\Delta t / \Delta V$	Input Transition Rise or Fall Rate $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0	10	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# NL17SG07E

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			-55°C ≤ T <sub>A</sub> ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	High-Level Input Voltage		0.9	V <sub>CC</sub>			V <sub>CC</sub>		V
			1.1 to 1.3	0.70 x V <sub>CC</sub>			0.70 x V <sub>CC</sub>		
			1.4 to 1.6	0.65 x V <sub>CC</sub>			0.65 x V <sub>CC</sub>		
			1.65 to 1.95	0.65 x V <sub>CC</sub>			0.65 x V <sub>CC</sub>		
			2.3 to 2.7	1.7			1.7		
			3.0 to 3.6	2.0			2.0		
V <sub>IL</sub>	Low-Level Input Voltage		0.9			GND		GND	V
			1.1 to 1.3			0.30 x V <sub>CC</sub>		0.30 x V <sub>CC</sub>	
			1.4 to 1.6			0.35 x V <sub>CC</sub>		0.35 x V <sub>CC</sub>	
			1.65 to 1.95			0.35 x V <sub>CC</sub>		0.35 x V <sub>CC</sub>	
			2.3 to 2.7			0.7		0.7	
			3.0 to 3.6			0.8		0.8	
V <sub>OL</sub>	Low-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	0.9		0.1		0.1	V
			I <sub>OL</sub> = 0.3 mA	1.1 to 1.3		0.25 x V <sub>CC</sub>		0.25 x V <sub>CC</sub>	
			I <sub>OL</sub> = 1.7 mA	1.4 to 1.6		0.25 x V <sub>CC</sub>		0.25 x V <sub>CC</sub>	
			I <sub>OL</sub> = 3.0 mA	1.65 to 1.95		0.45		0.45	
			I <sub>OL</sub> = 4.0 mA	2.3 to 2.7		0.4		0.4	
			I <sub>OL</sub> = 8.0 mA	3.0 to 3.6		0.4		0.4	
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 0 to 3.6 V	0.9 to 3.6			±0.1		±1.0	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	3.6			0.5		10	μA
I <sub>OZ</sub>	Output Tri-State Leakage Current	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> = 0 to 3.6 V	0.9 to 3.6			1.0		10	μA
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>IN</sub> = 0 to 3.6 V V <sub>OUT</sub> = 0 to 3.6 V	0			1.0		10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# NL17SG07E

## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Condition	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
$t_{PZL}$	Propagation Delay, Enable Time, A to Y	$C_L = 10$ pF, $R_1 = R_L = 5$ k $\Omega$	0.9	–	12	–	–	–	ns
			1.1 to 1.3	–	5.5	7.9	–	9.0	
			1.4 to 1.6	–	4.0	5.7	–	7.3	
			1.65 to 1.95	–	3.3	3.9	–	5.9	
			2.3 to 2.7	–	2.7	3.3	–	4.5	
			3.0 to 3.6	–	2.4	2.9	–	3.7	
		$C_L = 15$ pF, $R_1 = R_L = 5$ k $\Omega$	0.9	–	12.5	–	–	–	ns
			1.1 to 1.3	–	5.8	8.1	–	9.2	
			1.4 to 1.6	–	4.1	6.0	–	7.4	
			1.65 to 1.95	–	3.4	4.0	–	6.2	
			2.3 to 2.7	–	2.8	3.4	–	4.6	
			3.0 to 3.6	–	2.5	3.0	–	3.7	
		$C_L = 30$ pF, $R_1 = R_L = 5$ k $\Omega$	0.9	–	13.2	–	–	–	ns
			1.1 to 1.3	–	6.2	8.7	–	9.8	
			1.4 to 1.6	–	4.5	6.2	–	7.6	
			1.65 to 1.95	–	3.5	4.2	–	6.4	
			2.3 to 2.7	–	3.0	3.6	–	4.7	
			3.0 to 3.6	–	2.6	3.1	–	3.9	
$t_{PLZ}$	Propagation Delay, Disable Time, A to Y	$C_L = 10$ pF, $R_1 = R_L = 5$ k $\Omega$	0.9	–	8.0	–	–	–	ns
			1.1 to 1.3	–	6.5	10.9	–	11.5	
			1.4 to 1.6	–	5.2	8.9	–	9.5	
			1.65 to 1.95	–	4.9	8.8	–	9.4	
			2.3 to 2.7	–	3.8	8.4	–	9.3	
			3.0 to 3.6	–	3.5	8.1	–	8.5	
		$C_L = 15$ pF, $R_1 = R_L = 5$ k $\Omega$	0.9	–	11.1	–	–	–	ns
			1.1 to 1.3	–	9.0	13.4	–	14	
			1.4 to 1.6	–	7.9	11.4	–	12.0	
			1.65 to 1.95	–	7.6	11.3	–	11.9	
			2.3 to 2.7	–	6.3	10.9	–	11.8	
			3.0 to 3.6	–	6.0	10.6	–	11.0	
		$C_L = 30$ pF, $R_1 = R_L = 5$ k $\Omega$	0.9	–	16.2	–	–	–	ns
			1.1 to 1.3	–	14	20.2	–	20	
			1.4 to 1.6	–	13	18.9	–	19.5	
			1.65 to 1.95	–	12.5	18.8	–	19.4	
			2.3 to 2.7	–	11.2	18.4	–	19.3	
			3.0 to 3.6	–	11	18.1	–	18.3	
$C_{IN}$	Input Capacitance		0 to 3.6	–	3	–	–	–	pF
$C_{PD}$	Power Dissipation Capacitance (Note 4)		0.9 to 3.6	–	4	–	–	–	pF

4.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$ .  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

# NL17SG07E

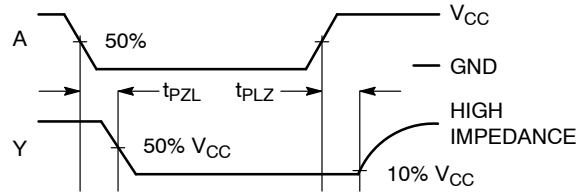
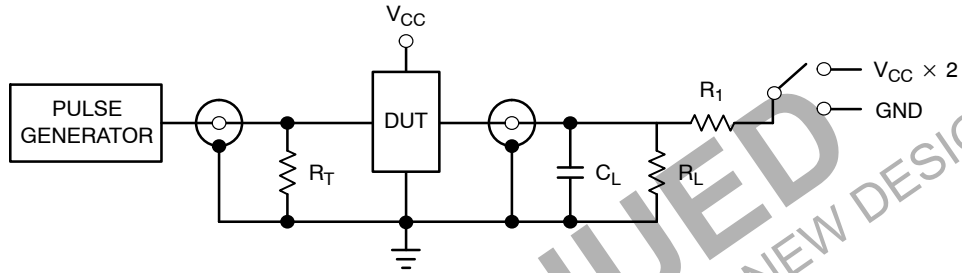


Figure 3. Switching Waveform



Test	Switch
tpZL	V <sub>CC</sub> × 2
tpLZ	V <sub>CC</sub> × 2

Figure 4. Test Circuit

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NL17SG07EDFT2G	SC-88A (Pb-Free)	3000 / Tape & Reel

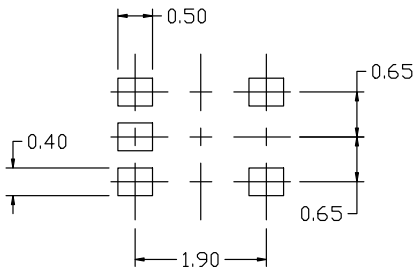
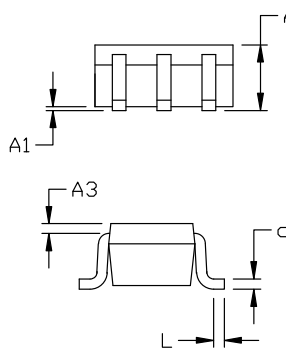
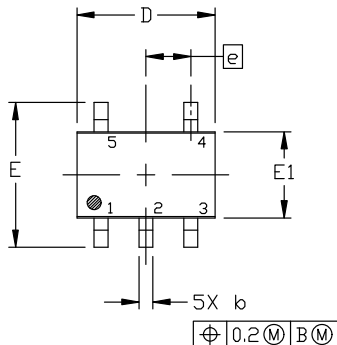
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 2:1

### SC-88A (SC-70-5/SOT-353) CASE 419A-02 ISSUE M

DATE 11 APR 2023



#### RECOMMENDED MOUNTING FOOTPRINT

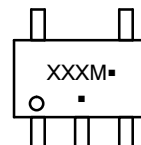
\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30

#### GENERIC MARKING DIAGRAM\*



\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### STYLE 1:

- PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

#### STYLE 2:

- PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

#### STYLE 3:

- PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

#### STYLE 4:

- PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

#### STYLE 5:

- PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

#### STYLE 6:

- PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

#### STYLE 7:

- PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

#### STYLE 8:

- PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

#### STYLE 9:

- PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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