D-Type Transparent Latch with 3-State Output

NL17SG373A

The NL17SG373A is a D−type transparent latch with 3−state output in tiny footprint packages. The device is designed to operate for V_{CC} = 0.9 V to 3.6 V.

Features

- Designed for 0.9 V to 3.6 V V_{CC} Operation
- 2.7 ns (Typ) at V_{CC} = 3.0 V, C_L = 15 pF
- Inputs/Outputs Over−Voltage Tolerant up to 3.6 V
- I_{OFF} Supports Partial Power Down Protection
- Available in SC−88 Package
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen−Free/BFR−Free and RoHS−Compliant

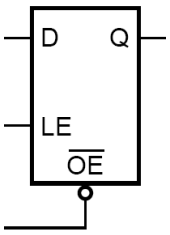

Figure 1. Logic Symbol

PIN ASSIGNMENTS

Pin	Name
1	LE
2	GND
3	D
4	Q
5	V_{CC}
6	$\overline{OE}$

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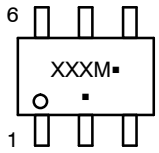
SC−88
DF SUFFIX
CASE 419B−02

MARKING DIAGRAM

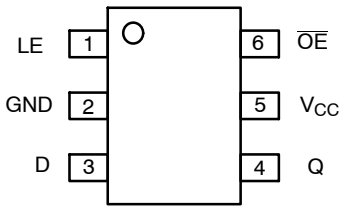


X, XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

PINOUT DIAGRAM



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 8 of this data sheet.

FUNCTION TABLE

Input				Output	
$\overline{OE}$	LE	D	Internal Latch	Q	Operating Mode
L	H	L	L	L	Enable and Read Register (Transparent Mode)
L	H	H	H	H	
L	L	X	L	L	Latch and Read Register
L	L	X	H	H	
H	X	X	X	Z	Latch Register and Disable Output

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +4.3	V
V_{IN}	DC Input Voltage		−0.5 to +4.3	V
V_{OUT}	DC Output Voltage	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +4.3 −0.5 to +4.3	V
I_{IK}	DC Input Diode Current	V_{IN} < GND	−20	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND	−20	mA
I_{OUT}	DC Output Source/Sink Current		±20	mA
I_{CC} or I_{GND}	DC Supply Current Per Supply Pin or Ground Pin		±20	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)		377	°C/W
P_D	Power Dissipation in Still Air		332	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 1000	V
$I_{LATCHUP}$	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm − by − 1inch, 2 ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

Table 1. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		0.9	3.6	V
V_{IN}	Digital Input Voltage		0	3.6	V
V_{OUT}	Output Voltage	Active Mode (High or Low State) Tri−State Mode (Note 1) Power Down Mode (V_{CC} = 0 V)	0 0 0	V_{CC} 3.6 3.6	V
T_A	Operating Free−Air Temperature		−55	+125	°C
t_r, t_f	Input Transition Rise or Fall Rate	V_{CC} = 3.3 V ± 0.3 V	0	10	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 2. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High−Level Input Voltage		0.9	–	V_{CC}	–	–	–	V
			1.1 to 1.3	$0.7 \times V_{CC}$	–	–	$0.7 \times V_{CC}$	–	
			1.4 to 1.6	$0.65 \times V_{CC}$	–	–	$0.65 \times V_{CC}$	–	
			1.65 to 1.95	$0.65 \times V_{CC}$	–	–	$0.65 \times V_{CC}$	–	
			2.3 to 2.7	1.7	–	–	1.7	–	
			3.0 to 3.6	2.0	–	–	2.0	–	
V_{IL}	Low−Level Input Voltage		0.9	–	GND	–	–	–	V
			1.1 to 1.3	–	–	$0.3 \times V_{CC}$	–	$0.3 \times V_{CC}$	
			1.4 to 1.6	–	–	$0.35 \times V_{CC}$	–	$0.35 \times V_{CC}$	
			1.65 to 1.95	–	–	$0.35 \times V_{CC}$	–	$0.35 \times V_{CC}$	
			2.3 to 2.7	–	–	0.7	–	0.7	
			3.0 to 3.6	–	–	0.8	–	0.8	
V_{OH}	High−Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}							V
		I_{OH} = −20 μA	0.9	–	0.75	–	–	–	
		I_{OH} = −0.3 mA	1.1 o 1.3	0.75 x V_{CC}	–	–	0.75 x V_{CC}	–	
		I_{OH} = −1.7 mA	1.4 to 1.6	0.75 x V_{CC}	–	–	0.75 x V_{CC}	–	
		I_{OH} = −3.0 mA	1.65 to 1.95	V_{CC} − 0.45	–	–	V_{CC} − 0.45	–	
		I_{OH} = −4.0 mA	2.3 to 2.7	2.0	–	–	2.0	–	
		I_{OH} = −8.0 mA	3.0 to 3.6	2.48	–	–	2.48	–	
V_{OL}	Low−Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}							V
		I_{OL} = 20 μA	0.9	–	0.1	–	–	–	
		I_{OL} = 0.3 mA	1.1 o 1.3	–	–	$0.25 \times V_{CC}$	–	$0.25 \times V_{CC}$	
		I_{OL} = 1.7 mA	1.4 to 1.6	–	–	$0.25 \times V_{CC}$	–	$0.25 \times V_{CC}$	
		$_{OL}$ = 3.0 mA	1.65 to 1.95	–	–	0.45	–	0.45	
		I_{OL} = 4.0 mA	2.3 to 2.7	–	–	0.4	–	0.4	
		I_{OL} = 8.0 mA	2.7 to 3.6	–	–	0.4	–	0.4	
I_{IN}	Input Leakage Current	V_{IN} = 0 V to 3.6 V	0.9 to 3.6	–	–	±0.1	–	±1.0	μA
I_{OZ}	3−State Output Leakage Current	V_{OUT} = 0 V to 3.6 V	0.9 to 3.6	–	–	1.0	–	10.0	μA
I_{OFF}	Power Off Leakage Current	V_{IN} = 0 V to 3.6 V; V_{OUT} = 0 V to 3.6 V	0	–	–	1.0	–	10.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	0.9 to 3.6	–	–	0.5	–	10.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 3. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V_{CC} (V)	T_A = 25°C			T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, D to Q (Figures 2 and 3)	C_L = 10 pF, R_L = 1 MΩ	0.9	–	37.6	–	–	–	ns
			1.1 to 1.3	–	10.8	24.4	–	27.0	
			1.4 to 1.6	–	6.1	8.6	–	9.4	
			1.65 to 1.95	–	4.5	6.2	–	6.7	
			2.3 to 2.7	–	3.1	4.2	–	4.8	
			3.0 to 3.6	–	2.6	3.4	–	3.7	
		C_L = 15 pF, R_L = 1 MΩ	0.9	–	38.2	–	–	–	ns
			1.1 to 1.3	–	11.0	25.1	–	27.7	
			1.4 to 1.6	–	6.3	9.2	–	10.4	
			1.65 to 1.95	–	4.7	6.9	–	7.1	
			2.3 to 2.7	–	3.2	4.4	–	5.0	
			3.0 to 3.6	–	2.7	3.4	–	3.9	
		C_L = 30 pF, R_L = 1 MΩ	0.9	–	39.9	–	–	–	ns
			1.1 to 1.3	–	11.6	27.0	–	29.6	
			1.4 to 1.6	–	6.8	11.6	–	12.6	
			1.65 to 1.95	–	5.1	9.1	–	9.6	
			2.3 to 2.7	–	3.5	5.7	–	6.1	
			3.0 to 3.6	–	3.0	4.4	–	4.8	
t_{PLH}, t_{PHL}	Propagation Delay, LE to Q (Figures 2 and 3)	C_L = 10 pF, R_L = 1 MΩ	0.9	–	37.6	–	–	–	ns
			1.1 to 1.3	–	10.8	24.4	–	27.0	
			1.4 to 1.6	–	6.1	8.6	–	9.4	
			1.65 to 1.95	–	4.5	6.2	–	6.7	
			2.3 to 2.7	–	3.1	4.2	–	4.8	
			3.0 to 3.6	–	2.6	3.4	–	3.7	
		C_L = 15 pF, R_L = 1 MΩ	0.9	–	38.2	–	–	–	ns
			1.1 to 1.3	–	11.0	25.1	–	27.7	
			1.4 to 1.6	–	6.3	9.2	–	10.4	
			1.65 to 1.95	–	4.7	6.9	–	7.1	
			2.3 to 2.7	–	3.2	4.4	–	5.0	
			3.0 to 3.6	–	2.7	3.4	–	3.9	
		C_L = 30 pF, R_L = 1 MΩ	0.9	–	39.9	–	–	–	ns
			1.1 to 1.3	–	11.6	27.0	–	29.6	
			1.4 to 1.6	–	6.8	11.6	–	12.6	
			1.65 to 1.95	–	5.1	9.1	–	9.6	
			2.3 to 2.7	–	3.5	5.7	–	6.1	
			3.0 to 3.6	–	3.0	4.4	–	4.8	

Table 3. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V_{CC} (V)	T_A = 25°C			T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
t_{PZH}, t_{PZL}	Output Enable Time, $\overline{OE}$ to Q (Figures 2 and 3)	C_L = 10 pF, R_L = 5 kΩ	0.9	–	32.4	–	–	–	ns
			1.1 to 1.3	–	9.4	20.5	–	22.6	
			1.4 to 1.6	–	5.3	8.1	–	8.2	
			1.65 to 1.95	–	4.0	5.4	–	5.8	
			2.3 to 2.7	–	2.8	3.9	–	4.0	
			3.0 to 3.6	–	2.4	2.9	–	3.2	
		C_L = 15 pF, R_L = 5 kΩ	0.9	–	33.0	–	–	–	ns
			1.1 to 1.3	–	9.6	21.2	–	23.3	
			1.4 to 1.6	–	5.5	8.3	–	8.4	
			1.65 to 1.95	–	4.1	6.1	–	6.5	
			2.3 to 2.7	–	3.0	3.9	–	4.2	
			3.0 to 3.6	–	2.5	3.0	–	3.3	
		C_L = 30 pF, R_L = 5 kΩ	0.9	–	34.7	–	–	–	ns
			1.1 to 1.3	–	10.2	23.1	–	25.2	
			1.4 to 1.6	–	6.1	9.5	–	10.5	
			1.65 to 1.95	–	4.6	7.9	–	8.6	
			2.3 to 2.7	–	3.3	5.0	–	5.5	
			3.0 to 3.6	–	2.7	3.8	–	4.2	
t_{PHZ}, t_{PLZ}	Output Disable Time, $\overline{OE}$ to Q (Figures 2 and 3)	C_L = 10 pF, R_L = 5 kΩ	0.9	–	22.0	–	–	–	ns
			1.1 to 1.3	–	8.0	13.7	–	13.8	
			1.4 to 1.6	–	5.3	7.6	–	7.7	
			1.65 to 1.95	–	5.1	6.8	–	6.9	
			2.3 to 2.7	–	3.8	5.3	–	5.4	
			3.0 to 3.6	–	4.4	5.6	–	5.9	
		C_L = 15 pF, R_L = 5 kΩ	0.9	–	23.5	–	–	–	ns
			1.1 to 1.3	–	9.1	14	–	14.2	
			1.4 to 1.6	–	6.1	9.0	–	9.2	
			1.65 to 1.95	–	6.2	8.3	–	8.4	
			2.3 to 2.7	–	4.6	6.6	–	6.7	
			3.0 to 3.6	–	5.6	7.3	–	7.5	
		C_L = 30 pF, R_L = 5 kΩ	0.9	–	27.8	–	–	–	ns
			1.1 to 1.3	–	12.3	17.6	–	18.1	
			1.4 to 1.6	–	8.6	12.4	–	12.5	
			1.65 to 1.95	–	9.4	12.9	–	12.9	
			2.3 to 2.7	–	6.8	9.1	–	9.5	
			3.0 to 3.6	–	9.0	12.5	–	13.0	

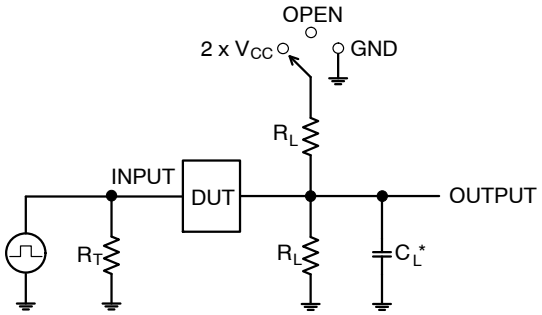
Table 4. TIMING REQUIREMENTS

Symbol	Parameter	Test Condition	V_{CC} (V)	T_A = 25°C			T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
t_W	Pulse Width, LE (Figures 2 and 3)	High	0.9	–	3.2	–	–	–	ns
			1.1 to 1.3	–	1.6	–	2.1	–	
			1.4 to 1.6	–	1.4	–	1.75	–	
			1.65 to 1.95	–	1.4	–	1.65	–	
			2.3 to 2.7	–	1.3	–	1.6	–	
			3.0 to 3.6	–	1.3	–	1.55	–	
t_{SU}	Setup Time, D to LE (Figures 2 and 3)	High or Low	0.9	–	2.0	–	–	–	ns
			1.1 to 1.3	–	0.2	–	2.7	–	
			1.4 to 1.6	–	0.1	–	1.5	–	
			1.65 to 1.95	–	0.1	–	1.2	–	
			2.3 to 2.7	–	0.1	–	0.9	–	
			3.0 to 3.6	–	0.1	–	0.7	–	
t_H	Hold Time, D to LE (Figures 2 and 3)	High or Low	0.9	–	−2.0	–	–	–	ns
			1.1 to 1.3	–	−0.2	–	0.4	–	
			1.4 to 1.6	–	0.1	–	0.5	–	
			1.65 to 1.95	–	0.1	–	0.5	–	
			2.3 to 2.7	–	0.1	–	0.5	–	
			3.0 to 3.6	–	0.2	–	0.5	–	

Table 5. CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition	Typical (T_A = 25°C)	Unit
C_{IN}	Input Capacitance	V_{CC} = 0 V	3.0	pF
C_{OUT}	Output Capacitance	V_{CC} = 0 V	3.0	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	f = 10 MHz, V_{CC} = 0.9 V to 3.6 V, V_{IN} = 0 V or V_{CC}	4.0	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \times V_{CC} \times f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption: $P_D = C_{PD} \times V_{CC}^2 \times f_{in} + I_{CC} \times V_{CC}$.



Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	$2 \times V_{CC}$
t_{PHZ} / t_{PZH}	GND

C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 W)
f = 1 MHz

Figure 2. Test Circuit

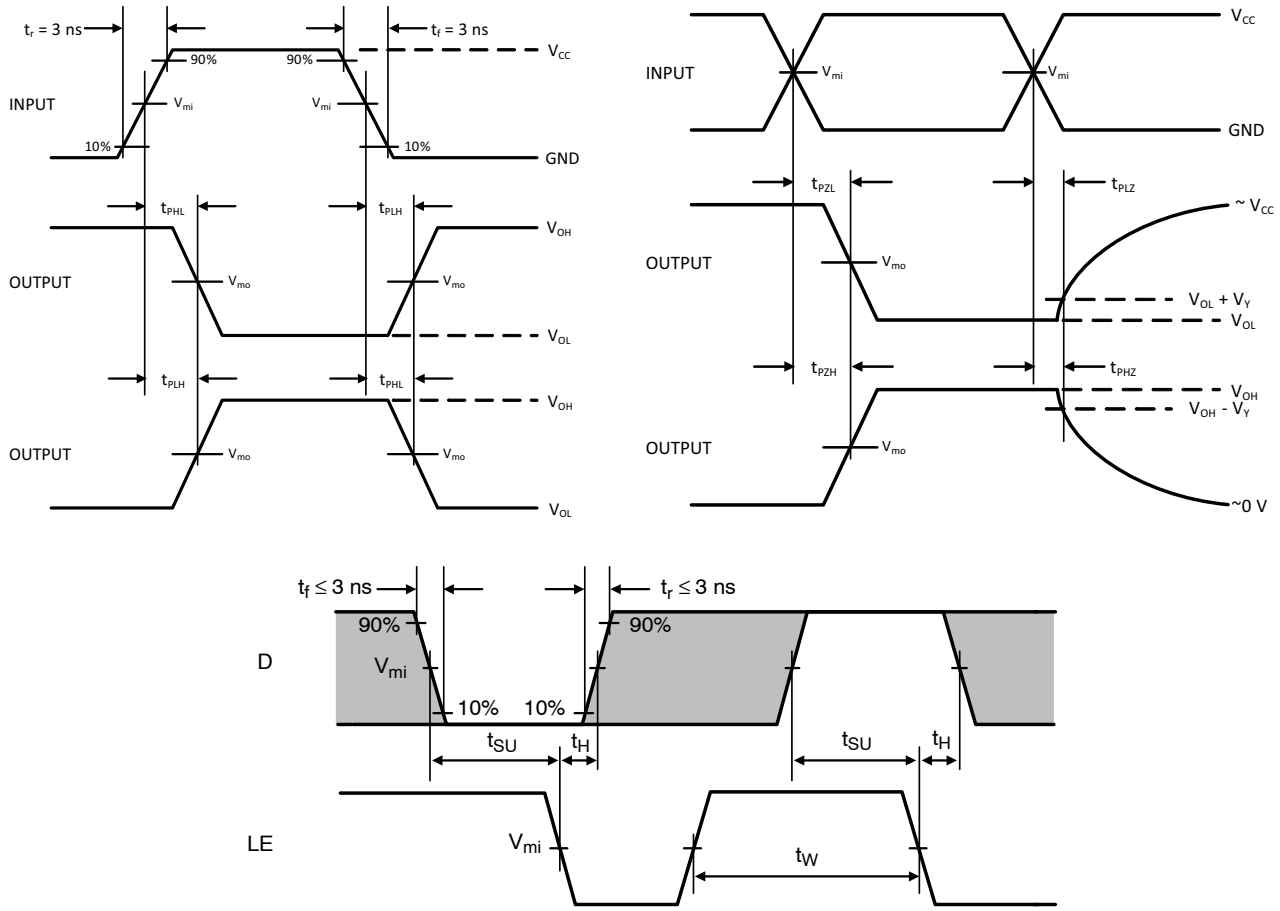


Figure 3. Switching Waveforms

V_{CC}, V	V_{mi}, V	V_{mo}, V	V_Y, V
0.9	V_{CC}/2	V_{CC}/2	0.1
1.1 to 1.3	V_{CC}/2	V_{CC}/2	0.1
1.4 to 1.6	V_{CC}/2	V_{CC}/2	0.1
1.65 to 1.95	V_{CC}/2	V_{CC}/2	0.15
2.3 to 2.7	V_{CC}/2	V_{CC}/2	0.15
3.0 to 3.6	1.5	1.5	0.3

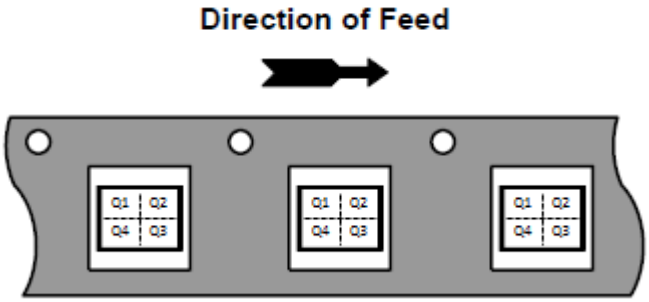
ORDERING INFORMATION

Device	Package	Marking	Pin 1 Orientation (See below)	Shipping†
NL17SG373ADFT2G	SC−88	AAA	Q4	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

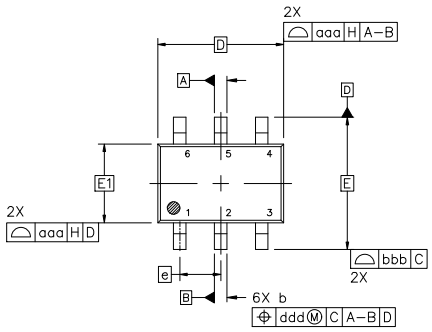
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC − Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel

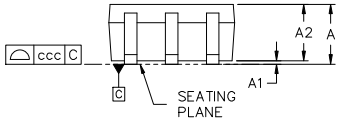


SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

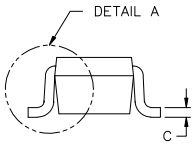
DATE 18 APR 2024



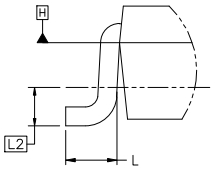
TOP VIEW



SIDE VIEW



END VIEW

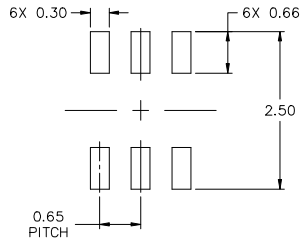


DETAIL A
SCALE 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

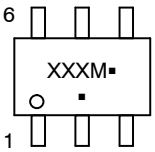
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	−−−	−−−	1.10
A1	0.00	−−−	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00 BSC		
E	2.10 BSC		
E1	1.25 BSC		
e	0.65 BSC		
L	0.26	0.36	0.46
L2	0.15 BSC		
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

DATE 18 APR 2024

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales