

NL17SH17

Single Schmitt-Trigger Buffer

The NL17SH17 is a single gate CMOS Schmitt-trigger non-inverting buffer fabricated with silicon gate CMOS technology. The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The NL17SH17 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the NL17SH17 to be used to interface 5 V circuits to 3 V circuits.

The NL17SH17 can be used to enhance noise immunity or to square up slowly changing waveforms.

Features

- High Speed: $t_{PD} = 4.0 \text{ ns}$ (Typ) at $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 1.0 \text{ }\mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 101
- These Devices are Pb-Free and are RoHS Compliant

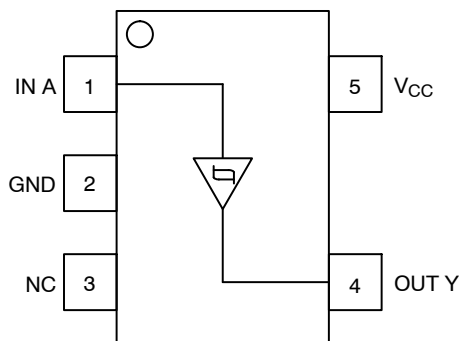


Figure 1. Pinout

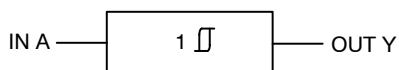


Figure 2. Logic Symbol



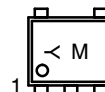
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM



SOT-953
CASE 527AE



Y = Specific Device Code
(Rotated 90°)
M = Month Code

PIN ASSIGNMENT

1	IN A
2	GND
3	NC
4	OUT Y
5	V _{CC}

FUNCTION TABLE

Input A	Output Y
L	L
H	H

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

NL17SH17

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current V _{IN} < GND	-20	mA
I _{OK}	DC Output Diode Current V _{OUT} < GND, V _{OUT} > V _{CC}	±20	mA
I _{OUT}	DC Output Source/Sink Current	±12.5	mA
I _{CC}	DC Supply Current per Supply Pin	±25	mA
I _{GND}	DC Ground Current per Ground Pin	±25	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature Under Bias	+150	°C
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>3000 >200 N/A	V
I _{LATCHUP}	Latchup Performance Above V _{CC} and Below GND at 125°C (Note 5)	±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage	1.65	5.5	V
V _{IN}	Digital Input Voltage	0.0	5.5	V
V _{OUT}	Output Voltage	0.0	V _{CC}	V
T _A	Operating Temperature Range	-55	+125	°C
Δt / ΔV	Input Transition Rise or Fall Rate V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0	No Limit No Limit	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0



Figure 3. Failure Rate vs. Time Junction Temperature

NL17SH17

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25°C			T _A ≤ 85°C		-55°C to 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{T+}	Positive Threshold Voltage		3.0 4.5 5.5		2.0 3.0 3.6	2.2 3.15 3.85		2.2 3.15 3.85		2.2 3.15 3.85	V
V _{T-}	Negative Threshold Voltage		3.0 4.5 5.5	0.9 1.35 1.65	1.5 2.3 2.9		0.9 1.35 1.65		0.9 1.35 1.65		V
V _H	Hysteresis Voltage		3.0 4.5 5.5	0.3 0.4 0.5	0.57 0.67 0.74	1.2 1.4 1.6	0.3 0.4 0.5	1.2 1.4 1.6	0.3 0.4 0.5	1.2 1.4 1.6	V
V _{OH}	High-Level Output Voltage	V _{IN} ≥ V _{Tmin} I _{OH} = -50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		V _{IN} ≥ V _{Tmin} I _{OH} = -4 mA I _{OH} = -8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V _{OL}	Low-Level Output Voltage	V _{IN} ≤ V _{Tmax} I _{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		V _{IN} ≤ V _{Tmax} I _{OL} = 4 mA I _{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			1.0		20		40	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

Symbol	Parameter	V _{CC} (V)	Test Conditions	T _A = 25°C			T _A ≤ 85°C		-55°C to 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay, A to Y	3.0 to 3.6	C _L = 15 pF C _L = 50 pF		7.0 8.5	12.8 16.3	1.0 1.0	15.0 18.5	1.0 1.0	17.0 20.5	ns
		4.5 to 5.5	C _L = 15 pF C _L = 50 pF		4.0 5.5	8.6 10.6	1.0 1.0	10.0 12.0	1.0 1.0	11.5 13.5	
C _{IN}	Input Capacitance				5.0	10		10		10	pF
C _{PD}	Power Dissipation Capacitance (Note 6)	Typical @ 25°C, V_{CC} = 5.0 V									
		7.0									pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NL17SH17

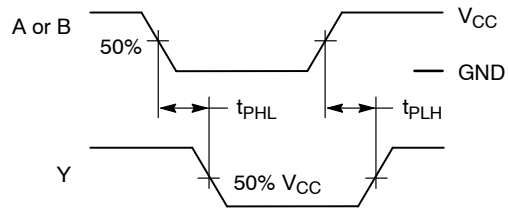
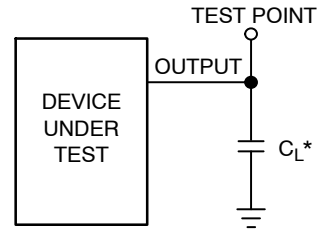


Figure 4. Switching Waveform



*Includes all probe and jig capacitance.

Figure 5. Test Circuit

ORDERING INFORMATION

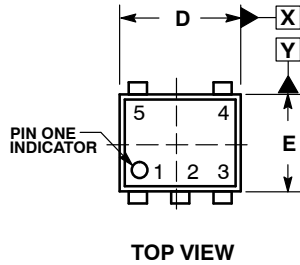
Device	Package	Shipping†
NL17SH17P5T5G	SOT-953 (Pb-Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

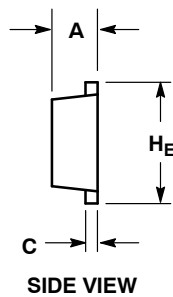
NL17SH17

PACKAGE DIMENSIONS

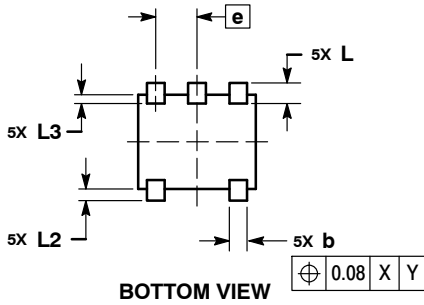
SOT-953
CASE 527AE
ISSUE E



TOP VIEW



SIDE VIEW



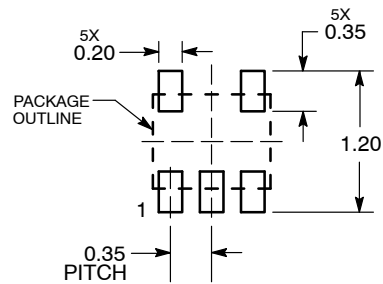
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.


DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
HE	0.95	1.00	1.05
L	0.175 REF		
L2	0.05	0.10	0.15
L3	---	---	0.15

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative