PRELIMINARY

NEC LCD Technologies, Ltd.

TFT COLOR LCD MODULE

NL192120AC25-02

57cm (22.5 Type)
WUXGA
LVDS Interface (4 ports)

PRELIMINARY DATA SHEET

DOD-PP-0539 (3rd edition)

RoHS Compliant 2002/95/EC

This PRELIMINARY DATA SHEET is updated document from DOD-PP-0477(2).

All information is subject to change without notice. Please confirm the sales representative before starting to design your system.

INTRODUCTION

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Examples: Computers, office automation equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment, industrial robots, etc.

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Examples: Control systems for transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, medical equipment not specifically designed for life support, safety equipment, etc.

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Examples: Military systems, aircraft control equipment, aerospace equipment, nuclear reactor control systems, medical equipment/devices/systems for life support, etc.

The quality grade of this product is the **"Standard"** unless otherwise specified in this document.

CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Color LCD module NL192120AC25-02 are composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Grayscale data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

1.2 APPLICATION

- Color monitor system

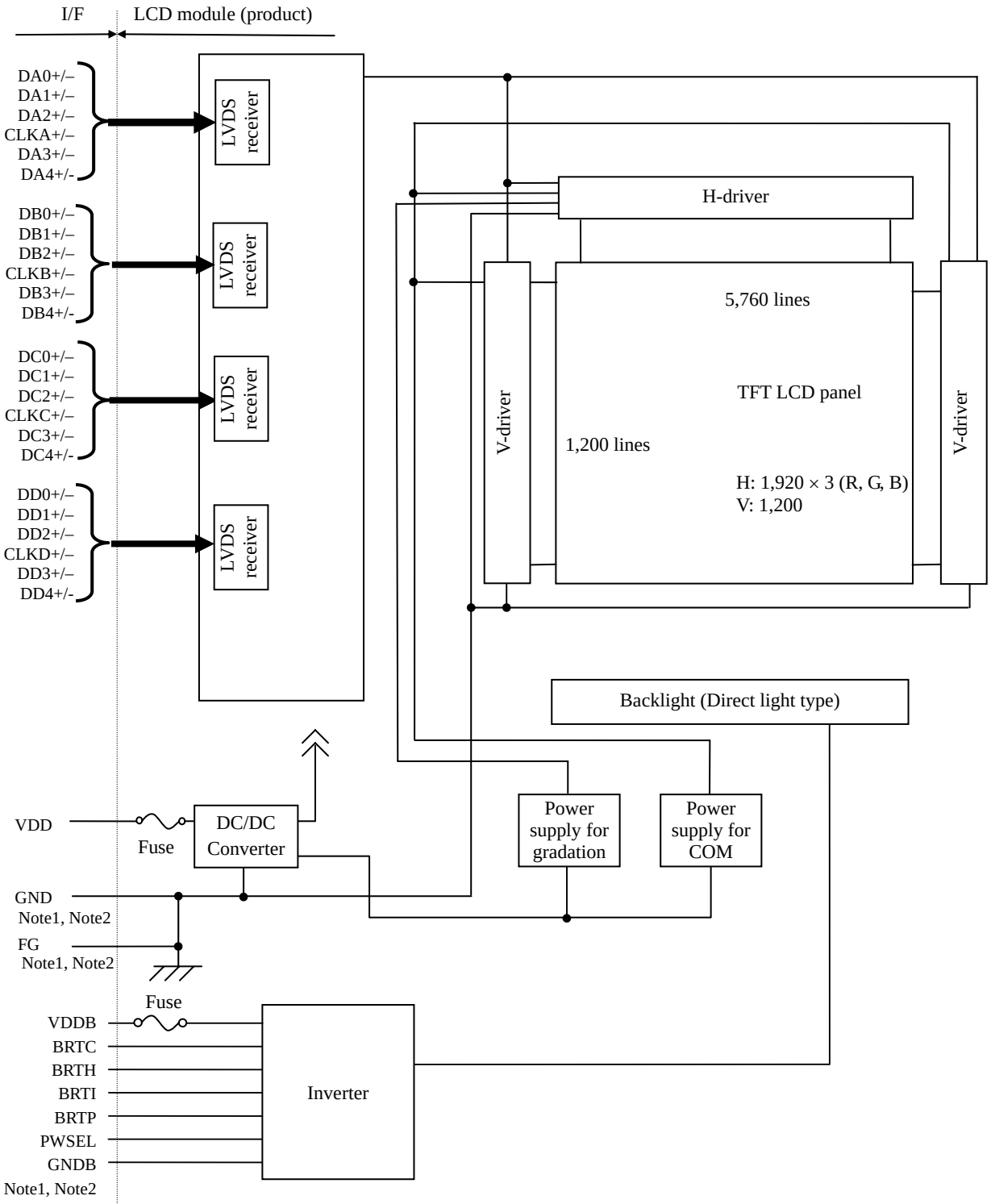
1.3 FEATURES

- Ultra-wide viewing angle (Adoption of Ultra-Advanced Super Fine TFT (UA-SFT)) 3
- Active matrix LCD
- LVDS interface (4ports)
- 1,024 gray scales per 1 sub-pixel (10-bit)
- High contrast
- 120Hz frame driving
- Fast response time

2. GENERAL SPECIFICATIONS

Display area	483.84 (H) ×302.4(V) mm	
Diagonal size of display	57.0 cm (22.5 inches)	
Drive system	a-Si TFT active matrix	
Display gray scale	1,073,741,824 colors (10-bit)	
Pixel	1,920 (H) × 1,200 (V) pixels	
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe	
Sub-pixel pitch	0.084 (H) × 0.252 (V) mm	
Pixel pitch	0.252 (H) × 0.252 (V) mm	
Module size	542 (W) × 362 (H) × 40 (D) mm (typ.) / 55.5 (D) mm (max.)	
Weight	(3,450) g (typ.)	3
Contrast ratio	(900:1) (typ.)	3
Viewing angle	*At the contrast ratio ≥10:1* • Horizontal: Right side 88° (typ.), Left side 88° (typ.) • Vertical: Up side 88° (typ.), Down side 88° (typ.)	
Designed viewing direction	Viewing angle with optimum grayscale (γ=2.2): normal axis (perpendicular)	
Polarizer surface	Antiglare	
Polarizer pencil-hardness	2H (min.) [by JIS K5400]	
Response time	*Ton + Toff (10%←→ 90%)* (12) ms (typ.)	
Luminance	*At the maximum luminance control* (420) cd/m^2 (typ.)	3
Color gamut	*At LCD panel center* (95) % (typ.) [against Adobe RBG]	3
Signal system	4 ports LVDS interface (THC63LVD104S×2pcs, THine Electronics, Inc. or equivalent) [RGB 10-bit signals, Data enable signal (DE), Dot clock (CLK)]	
Power supply voltage	LCD panel signal processing board: 12.0V Inverter: 12.0V	
Backlight	Direct light type: cold cathode fluorescent lamp with an inverter	
Power consumption	(70.32) W (typ.)	3

3. BLOCK DIAGRAM



Note1: Relations between GND (Signal ground), FG (Frame ground) and GNDB (Inverter ground) in the LCD module are as follows.

GND - FG	Connected
GND-GNDB	Not connected
FG-GNDB	Not connected

Note2: GND and FG must be connected to customer equipment's ground, and it is recommended that these grounds are connected together in customer equipment.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification		Unit
Module size	542 ±0.5 (W) × 362 ±0.5 (H) × 40 ±0.5 (D) 55.5 (max., D)	Note1	mm
Display area	483.84(H) × 302.4 (V)	Note1	mm
Weight	(3,450) (typ.)		g

Note1: See "**7. OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter			Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board		VDD	-0.3 to +14.0	V	Ta=25°C
	Inverter		VDDB	TBD	V	
Input voltage for signals	LVDS signal Note1		VD	-0.3 to+2.6	V	Ta=25°C VDD = 12.0V
	Inverter	BRTI signal	VBI	TBD	V	VDDB = TBD V
		BRTP signal	VBP	TBD	V	
		BRTC signal	VBC	TBD	V	
		PWSEL signal	VBS	TBD	V	
Storage temperature			Tst	(-20 to +60)	°C	-
Operating temperature		Front surface	TopF	(0 to +50)	°C	Note2
		Rear surface	TopR	TBD	°C	Note3
Relative humidity Note4			RH	≤ 95	%	Ta ≤ 40°C
				≤ 85	%	40°C < Ta ≤ 50°C
Absolute humidity Note4			AH	≤ 70 Note5	g/m^3	Ta > 50°C

Note1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CLKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CLKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CLKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CLKD+/-

Note2: Measured at center of LCD panel surface (including self-heat)

Note3: Measured at center of LCD module's rear shield surface (including self-heat)

Note4: No condensation

Note5: Water amount at Ta = 50°C and RH = 85%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta = 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDD	10.8	12.0	13.2	V	-
Power supply current		IDD	-	(1,000) Note1	(1,800) Note2	mA	at VDD = 12.0V
Permissible ripple voltage		VRP	-	-	100	mVp-p	for VDD
Differential input threshold voltage for Display signals	High	VTH	-	-	+100	mV	at VCM= 1.2V Note3, Note4
	Low	VTL	-100	-	-	mV	
Input voltage swing		VI	0	-	2.4	V	-
Terminating resistance		RT	-	100	-	Ω	-

Note1: Checkered flag pattern [by EIAJ ED-2522]
Note2: Pattern for maximum current
Note3: Common mode voltage for LVDS receiver
Note4: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CLKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CLKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CLKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CLKD+/-

4.3.2 Inverter

(Ta = 25°C)

Parameter	Symbol	min.	typ.	max.	Unit	Remarks	
Power supply voltage	VDDB	11.4	12.0	12.6	V	-	3
Power supply current	IDDB	-	(5,000)	(5,900)	mA	VDDB = TBD V, At the maximum luminance control	3

4.3.3 Power supply voltage ripple

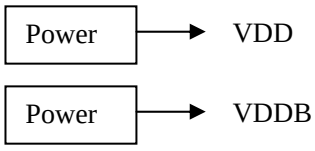
This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VDD	12.0 V	≤ 100	mVp-p
VDDB	12.0 V	≤ TBD	mVp-p

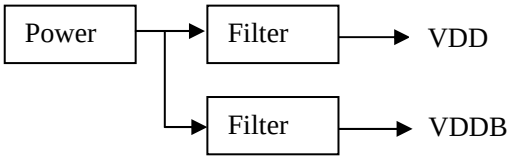
Note1: The permissible ripple voltage includes spike noise.

Example of the power supply connection

a) Separate the power supply



b) Put in the filter



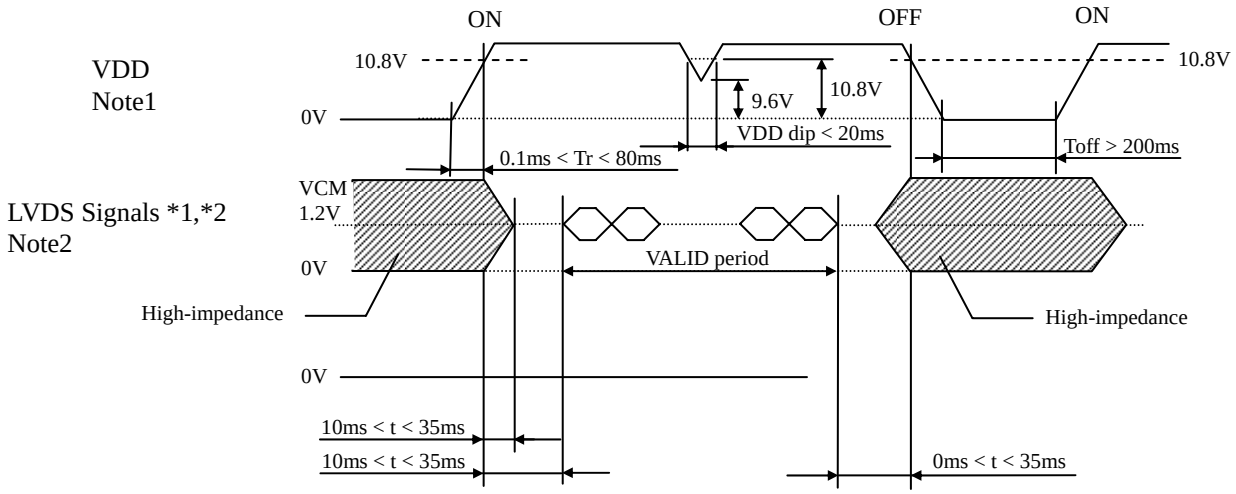
4.3.4 Fuse

Parameter	Fuse		Rating	Fusing current	Remarks	
	Type	Supplier				
VDD	TF16AT5.00TTD	KOA	5.0A 32V	10A, 5sec.max.	Note1	
VDDB	(R451010)	(Littel fuse)	(10A) (125V)	(20A, 5sec.max.)		3

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 LCD panel signal processing board



*1: DA0+/-, DA1+/-, DA2+/-, DA3+/-,DA4+/-, CLKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CLKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CLKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CLKD+/-

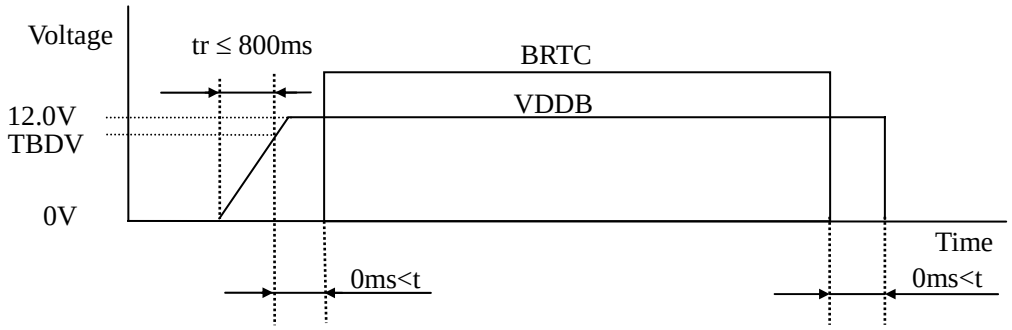
*2: LVDS signals should be measured at the terminal of 100Ω resistance.

Note1: In terms of voltage variation (voltage drop) while VDD rising edge is below 10.8V, a protection circuit may work, and then this product may not work.

Note2: LVDS signals must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged.
If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. VDD should be cut when the display and function signals are stopped.

Note3: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.

4.4.2 Inverter



Note1: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.

Note2: If tr is more than 800ms, the backlight will be turned off by a protection circuit for inverter.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

CN1 socket (LCD module side): FI-RE51S-HF (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: FI-RE51HL,FI-RE51CL (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	Note1
2	GND	Ground	Note1
3	GND	Ground	Note1
4	DA0-	Pixel data A0	LVDS differential data input Note2
5	DA0+		
6	GND	Ground	Note1
7	DA1-	Pixel data A1	LVDS differential data input Note2
8	DA1+		
9	GND	Ground	Note1
10	DA2-	Pixel data A2	LVDS differential data input Note2
11	DA2+		
12	GND	Ground	Note1
13	CLKA-	Pixel clock A	LVDS differential data input Note2
14	CLKA+		
15	GND	Ground	Note1
16	DA3-	Pixel data A3	LVDS differential data input Note2
17	DA3+		
18	GND	Ground	Note1
19	DA4-	Pixel data A4	LVDS differential data input Note2
20	DA4+		
21	GND	Ground	Note1
22	DB0-	Pixel data B0	LVDS differential data input Note2
23	DB0+		
24	GND	Ground	Note1
25	DB1-	Pixel data B1	LVDS differential data input Note2
26	DB1+		
27	GND	Ground	Note1
28	DB2-	Pixel data B2	LVDS differential data input Note2
29	DB2+		
30	GND	Ground	Note1
31	CLKB-	Pixel clock B	LVDS differential data input Note2
32	CLKB+		
33	GND	Ground	Note1
34	DB3-	Pixel data B3	LVDS differential data input Note2
35	DB3+		
36	GND	Ground	Note1
37	DB4-	Pixel data B4	LVDS differential data input Note2
38	DB4+		
39	GND	Ground	Note1
40	GND	Ground	Note1

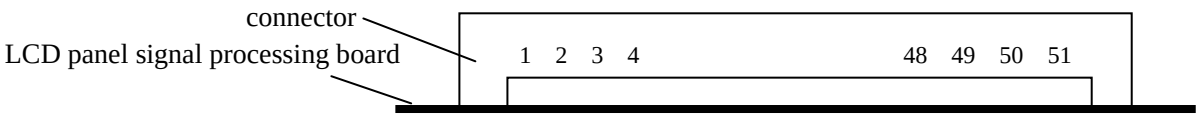
To be continued

Continued

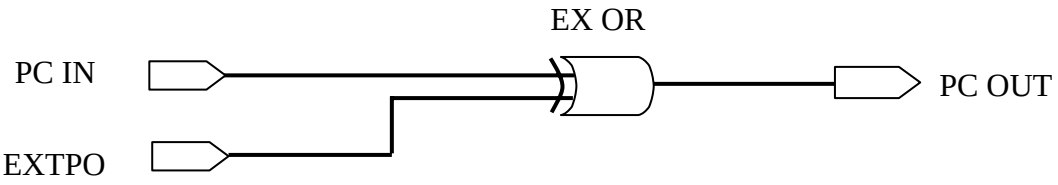
Pin No.	Symbol	Signal	Remarks
41	GND	Ground	Note1
42	RESERVED	RESERVED	Keep this pin Open.
43	RESERVED	RESERVED	Keep this pin Open.
44	RESERVED	RESERVED	Keep this pin Open.
45	RESERVED	RESERVED	Keep this pin Open.
46	GND	Ground	Note1
47	EXTPOL	External polarity control input signal	Note3
48	DLPOUT	Data latch pulse output signal	Note4
49	VSPOUT	Gate start pulse output signal	Note4
50	RESERVED	RESERVED	Keep this pin Open.
51	GND	Ground	Note1

3
3
3

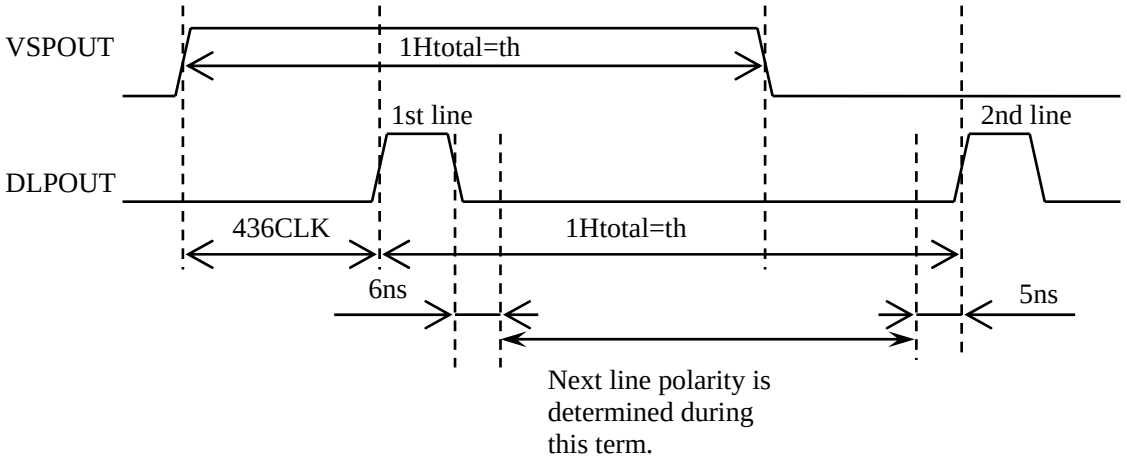
CN1: Connection inserting side



Note1: All GND terminals should be used without any non-connected lines.
Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.
Note3: It is possible to control the polarity inversion to input external signal into No.47pin. 3



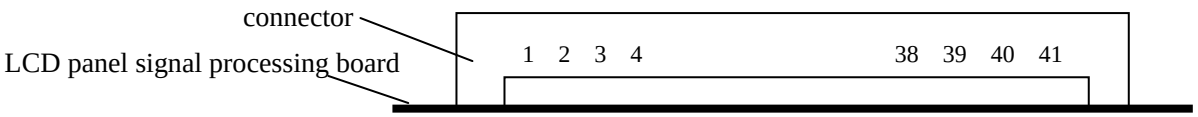
Note4: PC input signal to No.47 pin needs to synchronized with output signals from No.48 and 49. 3



CN2 socket (LCD module side): FI-RE41S-HS (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: FI-RE41HL , FI-RE41CL (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	Note1
2	GND	Ground	Note1
3	GND	Ground	Note1
4	DC0-	Pixel data C0	LVDS differential data input Note2
5	DC0+		
6	GND	Ground	Note1
7	DC1-	Pixel data C1	LVDS differential data input Note2
8	DC1+		
9	GND	Ground	Note1
10	DC2-	Pixel data C2	LVDS differential data input Note2
11	DC2+		
12	GND	Ground	Note1
13	CLKC-	Pixel clock C	LVDS differential data input Note2
14	CLKC+		
15	GND	Ground	Note1
16	DC3-	Pixel data C3	LVDS differential data input Note2
17	DC3+		
18	GND	Ground	Note1
19	DC4-	Pixel data C4	LVDS differential data input Note2
20	DC4+		
21	GND	Ground	Note1
22	DD0-	Pixel data D0	LVDS differential data input Note2
23	DD0+		
24	GND	Ground	Note1
25	DD1-	Pixel data D1	LVDS differential data input Note2
26	DD1+		
27	GND	Ground	Note1
28	DD2-	Pixel data D2	LVDS differential data input Note2
29	DD2+		
30	GND	Ground	Note1
31	CLKD-	Pixel clock D	LVDS differential data input Note2
32	CLKD+		
33	GND	Ground	Note1
34	DD3-	Pixel data D3	LVDS differential data input Note2
35	DD3+		
36	GND	Ground	Note1
37	DD4-	Pixel data D4	LVDS differential data input Note2
38	DD4+		
39	GND	Ground	Note1
40	GND	Ground	Note1
41	GND	Ground	Note1

CN2: Connector inserting side

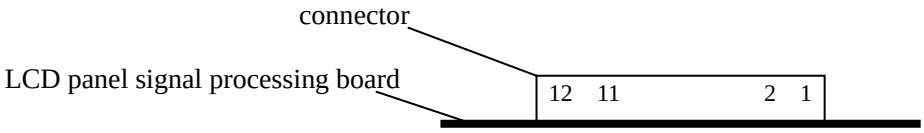


Note1: All GND terminals should be used without any non-connected lines.
Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

CN3 socket (LCD module side): IL-Z-12PL1-SMTYE (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: IL-Z-12S-S125C3 (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	VDD	Power supply	+12V Note1
2	VDD		
3	VDD		
4	VDD		
5	VDD		
6	VDD		
7	GND	Signal ground	Note1
8	GND		
9	GND		
10	GND		
11	GND		
12	GND		

CN3: Connector inserting side



Note1: All VDD and GND terminals should be used without any non-connected lines.

4.5.2 Inverter

CN201 socket (LCD module side): DF3Z-10P-2H (2∗) (Hirose Electric Co., Ltd.(HRS))
Adaptable plug: DF3-10S-2C (HIROSE ELECTRIC Co., Ltd. (HRS))

Pin No.	Symbol	Function	Description
1	GNDB	Inverter ground	Note1
2	GNDB		
3	GNDB		
4	GNDB		
5	GNDB		
6	VDDB	Power supply	Note1
7	VDDB		
8	VDDB		
9	VDDB		
10	VDDB		

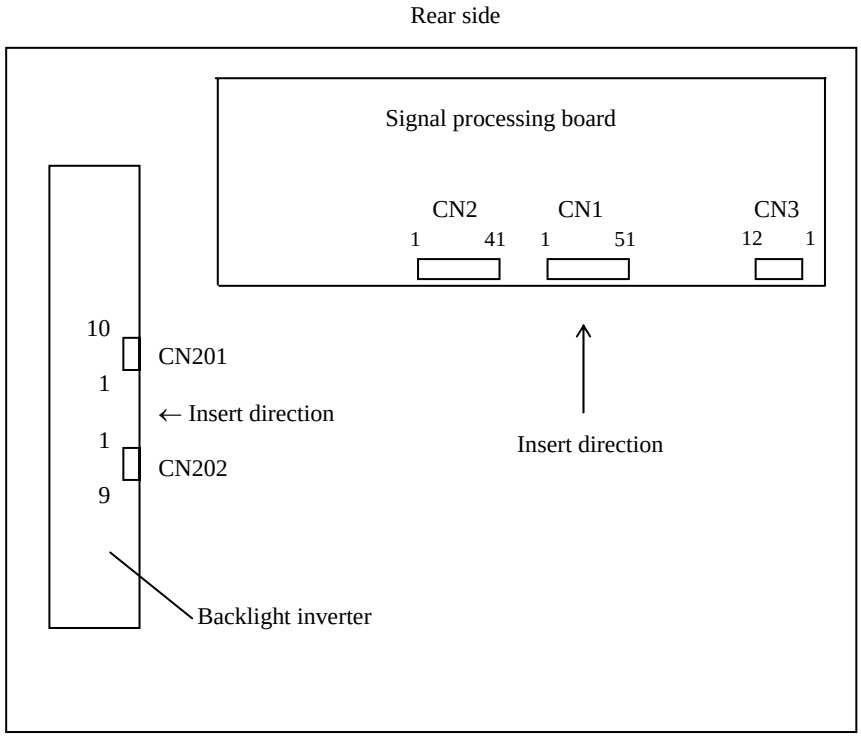
Note1: All GNDB and VDDB terminals should be used without any non-connected lines.

CN202 socket (LCD module side): IL-Z-9PL-SMTYE (Japan Aviation Electronics Industry Limited (JAE)) 3
Adaptable plug: IL-Z-9S-S125C3 (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	GNDB	Inverter ground	Note1
2	GNDB		
3	N.C.	-	Keep this pin Open.
4	BRTC	Backlight ON/OFF control signal	High or Open: Backlight ON Low: Backlight OFF
5	BRTH	Luminance control terminal	-
6	BRTI		
7	BRTP	BRTP signal	
8	GNDB	Inverter ground	Note1
9	PWSEL	Selection of luminance control signal method	Note2

Note1: All GNDB terminals should be used without any non-connected lines.
Note2: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

4.5.3 Positions of socket 3



4.6 Connection between receiver and transmitter for LVDS

	Bit mapping	Trancemitter Pin Assign: Single type LVDS Tx	Trancemitter Pin Assign: Dual type LVDS Tx (Thine THC63LVD103)	Output Connector		CN1: Pin No.	CN1: Signal Name
Pixel data A	RA4	TA0	R14			-	-
	RA5	TA1	R15	ATA-	→	4	DA0-
	RA6	TA2	R16				
	RA7	TA3	R17	ATA+	→	5	DA0+
	RA8	TA4	R18				
	RA9	TA5	R19				
	GA4	TA6	G14			-	-
	GA5	TB0	G15				
	GA6	TB1	G16	ATB-	→	7	DA1-
	GA7	TB2	G17				
	GA8	TB3	G18	ATB+	→	8	DA1+
	GA9	TB4	G19				
	BA4	TB5	B14				
	BA5	TB6	B15			-	-
	BA6	TC0	B16				
	BA7	TC1	B17	ATC-	→	10	DA2-
	BA8	TC2	B18				
	BA9	TC3	B19	ATC+	→	11	DA2+
	Hsync	TC4	Hsync				
	Vsync	TC5	Vsync				
	DE	TC6	DE			-	-
	RA2	TD0	R12				
	RA3	TD1	R13	ATD-	→	16	DA3-
	GA2	TD2	G12				
	GA3	TD3	G13	ATD+	→	17	DA3+
	BA2	TD4	B12				
	BA3	TD5	B13				
	N.C.	TD6	-			-	-
	RA0	TE0	R10				
	RA1	TE1	R11			19	DA4-
	GA0	TE2	G10	ATE-	→		
	GA1	TE3	G11		→	20	DA4+
	BA0	TE4	B10	ATE+			
	BA1	TE5	B11			-	-
	N.C.	TE6	-				
	CLK	CLK	CLK	ATCLK-	→	13	CLKA-
				ATCLK+	→	14	CLKA+
Pixel data B	RB4	TA0	R14			-	-
	RB5	TA1	R15	BTA-	→		
	RB6	TA2	R16				
	RB7	TA3	R17	BTA+	→	23	DB0+
	RB8	TA4	R18				
	RB9	TA5	R19				
	GB4	TA6	G14			-	-
	GB5	TB0	G15				
	GB6	TB1	G16	BTB-	→	25	DB1-
	GB7	TB2	G17				
	GB8	TB3	G18	BTB+	→	26	DB1+
	GB9	TB4	G19				
	BB4	TB5	B14				
	BB5	TB6	B15			-	-
	BB6	TC0	B16				
	BB7	TC1	B17	BTC-	→	28	DB2-
	BB8	TC2	B18				
	BB9	TC3	B19	BTC+	→	29	DB2+
	Hsync	TC4	Hsync				
	Vsync	TC5	Vsync				
	DE	TC6	DE			-	-
	RB2	TD0	R12				
	RB3	TD1	R13	BTD-	→	34	DB3-
	GB2	TD2	G12				
	GB3	TD3	G13	BTD+	→	35	DB3+
	BB2	TD4	B12				
	BB3	TD5	B13				
	N.C.	TD6	-			-	-
	RB0	TE0	R10				
	RB1	TE1	R11			37	DB4-
	GB0	TE2	G10	BTE-	→		
	GB1	TE3	G11		→	38	DB4+
	BB0	TE4	B10	BTE+			
	BB1	TE5	B11			-	-
	N.C.	TE6	-				
	CLK	CLK	CLK	BTCLK-	→	31	CLKB-
				BTCLK+	→	32	CLKB+

	Bit mapping	Trancemitter Pin Assign: Single type LVDS Tx	Trancemitter Pin Assign: Dual type LVDS Tx (Thine THC63LVD103)	Output Connector		CN2: Pin No.	CN2: Signal Name
Pixel Data C	RC4	TA0	R14			-	-
	RC5	TA1	R15	CTA-	→		
	RC6	TA2	R16				
	RC7	TA3	R17	CTA+	→	5	DC0+
	RC8	TA4	R18				
	RC9	TA5	R19				
	GC4	TA6	G14			-	-
	GC5	TB0	G15				
	GC6	TB1	G16	CTB-	→	7	DC1-
	GC7	TB2	G17				
	GC8	TB3	G18	CTB+	→	8	DC1+
	GC9	TB4	G19				
	BC4	TB5	B14				
	BC5	TB6	B15			-	-
	BC6	TC0	B16				
	BC7	TC1	B17	CTC-	→	10	DC2-
	BC8	TC2	B18				
	BC9	TC3	B19	CTC+	→	11	DC2+
	Hsync	TC4	Hsync				
	Vsync	TC5	Vsync				
	DE	TC6	DE			-	-
	RC2	TD0	R12				
	RC3	TD1	R13	CTD-	→	16	DC3-
	GC2	TD2	G12				
	GC3	TD3	G13	CTD+	→	17	DC3+
	BC2	TD4	B12				
	BC3	TD5	B13				
	N.C.	TD6	-			-	-
	RC0	TE0	R10				
	RC1	TE1	R11			19	DC4-
	GC0	TE2	G10	CTE-	→		
	GC1	TE3	G11			20	DC4+
	BC0	TE4	B10	CTE+	→		
	BC1	TE5	B11				
	N.C.	TE6	-			-	-
	CLK	CLK	CLK	CTCLK-	→	13	CLKC-
				CTCLK+	→	14	CLKC+
Pixel Data D	RD4	TA0	R14			-	-
	RD5	TA1	R15	DTA-	→		
	RD6	TA2	R16				
	RD7	TA3	R17	DTA+	→	23	DD0+
	RD8	TA4	R18				
	RD9	TA5	R19				
	GD4	TA6	G14			-	-
	GD5	TB0	G15				
	GD6	TB1	G16	DTB-	→	25	DD1-
	GD7	TB2	G17				
	GD8	TB3	G18	DTB+	→	26	DD1+
	GD9	TB4	G19				
	BD4	TB5	B14				
	BD5	TB6	B15			-	-
	BD6	TC0	B16				
	BD7	TC1	B17	DTC-	→	28	DD2-
	BD8	TC2	B18				
	BD9	TC3	B19	DTC+	→	29	DD2+
	Hsync	TC4	Hsync				
	Vsync	TC5	Vsync				
	DE	TC6	DE			-	-
	RD2	TD0	R12				
	RD3	TD1	R13	DTD-	→	34	DD3-
	GD2	TD2	G12				
	GD3	TD3	G13	DTD+	→	35	DD3+
	BD2	TD4	B12				
	BD3	TD5	B13				
	N.C.	TD6	-			-	-
	RD0	TE0	R10				
	RD1	TE1	R11	DTE-	→	37	DD4-
	GD0	TE2	G10				
	GD1	TE3	G11	DTE+	→	38	DD4+
	BD0	TE4	B10				
	BD1	TE5	B11			-	-
	N.C.	TE6	-				
	CLK	CLK	CLK	DTCLK-	→	31	CLKD-
				DTCLK+	→	32	CLKD+

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

4.7 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display in equivalent to 1,073,741,824 colors in 1,024 gray scales. Also the relation between display colors and input data signals is as the following table.

	Display colors	Data signal (0: Low level, 1: High level)																															
		RA9 RB9 RC9 RD9	RA8 RB8 RC8 RD8	RA7 RB7 RC7 RD7	RA6 RB6 RC6 RD6	RA5 RB5 RC5 RD5	RA4 RB4 RC4 RD4	RA3 RB3 RC3 RD3	RA2 RB2 RC2 RD2	RA1 RB1 RC1 RD1	RA0 RB0 RC0 RD0	GA9 GB9 GC9 GD9	GA8 GB8 GC8 GD8	GA7 GB7 GC7 GD7	GA6 GB6 GC6 GD6	GA5 GB5 GC5 GD5	GA4 GB4 GC4 GD4	GA3 GB3 GC3 GD3	GA2 GB2 GC2 GD2	GA1 GB1 GC1 GD1	GA0 GB0 GC0 GD0	BA9 BB9 BC9 BD9	BA8 BB8 BC8 BD8	BA7 BB7 BC7 BD7	BA6 BB6 BC6 BD6	BA5 BB5 BC5 BD5	BA4 BB4 BC4 BD4	BA3 BB3 BC3 BD3	BA2 BB2 BC2 BD2	BA1 BB1 BC1 BD1	BA0 BB0 BC0 BD0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	↓					:										:										:							
		1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	bright	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑					:										:										:							
	↓					:										:										:							
		0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	bright	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Blue gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	
	↑					:										:										:							
	↓					:										:										:							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

4.8 DISPLAY POSITIONS

Left half of display (0 ≤ n < 480, 0≤ m < 1200)

pixel (even) D(2n,m)			pixel (odd) D(2n+1,m)		
RA	GA	BA	RB	GB	BB

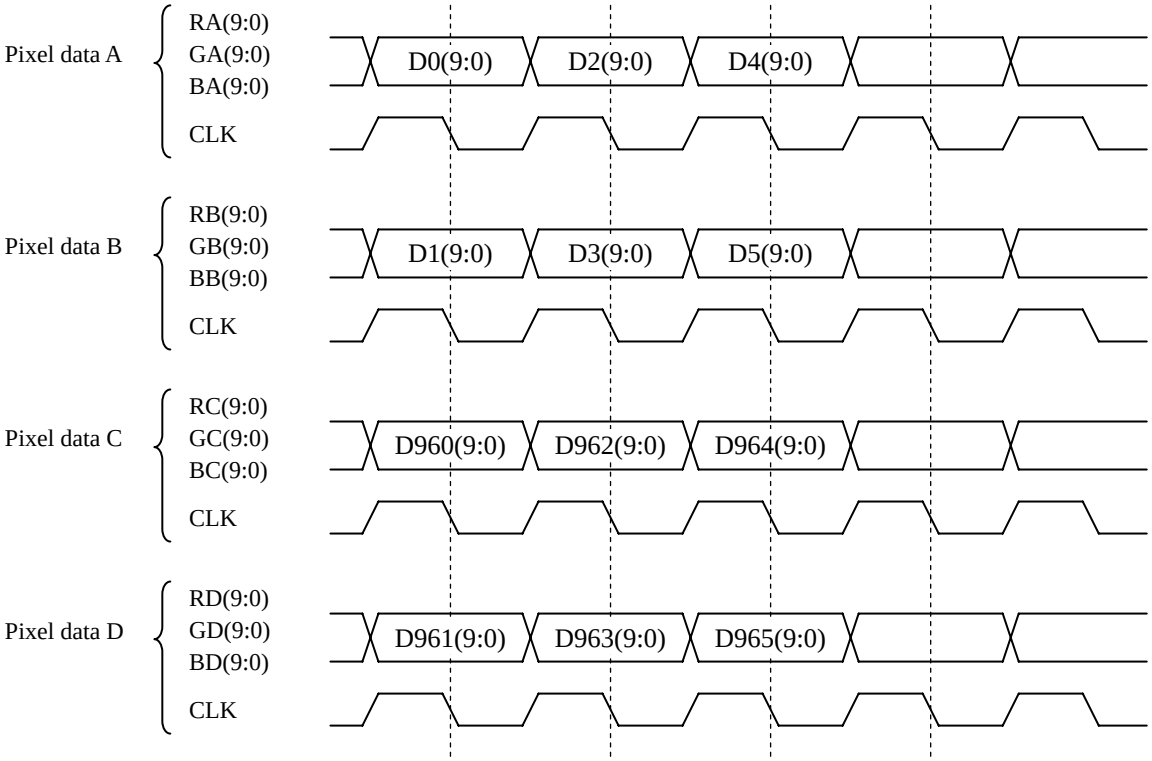
Right half of display (480 ≤ n < 960, 0 ≤ m1 < 200)

pixel (even) D(2n,m)			pixel (odd) D(2n+1,m)		
RC	GC	BC	RD	GD	BD

D(0,0)	D(1,0)	• • •	D(959,0)	D(960,0)	D(961,0)	• • •	D(1919,0)
D(0,1)	D(1,1)	• • •	D(959,1)	D(960,1)	D(961,1)	• • •	D(1919,1)
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
D(0,1199)	D(1,1199)	• • •	D(959,1199)	D(960,1199)	D(961,1199)	• • •	D(1919,1199)

Note1: n, m: counting number

4.9 LVDS DATA TRANSMISSION METHOD



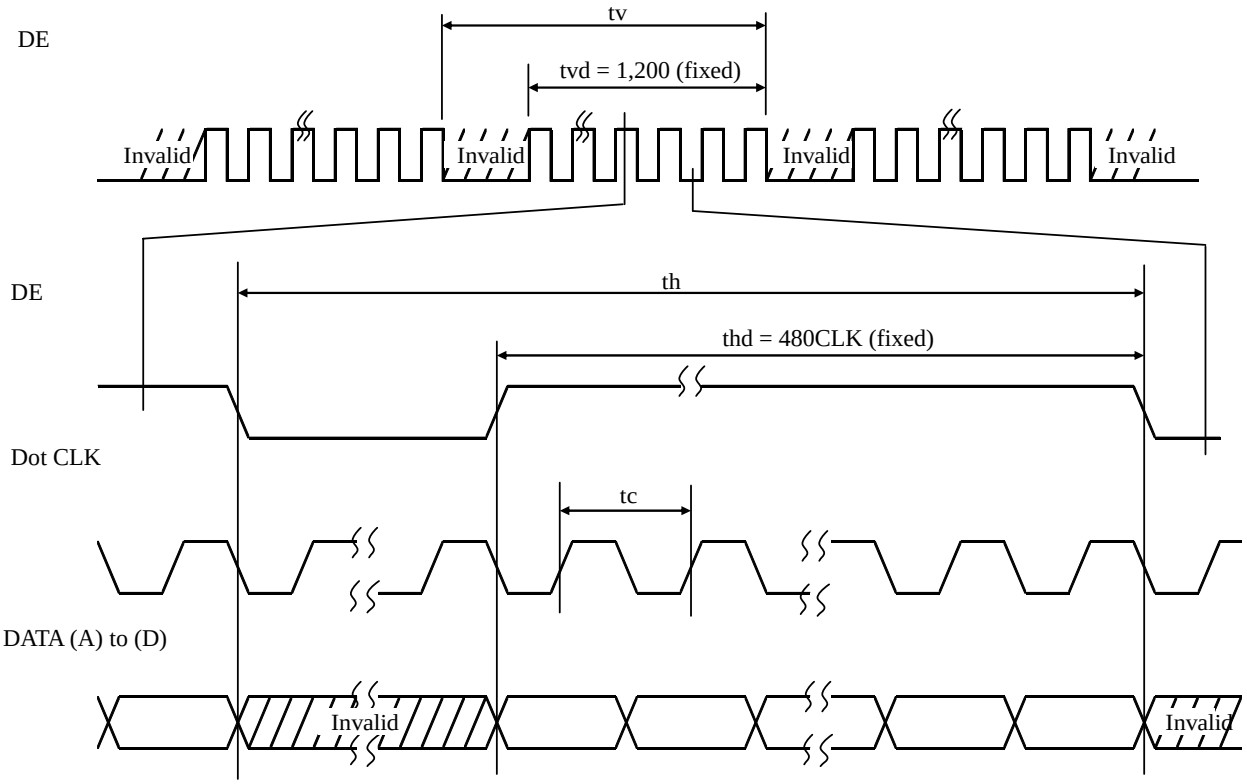
4.10 INPUT SIGNAL TIMINGS

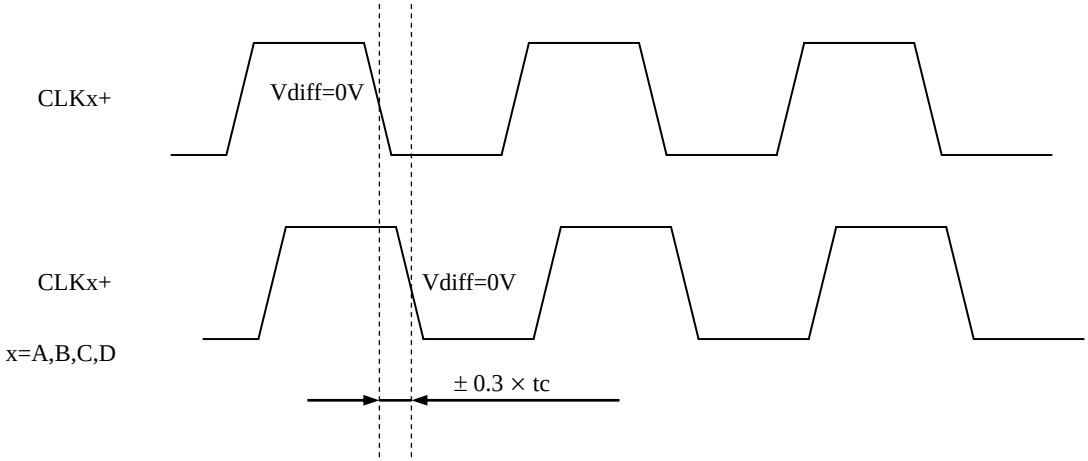
4.10.1 Timing characteristics

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/tc	(60)	77.0	82.5	MHz	-
			tc	-	12.195	-	ns	
	Rise time, Fall time		-	-			ns	Note1
	Duty		-				-	
DATA	CLK-DATA	Setup time	-	-			ns	Note1
		Hold time	-				ns	
	Rise time, Fall time		-				ns	
DE	Horizontal	Cycle	th	6.255	6.753	(9.351)	µs	148.077 kHz (typ.) Note2
				516	520	(720)	CLK	
		Display period	thd	480			CLK	
	Vertical (One frame)	Cycle	tv	7.530	8.340	(10.805)	ms	119.900Hz (typ.)
				1,204	1,235	(1,600)	H	
		Display period	tvd	1,200			H	
	CLK-DE	Setup time	-	-			ns	-
		Hold time	-				ns	
	Rise time, Fall time		-				ns	

Note1: See the data sheet of LVDS transmitter.
Note2: The sum of jitter and skew of horizontal period should be within ±1 CLK.

4.10.2 Input signal timing chart




CLKx+
Vdiff=0V
CLKx+
x=A,B,C,D
Vdiff=0V
± 0.3 × tc

4.11 OPTICS

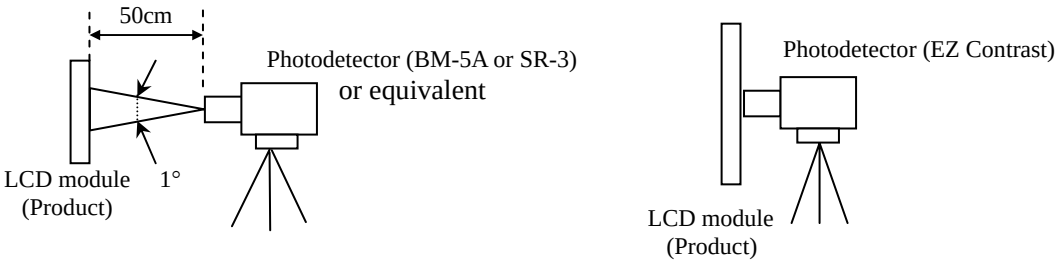
4.11.1 Optical characteristics

(Note1, Note2)

Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks	
Luminance		White at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	L	TBD	(420)	-	cd/m^2	BM-5A or SR-3	-	3
Contrast ratio		White/Black at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	CR	TBD	(900)	-	-	BM-5A or SR-3	Note3	3
Luminance uniformity		White θR = 0°, θL = 0°, θU = 0°, θD = 0°	LU	TBD	(80)	-	%	BM-5A or SR-3	Note4	
Chromaticity	White	**x** coordinate	Wx	TBD	(0.313)	TBD	-	SR-3	Note5	
		y coordinate	Wy	TBD	(0.329)	TBD	-			
Response time		Black to White	Ton	-	(6)	TBD	ms	BM-5A	Note6 Note7	
		White to Black	Toff	-	(6)	TBD	ms			
Viewing angle	Right	θU = 0°, θD = 0°, CR ≥ 10	θR	70	88	-	°	EZ Contrast	Note8	
	Left	θU = 0°, θD = 0°, CR ≥ 10	θL	70	88	-	°			
	Up	θR = 0°, θL = 0°, CR ≥ 10	θU	70	88	-	°			
	Down	θR = 0°, θL = 0°, CR ≥ 10	θD	70	88	-	°			

Note1: These are initial characteristics.
Note2: Measurement conditions are as follows.
Ta=25°C, VDD=12.0V, VDDB=TBDV, Luminance control = maximum, Display mode: WUXGA,
Horizontal cycle= 148.077 kHz, Vertical cycle = 119.900 Hz

Optical characteristics are measured after 20minutes from working the product, in the dark room. Also measurement methods are as follows.



Note3: See "**4.11.2 Definition of contrast ratio**".
Note4: See "**4.11.3 Definition of luminance uniformity**".
Note5: These coordinates are found on CIE 1931 chromaticity diagram.
Note6: Product surface temperature: TopF=TBD°C
Note7: See "**4.11.4 Definition of response times**".
Note8: See "**4.11.5 Definition of viewing angles**".

4.11.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

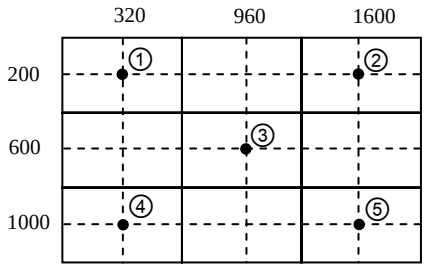
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.11.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

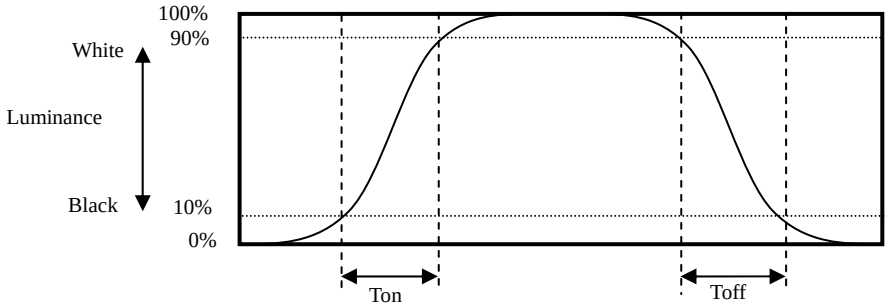
$$\text{Luminance uniformity (LU)} = \frac{\text{Minimum luminance from ① to ⑤}}{\text{Maximum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

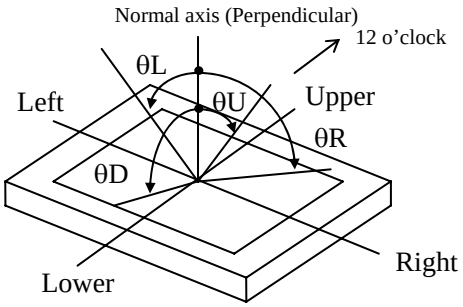


4.11.4 Definition of response times

Response time is measured, the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



4.11.5 Definition of viewing angles

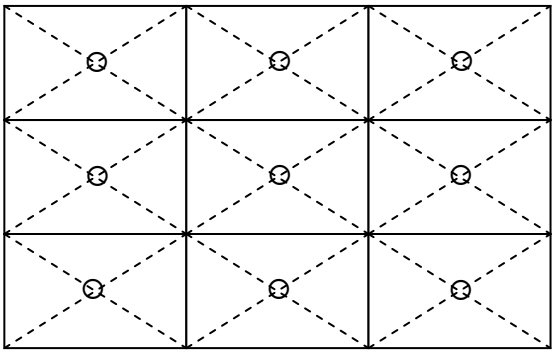


5. RELIABILITY TESTS

Test item	Condition	Judgment Note1
High temperature and humidity (Operation)	① (60) ± 2°C, RH= 60%, 240hours ② Display data is white.	No display malfunctions
Heat cycle (Operation)	① 0 ± 3°C…1hour (50) ± 3°C…1hour ② 50cycles, 4 hours/cycle ③ Display data is white.	
Thermal shock (Non operation)	① (-20) ± 3°C…30minutes (60) ± 3°C…30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
Vibration (Non operation)	① 5 to 100Hz, 11.76m/s^2 ② 1 minute/cycle ③ X, Y, Z direction ④ 10 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)	① 294m/ s^2, 11ms ② X, Y, Z direction ③ 3 times each directions	
ESD (Operation)	① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	No display malfunctions
Dust (Operation)	① Sample dust: No. 15 (by JIS-Z8901)) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.

Note2: See the following figure for discharge points



6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding these contents!**

	This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.
	This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.
	This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS

- **Do not touch the working backlight. There is a danger of an electric shock.**

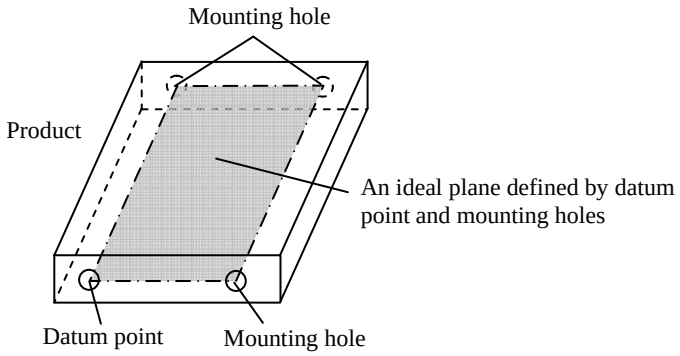
- **Do not touch the working backlight. There is a danger of burn injury.**
- **Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s^2 and to be not greater 11ms, Pressure: To be not greater 19.6N (ϕ16mm jig))**

6.3 ATTENTIONS 

6.3.1 Handling of the product

① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
② Do not hook nor pull cables such as lamp cable, and so on, in order to avoid any damage.
③ When the product is put on the table temporarily, display surface must be placed downward.
④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
⑤ The torque for product mounting screws must never exceed TBDN·m. Higher torque might result in distortion of the bezel.

⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura. Recommended installing method: An ideal plane that is defined by datum point and mounting holes is to be the same plane within ±0.2 mm.



⑦ Do not press or rub on the sensitive product surface. When cleaning the product surface, use of the cloth with ethanolic liquid such as screen cleaner for LCD is recommended.
⑧ Do not push nor pull the interface connectors while the product is working.
⑨ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.
⑩ Usually liquid crystals don't leak through the breakage of glasses because of the surface tension of thin layer and the construction of LCD panel. But, if you contact with liquid crystal for the worst, please wash it out with soap.

3

6.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
② In order to prevent dew condensation occurring by temperature difference, the product packing box should be opened after enough time being left under the environment of an unpacking room. Evaluate the leaving time sufficiently because a situation of dew condensation occurring is changed by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with packing state)
③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
④ This product is not designed as radiation hardened.

6.3.3 Characteristics

The following items are neither defects nor failures.

① Response time, luminance and color may be changed by ambient temperature.
② Display mura, flicker, vertical seam or small spot may be observed depending on display patterns.
③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
⑤ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
⑥ Optical characteristics may be changed depending on input signal timings.
⑦ The interference noise between input signal frequency for this product's signal processing board and luminance control frequency of the inverter may appear on a display. Set up luminance control frequency of the inverter so that the interference noise does not appear.

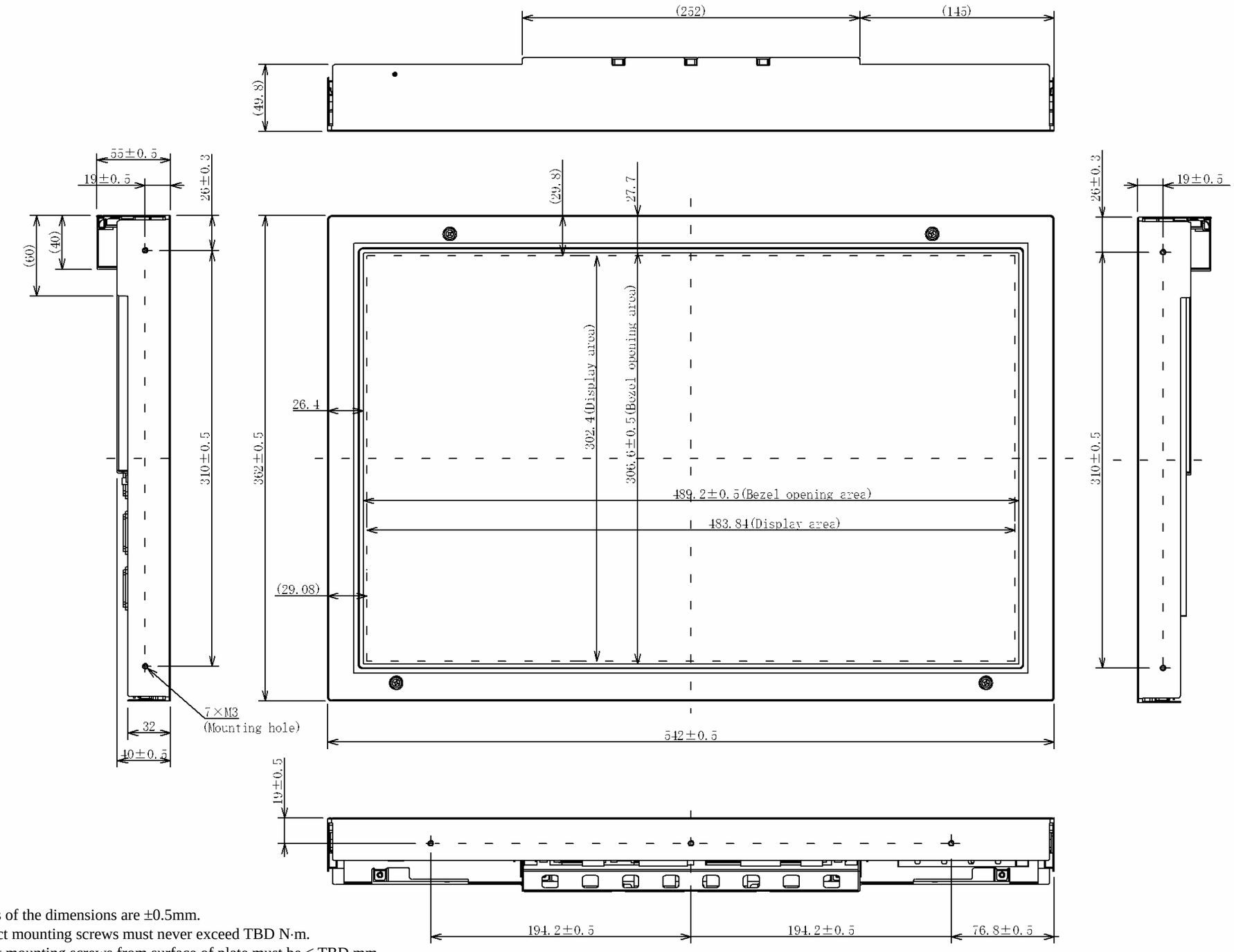
6.3.4 Other

① All GND, GNDB, VDD and VDDB terminals should be used without any non-connected lines.
② Do not disassemble a product or adjust variable resistors.
③ Pack the product with original shipping package, in order to avoid any damages during transportation, when returning the product to NEC for repair and so on.
④ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.

3

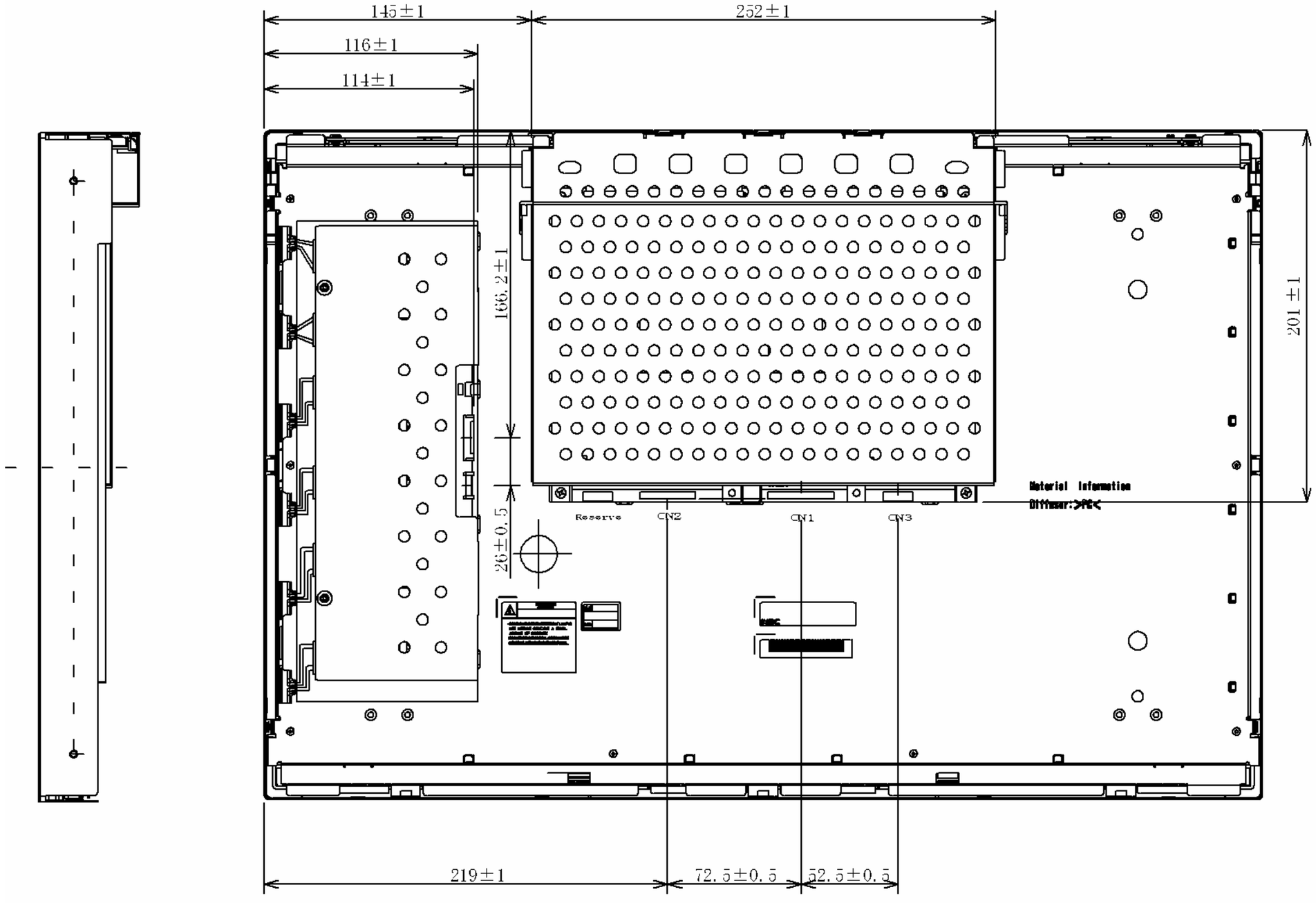
7. OUTLINE DRAWINGS

7.1 FRONT VIEW



Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for product mounting screws must never exceed TBD N·m.
Note3: The length of product mounting screws from surface of plate must be ≤ TBD mm.
Note4: The values in parentheses are for reference.

7.2 REAR VIEW


145±1
116±1
114±1
252±1
166.2±1
201±1
26±0.5
Reserve
CN2
CN1
CN3
Material Information
219±1
72.5±0.5
52.5±0.5

REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Document number	Prepared date	Revision contents and signature
1st edition	DOD-PP-0258	Jun.15, 2007	**Revision contents** New issue **Writer** *Approved by* T. OGAWA *Checked by* ——— *Prepared by* T. OGAWA
2nd edition	DOD-PP-0477	Feb.27, 2008	**Revision contents** P5 General specifications • Module size: TBD →542 (W) × 362 (H) × 40 (D) mm (typ.) / 55.5 (D) mm (max.) • Contrast ratio: (700:1) (typ.) →(800:1) (typ.) • Viewing angle-Right, Left, Up, Down: 85° (typ.) →88° (typ.) • Color gamut: TBD % (typ.) → (77) % (typ.) P7 Mechanical specifications • Module size: TBD →542 ± 0.5 (W) × 362 ± 0.5 (H) × 40 ±0.5 (D), 55.5 (D) (max.) P19 Timing characteristics • CLK- Frequency : TBD MHz (min.) → (60) MHz (min.) • DE- Horizontal- Cycle : TBD μs (max.), TBD CLK (max.) → (9.351) μs (min.), (720) CLK (max.) • DE- Vertical- Cycle : TBD ms (max.), TBD H (max.) → (10.805) ms (max.), (1,600) H (max.) P21 Optical characteristics • Contrast ratio: (700) (typ.) →(800) (typ.) • Luminance uniformity: TBD % (typ.) →(80) % (typ.) • Chromaticity • White-Wx: TBD (typ.) → (0.313) (typ.), -Wy: TBD (typ.) → (0.329) (typ.) • Viewing angle-Right, Left, Up, Down: 85° (typ.) →88° (typ.) P22 Definition of luminance uniformity • Formula: Maximum ←→ Minimum (correction) P28 Front view (addition) P29 Rear view (addition) **Writer** *Approved by* T. OGAWA *Checked by* ——— *Prepared by* T. OGAWA
3rd edition	DOD-PP-0539	May 9, 2008	**Revision contents** P4 Features • Super-Advanced Super Fine TFT (SA-SFT) → Ultra-Advanced Super Fine TFT (UA-SFT) (correction) P5 General specifications • Contrast ratio: (800:1) (typ.) →(900:1) (typ.) • Luminance: (400) cd/m^2 (typ.) → (420) cd/m^2 (typ.) • Color gamut: (77) % (typ.), NTSC color space → (95) % (typ.), Adobe RGB • Power consumption: TBD W (typ.) → (70.32) W (typ.) P5 General specifications P7 Mechanical specifications • Weight: TBD g (typ.) → (3,450) g (typ.) P6 Block diagram • BRTC, BRTH, BRTI, BRTP, PWSEL (addition)

REVISION HISTORY

Edition	Document number	Prepared date	Revision contents and signature
3rd edition	DOD-PP-0539	May 9, 2008	**Revision contents** P8 Electrical characteristics - LCD panel signal processing board • Power supply current: 920 mA (typ.), 1800 mA (max.) → (1,000) mA (typ.), (1,800) mA (max.) P9 Inverter • Power supply voltage: TBD → VDDB, : TBD (min.), TBD (max.) → 11.4V (min.), 12.6V (max.) • Power supply current: TBD (typ.), TBD (max.) → (5,000) mA (typ.), (5,900) mA (max.) P9 Fuse - VBBD (tentative specification) P10 Power supply voltage sequence - Inverter (specified) P12 LCD panel signal processing board – CN1 socket • Pin No.47, 48, 49 (change) • Note3, Note4 (addition) P14-15 Inverter • CN201 socket, Adaptable plug (specified) • CN202 socket, Adaptable plug (addition) P15 Position of socket (specified) P22 Optics - Optical characteristics • Luminance: (400) cd/m^2 (typ.) → (420) cd/m^2 (typ.) • Contrast ratio: (800) (typ.) → (900) (typ.) P25 Reliability tests • High temperature humidity:60±2°C → (60)±2°C • Heat cycle: 55±3°C → (50)±3°C • Thermal shock: -20±3°C → (-20)±3°C, 60±3°C → (60)±3°C P27 Attentions - Handling of the product • (addition) P28 Attentions - Other • (elimination) P29 Front view (addition) • (49.8) (addition) • 40±1 → 40±0.5 P30 Rear view (addition) • 199.4±1, 200.5±1 (elimination) • circular hole (addition) • 201±1 (addition) **Signature of writer** *Approved by* *Checked by* *Prepared by* T. OGAWA E. KATAYAMA