NEC LCD Technologies, Ltd.

TFT COLOR LCD MODULE

NL2432HC22-22A

8.9cm (3.5 Type)

QVGA

DATA SHEET

DOD-PD-0377 (3rd edition)

This DATA SHEET is updated document from DOD-PD-0221 (2).

All information is subject to change without notice. Please confirm the sales representative before starting to design your system.

INTRODUCTION

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The quality grade of this product is ***"Standard"*** unless otherwise specified in this document. If customers intend to use this product for applications other than those specified for ***"Standard"*** quality grade, they should contact NEC sales representative in advance.

CONTENTS

1. DESCRIPTION

The NL2432HC22-22A is a TFT (thin film transistor) active matrix color liquid crystal display (LCD) comprising an amorphous silicon TFT attached to each signal electrode, a driving circuit.
This module is consist of LCD panel, Driver and Backlight.

The 8.9 cm (3.5 Type) diagonal display area contains 240 × 320 pixels and can display 262,144 colors simultaneously.

2. FEATURES

- Transflective type
- Backlight attached
- Recommended LCD controller: Part No. S1L50282F23k100 (NEC corp.)
- High Brightness
- High contrast ratio
- Small footprint and light weight
- 6-bit digital RGB signals

3. APPLICATION

- PDAs
- Portable AV players

4. STRUCTURE AND FUNCTION

Transflective TFT (thin film transistor) color LCD module is comprised of a TFT liquid crystal panel structure with LSIs for driving the TFT array. Sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate creates the TFT panel structure.

RGB (red, green, blue) data signals from a source system are modulated into a form suitable for active-matrix addressing by the signal processor and sent to the driver LSIs, which in turn addresses the individual TFT cells.

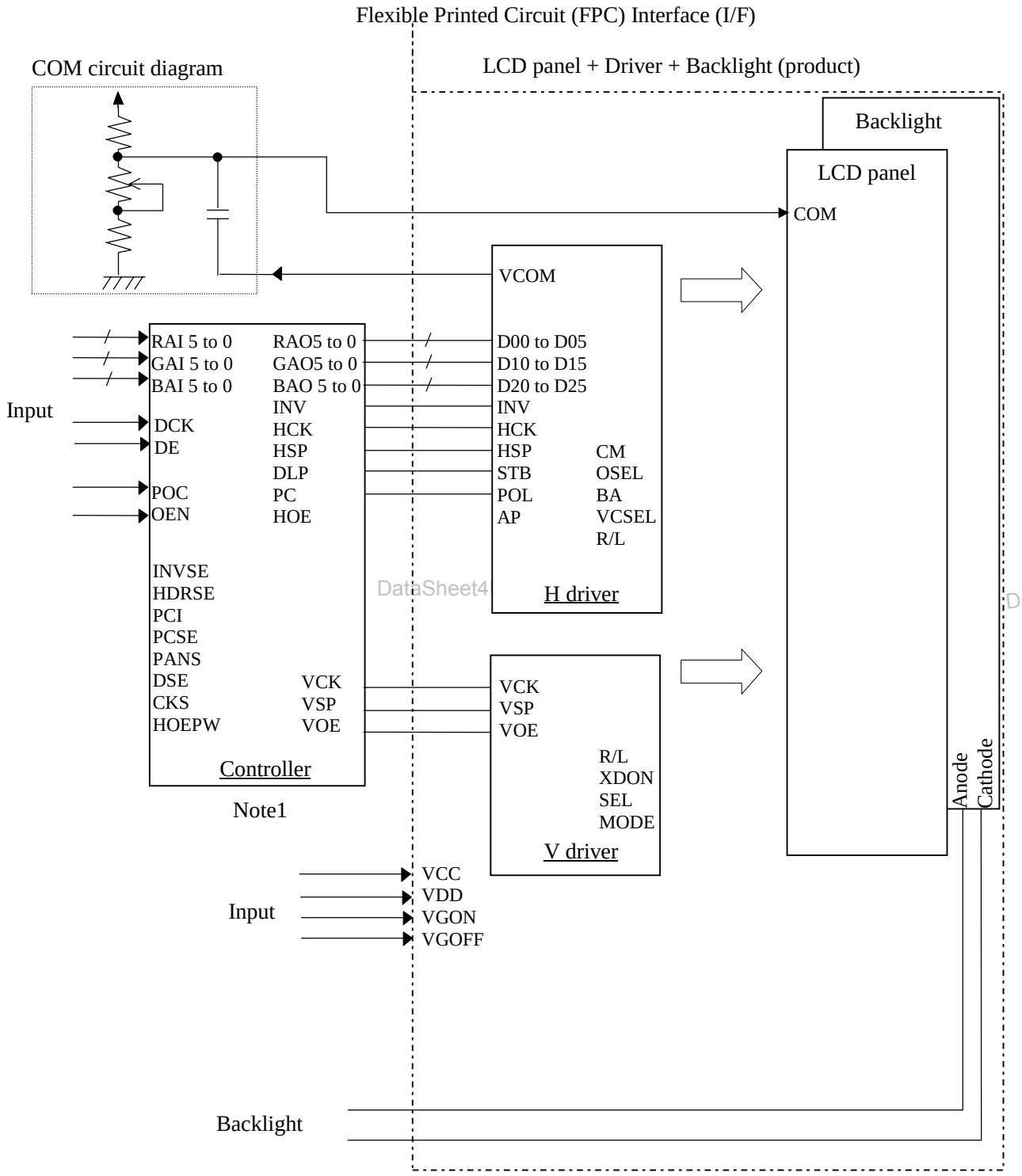
Acting as an Electro-optical switch, each TFT cell regulates light from the natural light and so on when activated by the data source. By regulating the amount of light reflection passing through the array of red, green, and blue dots, color images are created with clarity.

5. GENERAL SPECIFICATIONS

Display area	53.64 (W) × 71.52 (H) mm
Diagonal size of display	8.9 cm (3.5 inches)
Drive system	a-Si TFT active matrix
Display color	262,144 colors
Pixel	240 (H) × 320 (V) pixels
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe
Pixel pitch	0.2235 (W) × 0.2235 (H) mm
Module size	64.0 (H) × 85.0 (V) × 3.06 (D) mm (typ.)
Weight	28 g (typ.)
Contrast ratio	*At transmissive mode* 80:1 (typ., at IL= 18mA)
	At reflective mode 14:1 (typ.)
Reflection ratio	7% (typ.) ☆
Response time	39ms (typ., Ton + Toff)
Luminance	95 cd/m^2 (typ., at IL=18mA) 110 cd/m^2 (typ., at IL=20mA)
Signal system	Controller input (6-bit signals, DCK, DE, POC, OEN) signals Note1
Supply voltage	VCC 3.0V (typ., Logic) VDD 5.0V (typ., LCD H-driving) ☆ VGON +15.0 V (typ., LCD V-driving) VGOFF -15.0 V (typ., LCD V-driving)
Power consumption	LCD panel: 23mW (typ., At VDD=5.0V) ☆ 19mW (typ., At VDD=4.5V, reference) Backlight: 385mW (typ., at IL=18mA) 420mW (typ., at IL=20mA)

Note1: Refer to the controller (Part No.: S1L50282F23k100) specifications.

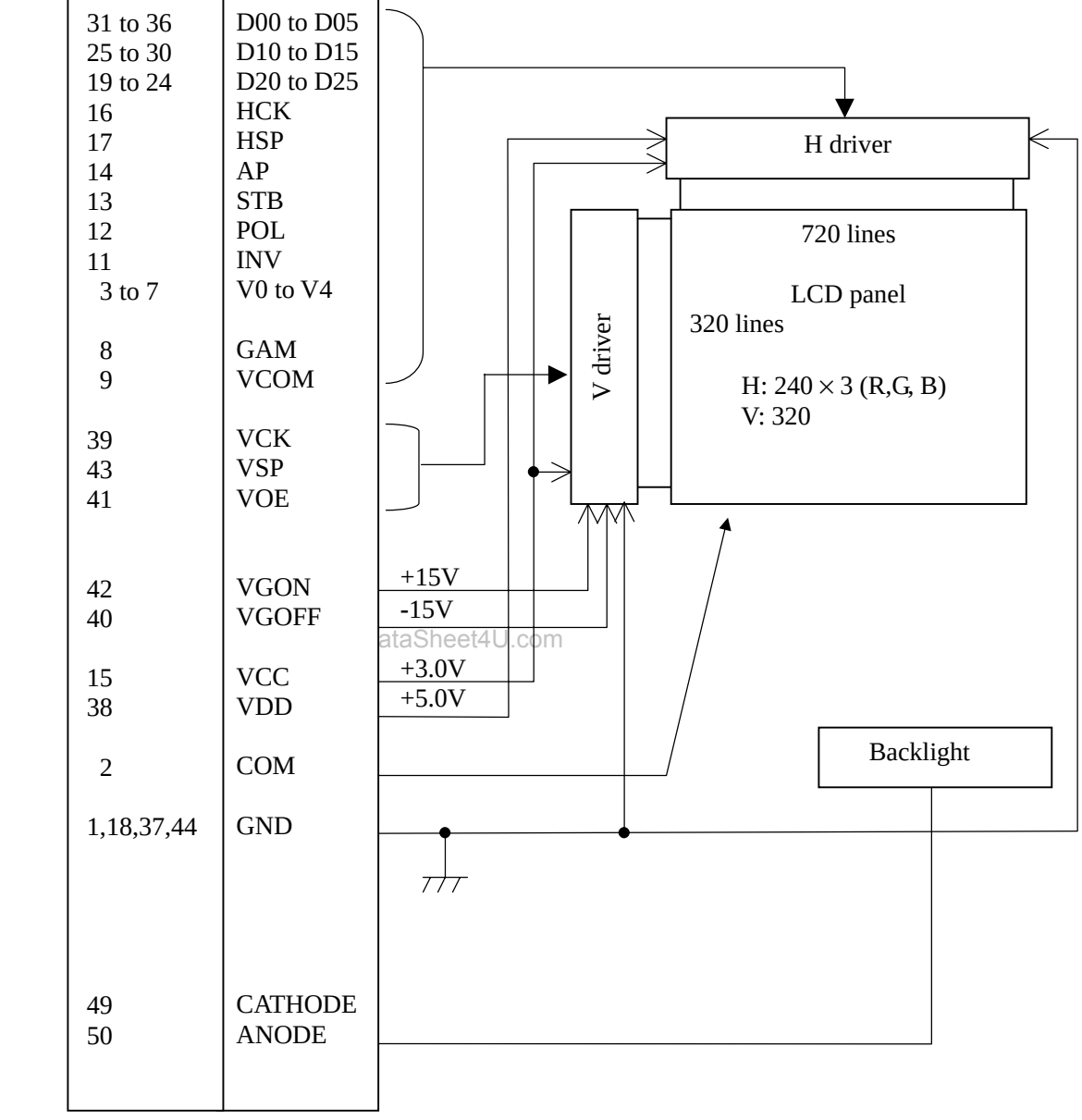
6. BLOCK DIAGRAM



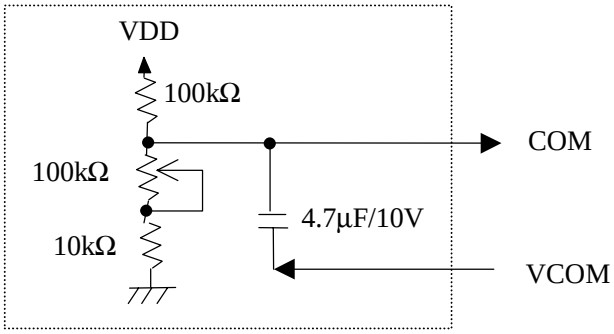
Note1 : Refer to the controller (Part No: S1L50282F23k100) specifications for input timings.

FPC I/F

Pin No.	Symbol
31 to 36	D00 to D05
25 to 30	D10 to D15
19 to 24	D20 to D25
16	HCK
17	HSP
14	AP
13	STB
12	POL
11	INV
3 to 7	V0 to V4
8	GAM
9	VCOM
39	VCK
43	VSP
41	VOE
42	VGON
40	VGOFF
15	VCC
38	VDD
2	COM
1,18,37,44	GND
49	CATHODE
50	ANODE



Reference design of COM circuit



7. GENERAL SPECIFICATIONS

Item	Specification	Unit
Module size	64.0 ± 0.3 (H) ×85.0 ± 0.3 (V) × 3.06 ± 0.2 (D) Note1	mm
Display area	53.64 (H) × 71.52 (V) [Diagonal display area: 8.9 cm (Type 3.5)] Note1	mm
Number of pixels	240 (H) × 320 (V)	pixel
Dot pitch	0.0745 (H) × 0.2235 (V)	mm
Pixel pitch	0.2235 (H) × 0.2235 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	-
Display colors	262,144	color
Weight	28 (Typ.)	g

Note1: Refer to **"17 OUTLINE DRAWINGS".**

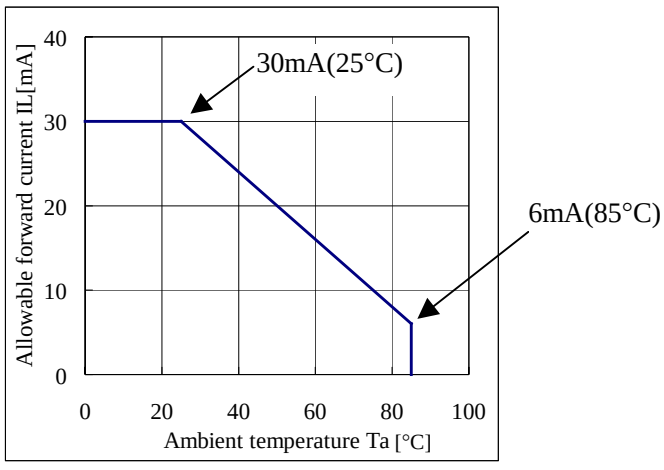
8. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remarks
Supply voltage	VCC	-0.3 to +4.0	V	Ta = 25 °C
	VDD	-0.3 to +6.0	V	
	VGON	-0.3 to +44.0		
	VGOFF	VGON - 44.0 to +0.3		
Logic input voltage	VI	-0.3 to VCC+0.3	V	Logic signals
γ control voltage	V0 to V4	-0.3 to VDD+0.3	V	-
Reverse voltage (Backlight)	VR	≤ 30	V	Ta = 25 °C
Power Dissipation (Backlight)	PD	≤ 720	mW	
Forward current (Backlight)	IL	Note3	mA	-
Storage temperature	Tst	-20 to +70	°C	-
Operating temperature	Top	-10 to +55		Product surface Note1
Relative humidity Note2	RH	≤ 95	%	Ta≤ 40°C
		≤ 85		40°C <Ta≤ 50°C
Absolute humidity Note2	AH	≤ 70 Note4	g/m^3	Ta>50°C
Storage altitude		≤ 13,600	m	-20°C ≤ Ta ≤ 70°C
Operating altitude		≤ 4,850	m	-10°C ≤ Ta ≤ 55°C

Note1: Measure at the display area

Note2: No condensation

Note3:



Note4: Ta= 50°C, RH= 85%

9. ELECTRICAL CHARACTERISTICS

(1) Logic/ LCD driving (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Logic supply voltage	VCC	2.6	3.0	3.6	V	-
H driver supply voltage	VDD	4.25	5.0	5.25	V	-
V driver(+) supply voltage	VGON	14.0	15.0	16.0	V	-
V driver(-) supply voltage	VGOFF	-16.0	-15.0	-14.0	V	-
Logic input high voltage	VIH	0.7×VCC	-	VCC	V	Logic signal
Logic input low voltage	VIL	0	-	0.3×VCC	V	
COM voltage input range	COM	VDD	-	-	Vp-p	-
COM center voltage	COM/C	-	1.6	-	V	At VDD=5.0V Note1
		-	1.2	-	V	At VDD=4.5V reference Note1
VCC supply current	ICC	-	0.2	0.3	mA	At VCC= 3.0 V Note2 Not include the controller
VDD supply current	IDD	-	4.2	8.0	mA	At VDD = 5.0V AP pulse width = 15µs Note2
		-	3.5	7.0	mA	At VDD = 4.5V AP pulse width = 15µs reference Note2
VGON supply current	IGON	-	0.04	0.1	mA	At VGON=+15.0 V Note2
VGOFF supply current	IGOFF	-	-0.04	-0.1	mA	At VGOFF= -15.0 V Note2

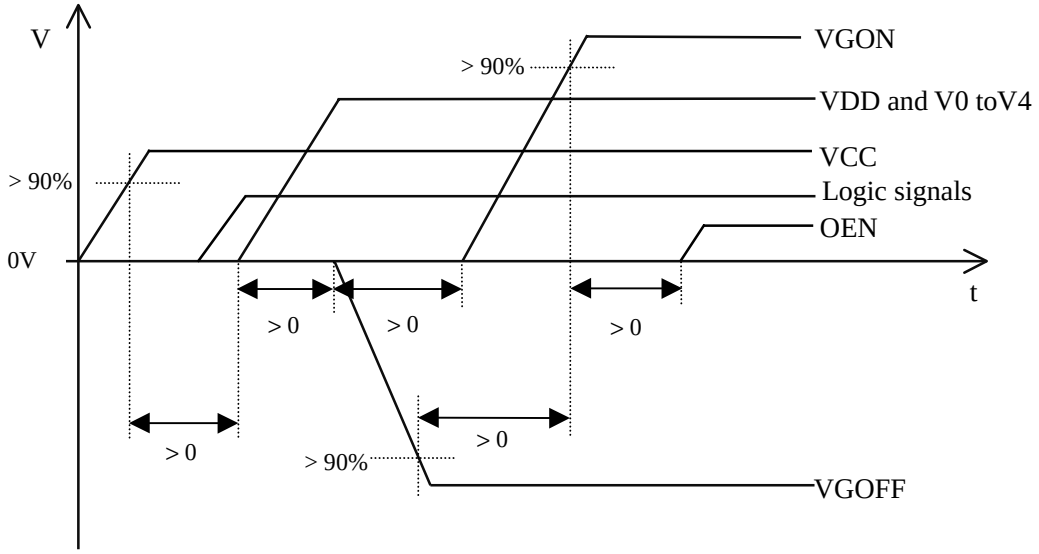
Note1: An optimal value for COM/C
At VDD = 5.0V: 1.1V to 2.1V
At VDD = 4.5V: 0.7V to 1.7V (reference)

Note2: HCK= 5.6MHz, STB= 19.44kHz, VCK= 19.44kHz, VSP= 60Hz,
Checkered flag pattern (by EIAJ ED-2522)

(2) Backlight (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Forward Current	IL	-	18	20	mA	-
Forward Voltage	VL	17.6	21.2	23.8	V	At IL=18mA

10. SUPPLY VOLTAGE SEQUENCE



Remark 1: Supply voltage sequence must be kept according to the above timings. And when it is turned off, the sequence must be reversed.

Remark 2: The “OEN” signal of the controller must be “H” after VGON is supplied.

Remark 3: All signals should not be stopped during the operation. Even if the signals recover, the product may not be operated correctly. In this case, reset the sequence again.

11. INTERFACE PIN CONNECTIONS

CN1 (FPC)
Adaptable socket: FH12-50S-0.5SH(05) (HIROSE ELECTRIC CO.,LTD.)

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	26	D11	Green data
2	COM	Signal for common electrode	27	D12	Green data
3	V0	External gamma setting voltage (These pins must be Open when GAM pin is "L".)	28	D13	Green data
4	V1		29	D14	Green data
5	V2		30	D15	Green data (MSB)
6	V3		31	D00	Red data (LSB)
7	V4		32	D01	Red data
8	GAM	Gamma selection switch	33	D02	Red data
9	VCOM	Driver output signal	34	D03	Red data
10	N.C.	No connection (Keep this pin Open.)	35	D04	Red data
11	INV	Data inversion signal	36	D05	Red data (MSB)
12	POL	Polarity reversal signal	37	GND	Ground
13	STB	H driver latch signal	38	VDD	H driver voltage
14	AP	H driver inhibition signal	39	VCK	V driver shift clock
15	VCC	Logic voltage	40	VGOFF	V driver OFF voltage
16	HCK	H driver shift clock	41	VOE	V driver output enable ("L" output)
17	HSP	H driver start pulse	42	VGON	V driver ON voltage
18	GND	Ground	43	VSP	V driver start pulse
19	D20	Blue data (LSB)	44	GND	Ground
20	D21	Blue data	45	N.C.	No connection (Keep these pins Open.)
21	D22	Blue data	46	N.C.	
22	D23	Blue data	47	N.C.	
23	D24	Blue data	48	N.C.	
24	D25	Blue data (MSB)	49	CATHODE	LED voltage (Cathode)
25	D10	Green data (LSB)	50	ANODE	LED voltage (Anode)

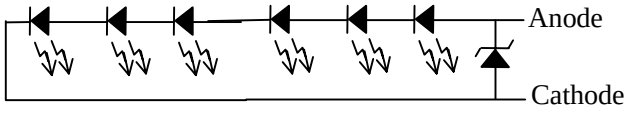
Description of pin functions

Pin	Description
COM	This is the Common voltage. The voltage needs to be adjusted. See "**6 BLOCK DIAGRAM - Reference design of COM circuit**".
V0 to V4	Provide the gamma setting voltages from outside. Maintain the following voltage relationships. VSS ≤ V4 ≤ V3 ≤ V2 ≤ V1 ≤ V0 ≤ VDD
GAM	H: External gamma setting voltage (V0-V4) is valid. L: External gamma setting voltage (V0-V4) is invalid. (Internal gamma setting is valid.)
VCOM	This pin inverts the signal input from the POL pin and outputs it following conversion to the VDD potential at the rising edge of STB.
INV	This pin inverts the input data signal. Input data in synchronization with the shift clock. INV = L: Normal, INV = H: Data inversion
POL	This pin inverts the output polarity. The polarity inversion signal data is captured at the rising edge of STB. The gamma-resistor is switched in accordance with the positive/negative polarity. POL = H: Positive polarity POL = L: Negative polarity

To be continued

Continued

Pin	Description
STB	A timing signal that latches the contents of the data register. When an H level is read at the rising edge of HCK, the contents of the data register are latched and transferred to the D/A converter, and analog voltage corresponding to the display data is output. Also, because the internal operation via HCK continues even after the STB latch, do not stop HCK. The contents of the shift register are cleared at the rising edge of STB.
AP	This pin turns on/off the BIAS circuit and turns on the output SW and amplifier. When AP is H, the amplifier is set and the product is driving. The amplifier output and output SW are turned on at the rising edge of AP, starting the product drive. Note that the output SW is turned off at the rising edge of STB and the output becomes Hi-Z.
HCK	This pin is the shift clock input of the column shift register. Display data is captured into the data register at the rising edge.
HSP	Fetching of display data starts when H is read at the rising edge of HCK.
VCK	This pin is the shift clock input of the gate shift register. The start pulse is captured at the rising edge of clock and output the pulse at the falling edge.
VOE	This pin controls the output of the gate drivers. Output can be controlled regardless of VSP and VCK.
VSP	This pin synchronizes with the frame and the gate driver.
ANODE CATHODE	Refer to the below “Circuits of backlight”.



Circuits of backlight

Remark: Do not fold the FPC. When folding the FPC, pattern disconnection may be caused. In case of bending FPC, the minimum curvature (R) must be more than 1.0 mm.

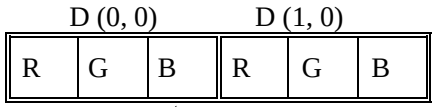
12. DISPLAY COLORS vs. DISPLAY POSITIONS

(1) Display colors

Display colors		Data signal(0: Low level, 1: High level)																	
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑				:						:						:		
	↓				:						:						:		
	bright	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	↑				:						:						:		
	↓				:						:						:		
	bright	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
		0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑				:						:						:		
	↓				:						:						:		
	bright	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Remark: Colors are developed in combination with 6-bit signals (64 steps in grayscale) of each primary red, green, and blue color.
This process can result in up to 262,144 (64×64×64) colors.

(2) Display positions of input data



D(0, 0)	D(1,0)	•••	D(239,0)
D(0,1)	D(1, 1)	•••	D(239,1)
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
D(0, 319)	D(1, 319)	•••	D(239,319)

13. INPUT SIGNAL TIMINGS

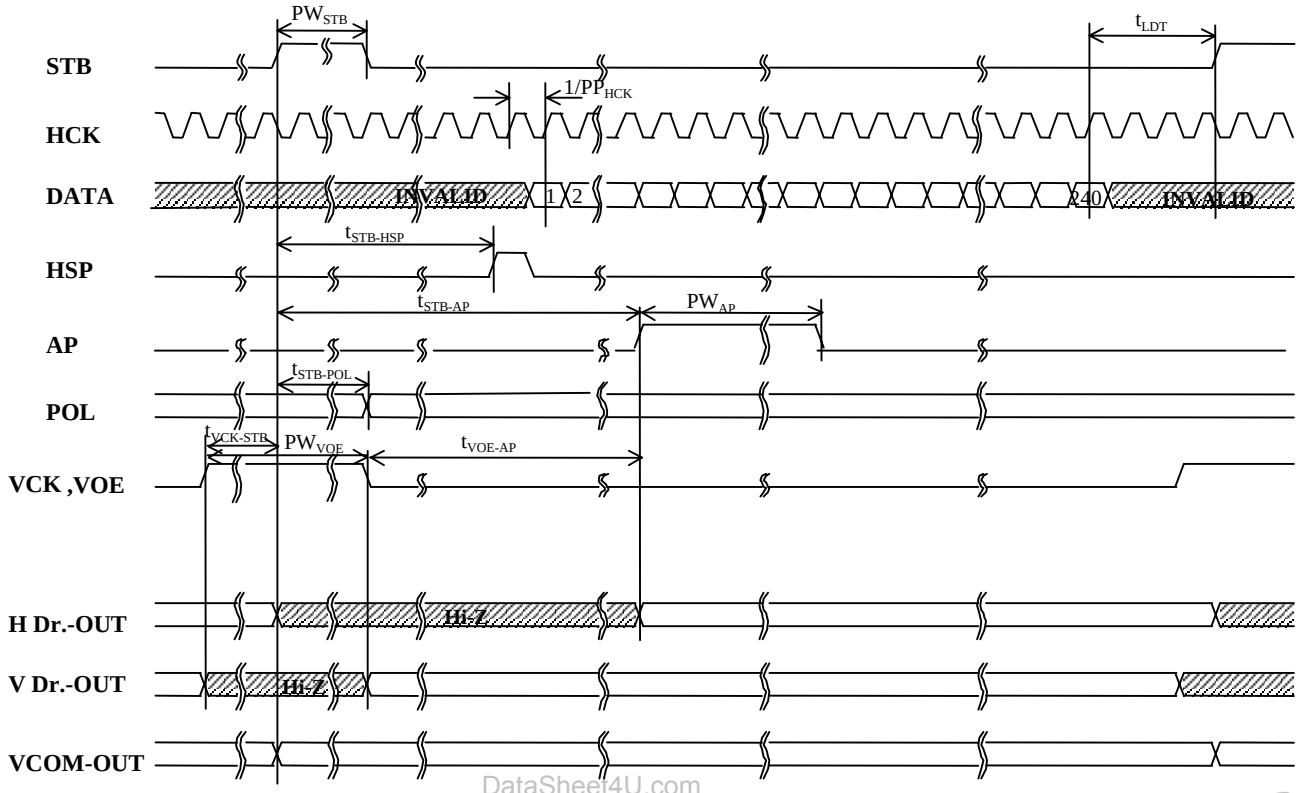
Input signal specifications (Ta=25°C, VCC=3.0V, VDD=5.0V) ☆

(1) Timing characteristics

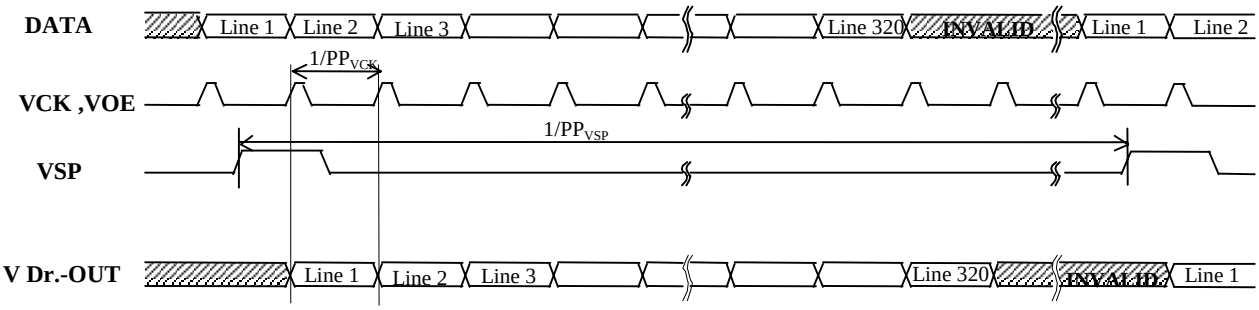
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
H Clock frequency	PPHCK	5.4	5.6	7.2	MHz	-
Last data timing	tLDT	2	-	-	CLK	-
STB frequency	PPSTB	16.5	19.44	20.0	kHz	-
STB pulse width	PWSTB	550	-	-	ns	-
STB-HSP time	tSTB-HSP	4	-	-	CLK	-
STB-AP time	tSTB-AP	10	-	-	µs	-
AP pulse width	PWAP	15	-	-	µs	-
VOE-AP time	tVOE-AP	0	10	-	µs	-
STB-POL time	tSTB-POL	40	-	-	ns	-
VCK-STB time	tVCK-STB	1	3	-	µs	-
VSP frequency	PPVSP	50	60	65	Hz	-
V Clock frequency	PPVCK	16.5	19.44	20	kHz	-

Remark: All parameters should be kept within the specified range.

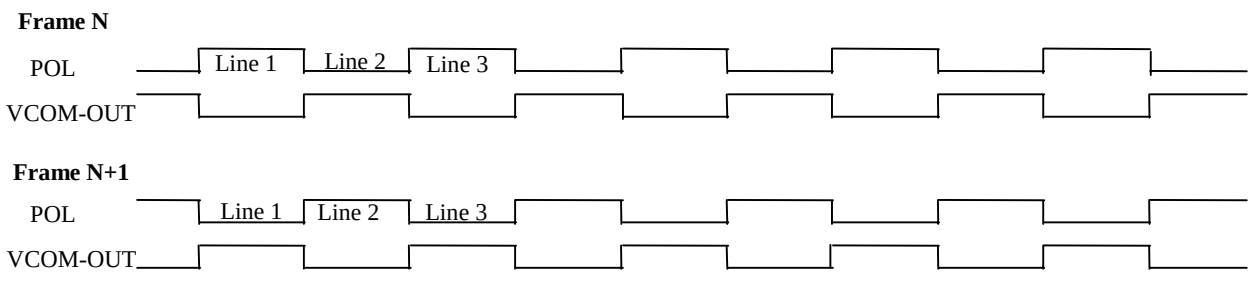
(2) Horizontal timing chart



(3) Vertical timing chart



(4) Polarity of signal "POL"



Note1: Unless otherwise specified, the input level is defined to be VIH= 0.7VCC, VIL= 0.3VCC.

14. OPTICAL CHARACTERISTICS

< Backlight turning off> Note1

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Contrast ratio	CR	-	7	14	-	-	Note2,3
Reflection ratio	RE	-	5	7	-	%	Note3 ☆

Reference data Note1

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Remarks
Chromaticity coordinates	W	White (x, y)		-	(0.31,0.32)	-	-	Note3
Color gamut	C	-		-	5	-	%	Remark1 Note3
Response time	Ton	White to black	90%→ 10%	-	14	28	ms	Note6
	Toff	Black to white	10%→ 90%	-	25	50		

< Backlight turning on > Note1

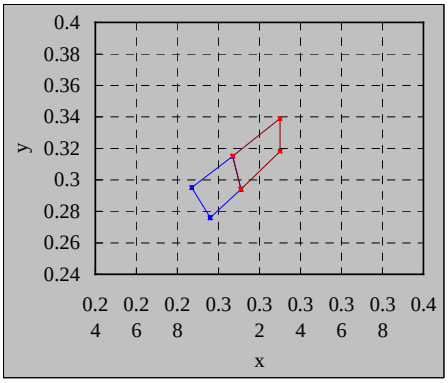
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Contrast ratio	CR	IL= 18mA	50	80	-	-	Note2, 4
Luminance	L	IL= 18mA	75	95	-	cd/m^2	Note4
Luminance uniformity	LU	Maximum luminance: 100%	60	70	-	%	Note5

Reference data Note1

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Remarks
Chromaticity coordinates	W	White (x, y)		(0.26,0.27)	(0.31,0.32)	(0.36,0.37)	-	Remark2 Note4
Color gamut	C	IL= 18mA		35	40	-	%	Remark1 Note4
Response time	Ton	White to black	90%→ 10%	-	14	28	ms	Note6
	Toff	Black to white	10%→ 90%	-	25	50		
Viewing angle	Right	θU=0°, θD=0° CR>2		-	55	-	°	Note7
	Left	θU=0°, θD=0° CR>2		-	55	-	°	
	Up	θR=0°, θL=0° CR>2		-	40	-	°	
	Down	θR=0°, θL=0° CR>2		-	45	-	°	

Remark1: Against NTSC color space

Remark2: The chromaticity coordinates of White are deviated by the LED deviation in addition to color filter deviation. (See following figure.)



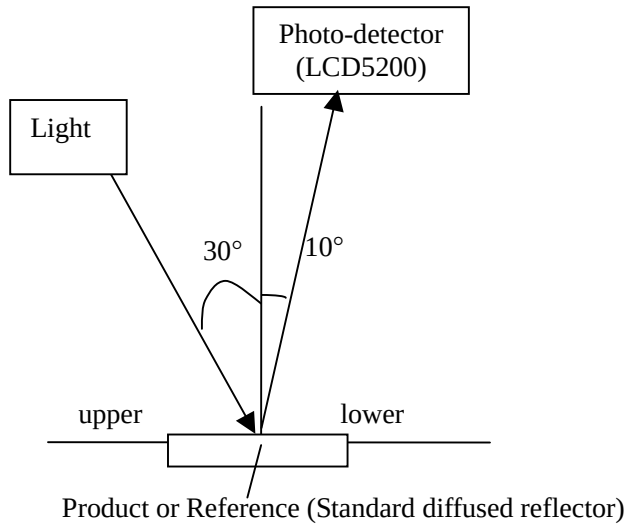
Chromaticity coordinates of LED

Note1 : Ta = 25°C, VCC=3.0V, VDD=5.0V, IL=18mA

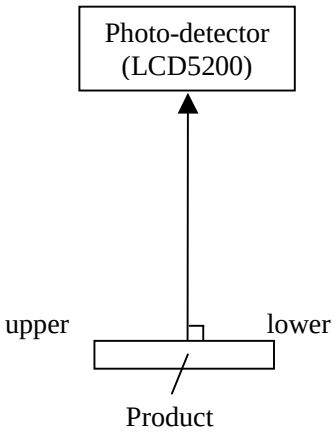
Note2 : The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Reflection ratio (Luminance) with all pixels in "white"}}{\text{Reflection ratio (Luminance) with all pixels in "black"}}$$

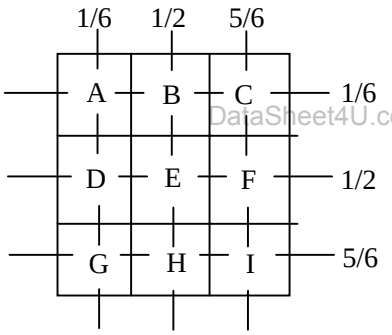
Note3: Contrast ratio, Chromaticity coordinates, Color gamut and Reflection ratio are measured as follows.



Note4: Contrast ratio, Chromaticity coordinates, Color gamut and Luminance are measured as follows.

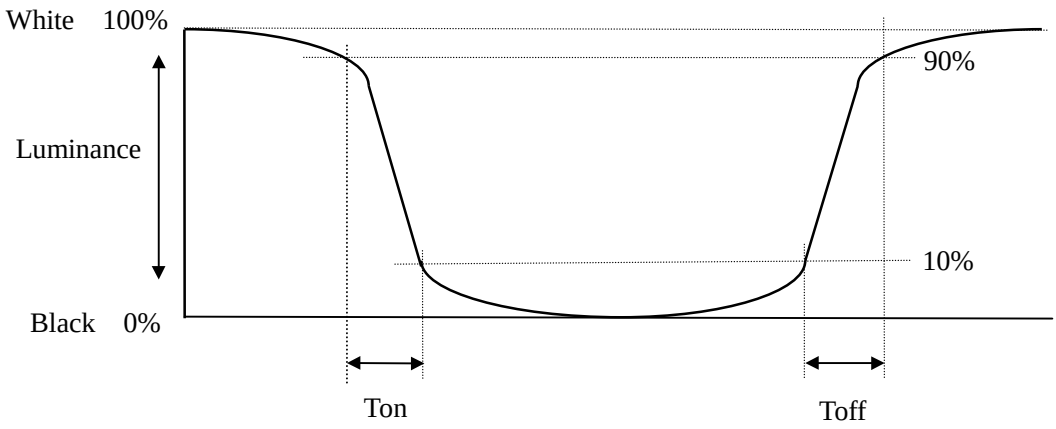


Note5: Luminance uniformity is calculated by using the following formula.

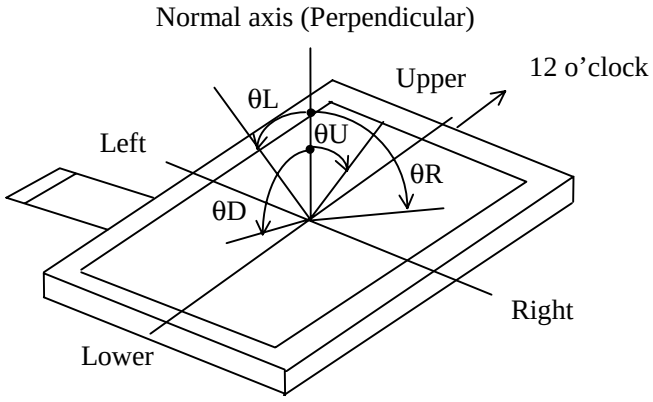


$$\text{Luminance uniformity (\%)} = \frac{\text{Minimum luminance from A to I}}{\text{Maximum luminance from A to I}} \times 100$$

Note6: Definition of response times is as follows.
Photo-detector output signal is measured when the luminance changes "white" to "black" or “black” to “white”.



Note7: Definition of viewing angle is as follows.



15. RELIABILITY TESTS

Test item	Condition	Judgment Note1
High temperature and humidity (Operation)	1) 55 ± 2°C, RH = 85%, 240hours 2) Display data is black.	No display malfunctions
Heat cycle (Operation)	1) -10 ± 3°C…1 hour 55 ± 3°C…1 hour 2) 50 cycles, 4 hours/cycle 3) Display data is black.	
Thermal shock (Non operation)	1) -20 ± 3°C…30 minutes 70 ± 3°C…30 minutes 2) 100 cycles, 4 hour/cycle 3) Temperature transition time is within 5 minutes.	
Low pressure (Non operation)	1) 15 kPa 2) -20 ± 3°C…24 hours 3) 70 ± 3°C…24 hours	
Low pressure (Operation)	1) 53.3 kPa 2) -10 ± 3°C…24 hours 3) 55 ± 3°C…24 hours	
ESD (Operation)	1) 150pF, 150Ω, ±10kV 2) 3 places on a panel surface 3) 10 times each place at 1s interval	
Dust (Operation)	1) Sample dust No.15 (by JIS-Z8901) 2) 15 seconds stir 3) 8 times repeat at 1 hour interval	
Vibration (Operation)	1) 30 to 100Hz, 19.6m/s^2 (2G) 2) 30 minutes/cycle 3) X, Y, Z direction 4) 1 time each direction	No display malfunctions No physical damages
Mechanical shock (Non operation)	1) 3920m/ s^2 (400 G), 2.5ms 2) X, Y, Z direction 3) 1 time each direction	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect specifications.

16. PRECAUTIONS

The following statements are very important, be sure to understand the following information.

This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

(1) Handling of the product

① Take hold of both ends without touch the FPC when customer pulls out products (LCD modules) from the tray.

② Take the measures of electrostatic discharge such as earth band, ionic shower and so on, when customer deals with the product, because products may be damaged by electrostatic.

③ 

Since the LCD panel is made from fragile glass materials, impulse and pressure to the product must be avoided.

④ As the surface of the panel is easily scratched, use a soft dry cloth without chemicals for cleaning.

⑤ Do not push/pull the FPC while the product is working, because wrong power sequence may break down the product.

⑥ Put the product rear side down on a flat horizontal plane.

⑦ Handle the FPC with care.

⑧ When the product is operating, do not loose the logic signals. If any one or more of these signals were lost, the product would be damaged.

⑨ Flexing or adding pressure to the product will result in a non-uniformity image. When the product is mounted to customer chassis, evaluate the display condition carefully.

⑩ Do not fold the FPC. When folding the FPC, pattern disconnection may be caused. In case of bending FPC, the minimum curvature (R) must be more than 1.0 mm.

(2) Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product on the tray in antistatic pouch in room temperature, because of avoidance for dusts and sunlight, if customer stores the product.

② In order to prevent dew condensation occurring by temperature difference, the product packing box must be opened after leave under the environment of an unpacking room temperature enough. Because a situation of dew condensation occurring is changed by the environmental temperature and humidity, evaluate the leaving time sufficiently. (Recommendation leaving time: 6 hour or more with packing state)

③ Do not operate in high magnetic field. Circuit boards may be broken down by it.

④ This product is not designed as radiation hardened.

(3) Characteristics

① Response time, luminance and color may be changed by ambient temperature.

② Do not display the fixed pattern for a long time because it may cause image sticking.

③ The LCD may be seemed luminance non-uniformity, flicker, vertical seam or small spot by display patterns.

④ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, because the product has LED backlight.

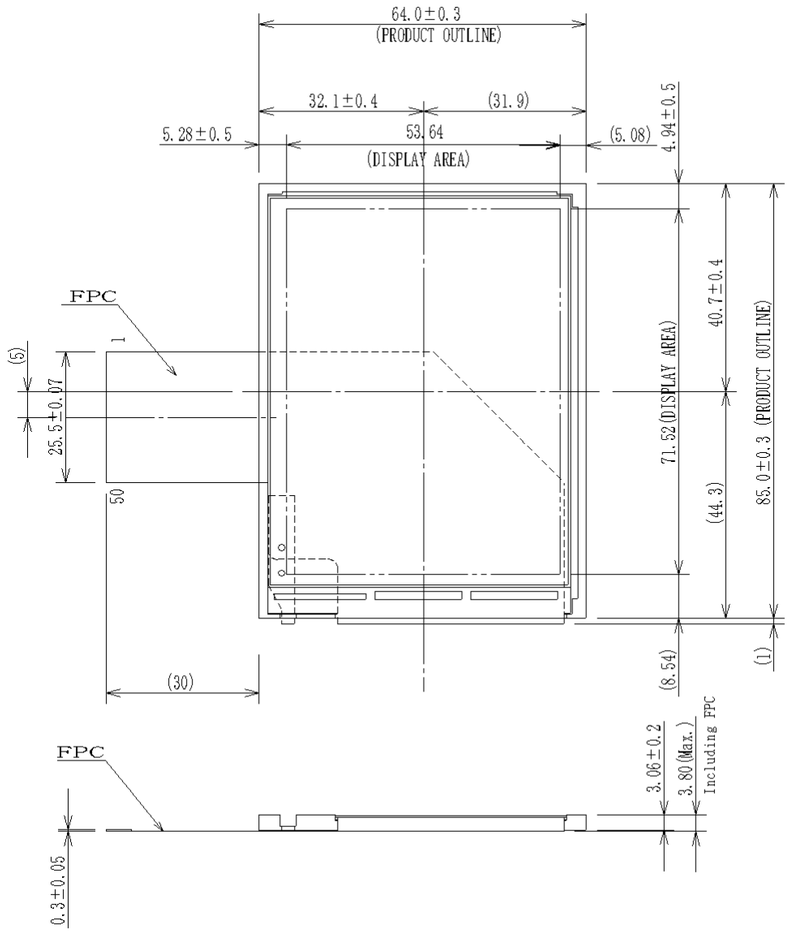
(4) Other

① Do not disassemble and/or reassemble the product.

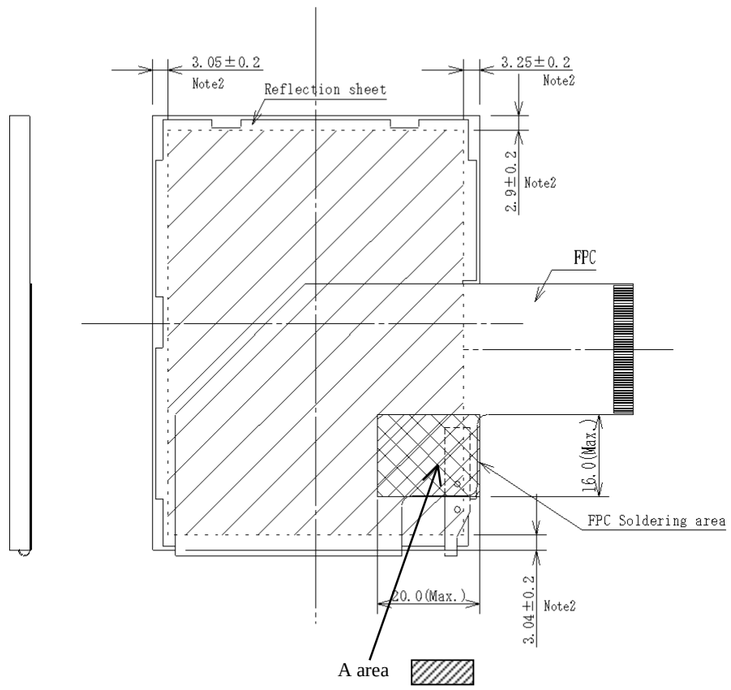
② Pack the product with original shipping package, because of avoidance of some damages during transportation, when customer returns it to NEC for replacement and so on.

17. OUTLINE DRAWINGS

FRONT VIEW



REAR VIEW



Pin No.	Symbol	Pin No.	Symbol
1	GND	26	D11
2	COM	27	D12
3	V0	28	D13
4	V1	29	D14
5	V2	30	D15
6	V3	31	D00
7	V4	32	D01
8	GAM	33	D02
9	VCOM	34	D03
10	N.C.	35	D04
11	INV	36	D05
12	POL	37	GND
13	STB	38	VDD
14	AP	39	VCK
15	VCC	40	VGOFF
16	HCK	41	VOE
17	HSP	42	VGON
18	GND	43	VSP
19	D20	44	GND
20	D21	45	N.C.
21	D22	46	N.C.
22	D23	47	N.C.
23	D24	48	N.C.
24	D25	49	CATHODE
25	D10	50	ANODE

Note1: The values in parentheses are for reference.
Note2: Frame width of product chassis
Note3: When installing the product to the customer equipment, do not apply undue stress to the A area, FPC and FPC Soldering area.
If not, it may cause display un-uniformity or product breaking.

(Unit: mm)