PRELIMINARY

NEC LCD Technologies, Ltd.

TFT COLOR LCD MODULE

NL256204AC15-02

2

51cm (20.1 Type)
QSXGA

PRELIMINARY DATA SHEET

DOD-PD-0081 (2nd edition)

This PRELIMINARY DATA SHEET is updated document from DOD-M-1312(1).

All information is subject to change without notice. Please confirm the sales representative before starting to design your system.

INTRODUCTION

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Specific: Military systems, aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems (medical equipment, etc.) and any other equipment

The quality grade of this product is ***"Standard"*** unless otherwise specified in this document. If customers intend to use this product for applications other than those specified for ***"Standard"*** quality grade, they should contact NEC sales representative in advance.

CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

NL256204AC15-02 module is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Color (Red, Green, Blue) data signals from a host system (e.g. PC, signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

1.2 APPLICATIONS

- EWS monitors
- Monitors for CAD system

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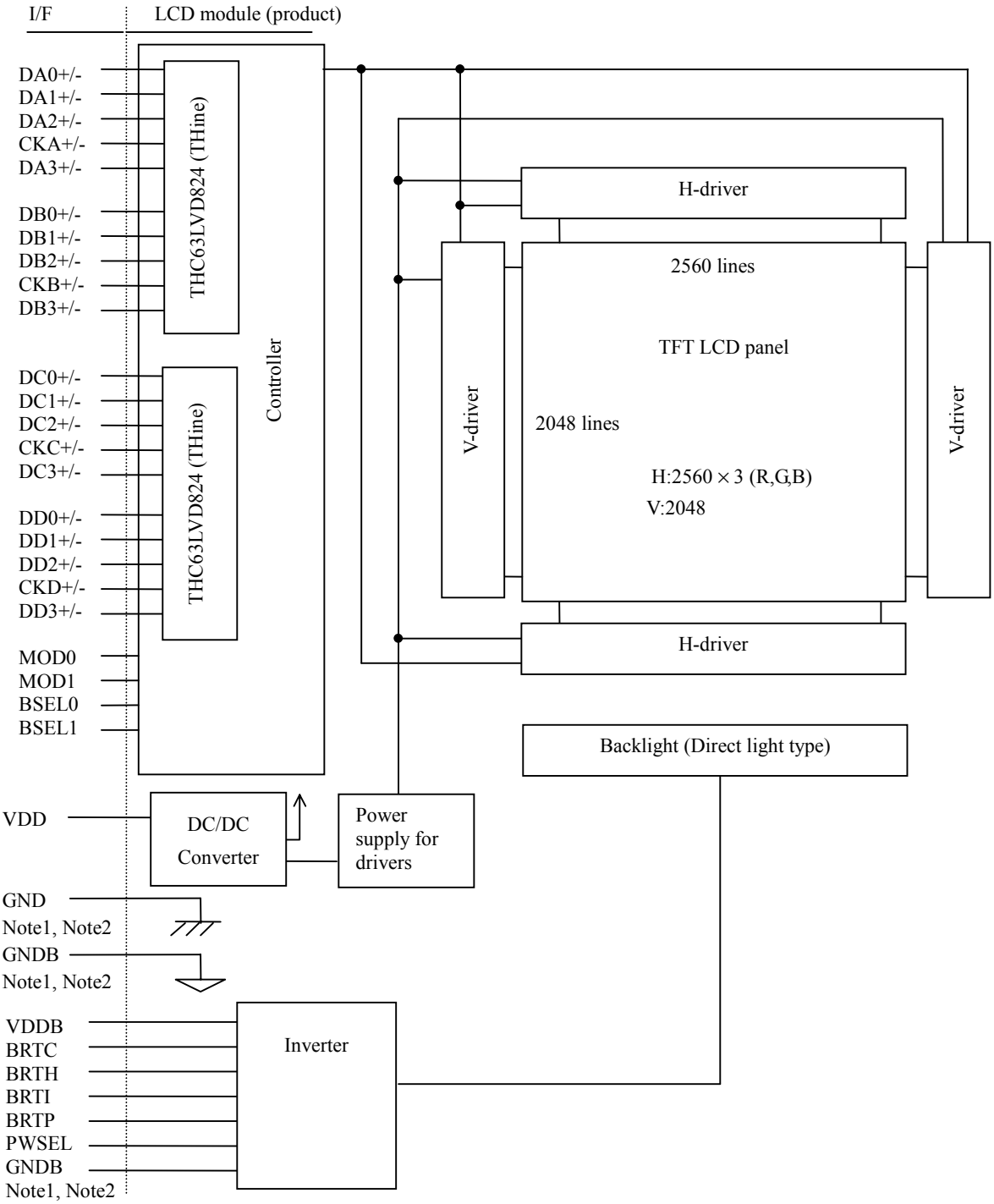
1.3 FEATURES

- Ultra-wide viewing angle (with lateral electric field)
- High resolution
- Low reflection
- LVDS interface
- Selectable 3 types of LVDS data bit mapping mode
- Selectable 2 types of LVDS data transmission mode
- Adjustable Gamma characteristics by 10-bit look up table
- High luminance
- Small foot print
- Incorporated direct type backlight
- Replaceable backlight unit
- Replaceable inverter

2. GENERAL SPECIFICATIONS

Display area	399.36 (W) × 319.49 (H) mm (typ.)	
Diagonal size of display	51 cm (20.1 inches)	
Drive system	a-Si TFT active matrix	
Display color	16,777,216 colors	
Pixel	2560 (H) × 2048 (V) pixels	
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe	
Dot pitch	0.052 (W) × 0.156 (H) mm	
Pixel pitch	0. 156 (W) × 0. 156 (H) mm	
Module size	423.4 (W) × 343.5 (H) × 43.5 (D) mm (typ.)	
Weight	2440 g (typ.)	2
Contrast ratio	450:1 (typ.)	
Viewing angle	*At the contrast ratio 10:1* • Horizontal: Right side 85° (typ.), Left side 85° (typ.) • Vertical: Up side 85° (typ.), Down side 85° (typ.)	
Designed viewing direction	Viewing angle with optimum grayscale (γ=2.2): normal axis	
Polarizer surface	Antiglare	
Polarizer pencil-hardness	2H (min.) [by JIS K5400]	
Color gamut	*At LCD panel center* 72 % (typ.) [against NTSC color space]	
Response time	*Ton (black 10%→ white 90%)* TBD ms (typ.)	2
Luminance	220 cd/m^2 (typ.)	
Signal system	4 ports LVDS interface (Equivalent of THC63LV824×2pcs, THine Electronics, Inc.) RGB 8-bit signals, Data enable signal (DE), Dot clock (CLK)	
Power supply voltage	LCD panel signal processing board: 12.0V Backlight inverter: 12.0V	
Backlight	Direct light type: 12 cold cathode fluorescent lamps with an inverter (Replaceable parts • Backlight unit: Type No.: TBD • Inverter: Type No.: 201PW121)	2
Power consumption	*At checkered flag pattern and maximum luminance* 49.2 W (typ.)	

3. BLOCK DIAGRAM



Note1: Connections between GND (Signal ground), FG (Frame ground) and GNDB (Backlight inverter ground) in the LCD module

GND - FG	Not connected
GND - GNDB	Not connected
FG - GNDB	Not connected

Note2: GND, FG and GNDB should be connected together in customer equipment.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	423.4 ± 1.0 (W) × 343.5 ± 1.0 (H) × 43.5 ± 1.0 (D) Note1	mm
Display area	399.36 (W) × 319.488 (H) Note1	mm
Weight	2440 (typ.), 2600 (max.)	g

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Note1: See "**7. OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter			Symbol	Rating	Unit	Remarks
Power supply voltage		LCD panel signal processing board	VDD	-0.3 to +15.0	V	Ta = 25°C
		Backlight inverter	VDDB	-0.3 to +15.0	V	
Input voltage for signals	LCD panel signal processing board	Display signals Note1	VD	-0.3 to +3.6	V	Ta = 25°C VDD=12.0V
		Function signal 1 Note2	VF1	-0.3 to +3.9	V	
		Function signal 2 Note3	VF2			
	Backlight inverter	BRTI signal	VBI	-0.3 to +1.5	V	Ta = 25°C VDDB = 12.0V
		BRTP signal	VBP	-0.3 to +5.5	V	
		BRTC signal	VBC	-0.3 to +5.5	V	
		PWSEL signal	VPSL	-0.3 to +5.5	V	
Storage temperature			Tst	-20 to +60	°C	-
Operating temperature		Front surface	TopF	0 to +55	°C	Note4
		Rear surface	TopR	0 to +55	°C	Note5
Relative humidity Note6			RH	≤ 95	%	Ta ≤ 40°C
				≤ 85	%	40 < Ta ≤ 50°C
				≤ 70	%	50 < Ta ≤ 55°C
Absolute humidity Note6			AH	≤ 73 Note7	g/m^3	Ta > 55°C

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Note1: Display signals are DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/- and CKD+/-.
Note2: Function signal 1 is MOD0, MOD1, BSEL0 and BSEL1.
Note3: Function signal 2 is CSR, CSL, SCLK and SDAT
Note4: Measured at center of LCD panel surface (including self-heat)
Note5: Measured at center of LCD module's rear shield surface (including self-heat)
Note6: No condensation
Note7: Ta = 55°C, RH = 70%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 Driving for LCD panel signal processing board

(Ta = 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDD	10.8	12.0	13.2	V	-
Power supply current		IDD	-	900 Note1	1800 Note2	mA	at VDD = 12.0V, Mode 0 is selected.
Differential input threshold voltage for Display signals	Low	VTL	-100	-	-	mV	at VCM= 1.2V Note3
	High	VTH	-	-	+100	mV	
Terminating resister		RT	-	100	-	Ω	-
Input voltage for Function signal 1	Low	VFL1	0	-	0.8	V	MOD0,MOD1, BSEL0,BSEL1 Note4
Input current for Function signal 1	Low	IFL1	-10	-	10	μA	
Input voltage for Function signal 2	Low	VFL2	0	-	0.8	V	CSR, CSL, SCLK, SDAT Note5
	High	VFH2	2.0	-	3.6	V	

2

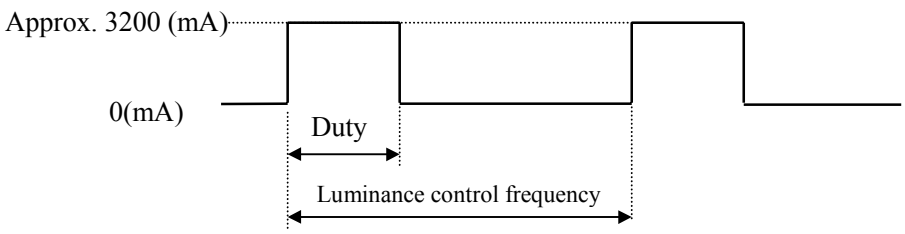
Note1: Checkered flag pattern [by EIAJ ED-2522]
Note2: 4H1V (170/255 grayscale)
Note3: Common mode voltage for LVDS receiver
Note4: High must be Open.
Note5: LVTTL level

4.3.2 Driving for backlight inverter

(Ta = 25°C)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage			VDDB	11.4	12.0	12.6	V	-
Power supply current			IDDB	-	3,200	4,000	mA	VDDB = 12.0V, at maximum luminance
Input voltage for signals	BRTI signal		VBI	0	-	1.0	V	-
	BRTP signal	Low	VBPL	0	-	0.8	V	
		High	VBPH	2.0	-	5.25	V	
	BRTC signal	Low	VBCL	0	-	0.8	V	
		High	VBCH	2.0	-	5.25	V	
	PWSEL signal	Low	VPSLL	0	-	0.8	V	
		High	VPSLH	2.0	-	5.25	V	
Input current for signals	BRTI signal		IBI	-130	-	-	μA	
	BRTP signal	Low	IBPL	-1.6	-	-	mA	
		High	IBPH	-	-	3.5	mA	
	BRTC signal	Low	IBCL	-610	-	-	μA	
		High	IBCH	-	-	440	μA	
	PWSEL signal	Low	IPSLL	-610	-	-	μA	
		High	IPSLH	-	-	440	μA	

4.3.3 Backlight inverter current wave 2



Maximum luminance control : 100%
Minimum luminance control : 20%
Luminance control frequency : 276Hz (typ.)

Note1: The power supply lines (VDDB and GNDB) occurs large ripple voltage (See "**4.3.4 Power supply voltage ripple**".) while luminance control. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on. Put a capacitor (5,000 to 6,000μF) between the power source lines (VDDB and GNDB) to reduce the noise, if the noise occurred in the circuit.

Note2: Luminance control frequency indicate the input pulse frequency, when select the external pulse control. See "**4.6.2 Detail of PWM timing**".

4.3.4 Power supply voltage ripple

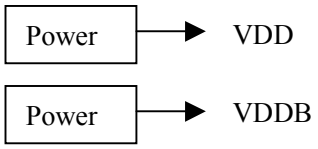
This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Parameter	Power supply voltage	Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VDD	12.0 V	≤ 100	mVp-p
VDDB	12.0 V	≤ 200	mVp-p

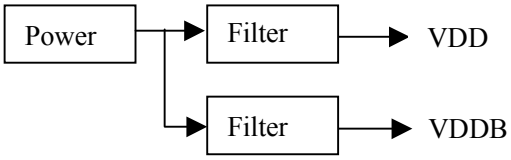
Note1: The permissible ripple voltage includes spike noise.

Example of the power supply connection

a) Separate the power supply



b) Put in the filter



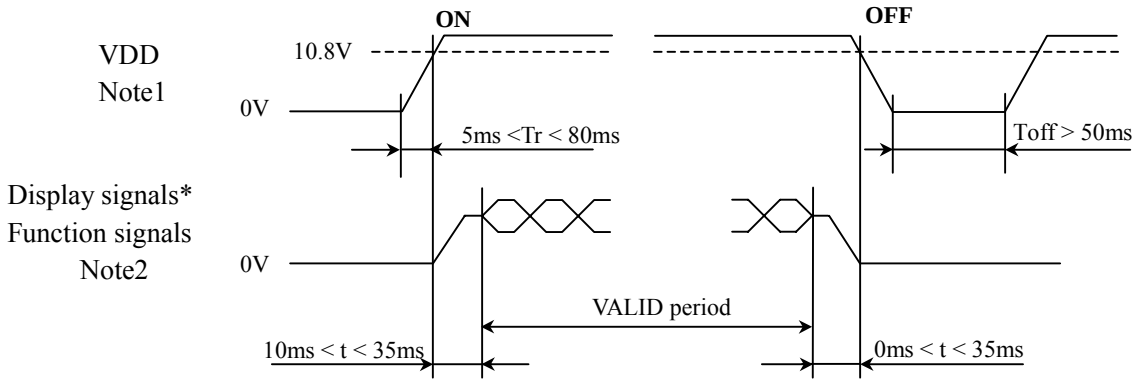
4.3.5 Fuses

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	FHC20 502AD	KAMAYA ELECTRIC Co., Ltd.	5A	12.5A	Note1
			24V		
VDDB	R451007	Littelfuse Inc.	7A	14A	
			63V		

Note1: The power supply capacity should be more than the fusing current. If the power supply capacity is less than the fusing current, the fuse may not blow for a short time, and then nasty smell, smoking and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 Sequence for LCD panel signal processing board



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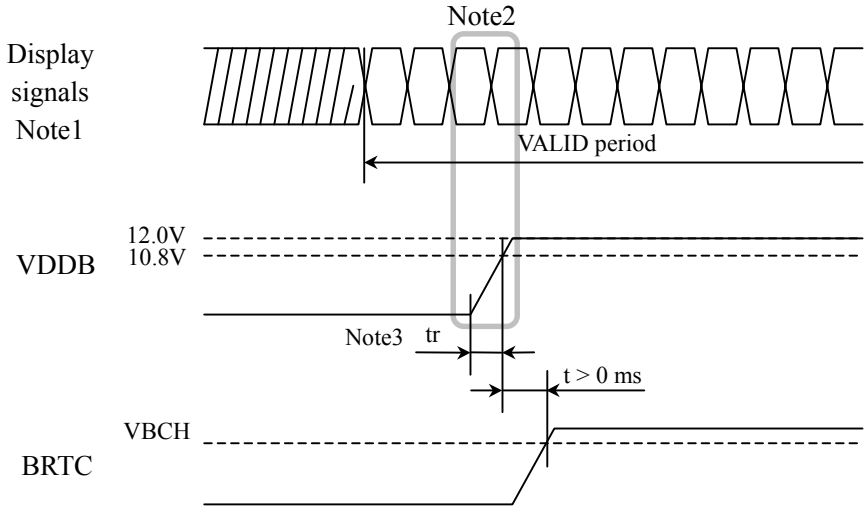
* These signals should be measured at the terminal of 100Ω resistor.

Note1: In terms of voltage variation (voltage drop) while VDD rising edge is below 10.8V, a protection circuit may work, and then this product may not work.

Note2: Display and function signals must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged.
If some of display and function signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. If customer stops the display and function signals, they should be cut VDD.
Display signals: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/- and CKD+/-
Function signals: MOD0, MOD1, BSEL0, BSEL1, CSR, CSL, SCLK and SDAT

4.4.2 Sequence for backlight inverter



Note1: These are the display signals for LCD panel signal processing board.

Note2: The backlight power supply voltage (VDDB) should be inputted within the valid period of display signals, in order to avoid unstable data display.

Note3: The tr should be less than 800ms when BRTC terminal [Socket: CN202, Pin No.: 4] (See "**4.5.2 Backlight inverter**".) is Open.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

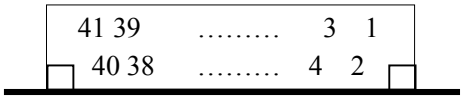
CN1 socket (LCD module side): FI-W41P-HF (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: FI-W41S (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	GND	Ground	-
2	CSR	Chip Select R	LUT control signal
3	CSL	Chip Select L	
4	SCLK	Serial Clock	
5	SDAT	Serial Data	
6	MOD0	Mode selection	LVDS transmission mode select
7	MOD1		
8	BSEL0	Bit mapping selection	LVDS bit mapping selection
9	BSEL1		
10	TEST	Test terminal	This terminal must be open.
11	GND	Ground	-
12	DB3+	Pixel data B3	LVDS differential signal Note1
13	DB3-		
14	GND	Ground	-
15	CKB+	Pixel clock B	LVDS differential signal Note1
16	CKB-		
17	GND	Ground	-
18	DB2+	Pixel data B2	LVDS differential signal Note1
19	DB2-		
20	GND	Ground	-

Pin No.	Symbol	Function	Description
21	DB1+	Pixel data B1	LVDS differential signal Note1
22	DB1-		
23	GND	Ground	-
24	DB0+	Pixel data B0	LVDS differential signal Note1
25	DB0-		
26	GND	Ground	-
27	DA3+	Pixel data A3	LVDS differential signal Note1
28	DA3-		
29	GND	Ground	-
30	CKA+	Pixel clock A	LVDS differential signal Note1
31	CKA-		
32	GND	Ground	-
33	DA2+	Pixel data A2	LVDS differential signal Note1
34	DA2-		
35	GND	Ground	-
36	DA1+	Pixel data A1	LVDS differential signal Note1
37	DA1-		
38	GND	Ground	-
39	DA0+	Pixel data A0	LVDS differential signal Note1
40	DA0-		
41	GND	Ground	-

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be connected between LCD panel signal processing board and LVDS transmitter.

CN1: Figure of socket



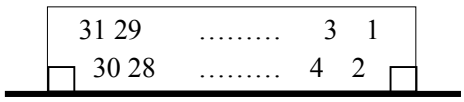
CN2 socket (LCD module side): FI-W31P-HF (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: FI-W31S (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	GND	Ground	-
2	DD3+	Pixel data D3	LVDS differential signal Note1
3	DD3-		
4	GND	Ground	-
5	CKD+	Pixel clock D	LVDS differential signal Note1
6	CKD-		
7	GND	Ground	-
8	DD2+	Pixel data D2	LVDS differential signal Note1
9	DD2-		
10	GND	Ground	-
11	DD1+	Pixel data D1	LVDS differential signal Note1
12	DD1-		
13	GND	Ground	-
14	DD0+	Pixel data D0	LVDS differential signal Note1
15	DD0-		

Pin No.	Symbol	Function	Description
16	GND	Ground	-
17	DC3+-	Pixel data C3	LVDS differential signal Note1
18	DC3-		
19	GND	Ground	-
20	CKC+	Pixel clock C	LVDS differential signal Note1
21	CKC-		
22	GND	Ground	-
23	DC2+	Pixel data C2	LVDS differential signal Note1
24	DC2-		
25	GND	Ground	-
26	DC1+	Pixel data C1	LVDS differential signal Note1
27	DC1-		
28	GND	Ground	-
29	DC0+	Pixel data C0	L LVDS differential signal Note1
30	DC0-		
31	GND	Ground	-

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be connected between LCD panel signal processing board and LVDS transmitter.

CN2: Figure of socket



CN3 socket (LCD module side): IL-Z-8PL-SMTY (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: IL-Z-8S-S125C (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	VDD	Power supply	-
2	VDD		
3	VDD		
4	VDD		
5	GND	Ground	-
6	GND		
7	GND		
8	GND		

4.5.2 Backlight inverter

CN201 socket (LCD module side): DF3-8P-2H (HIROSE ELECTRIC Co,.Ltd.)
Adaptable plug: DF3-8S-2C (HIROSE ELECTRIC Co,.Ltd.)

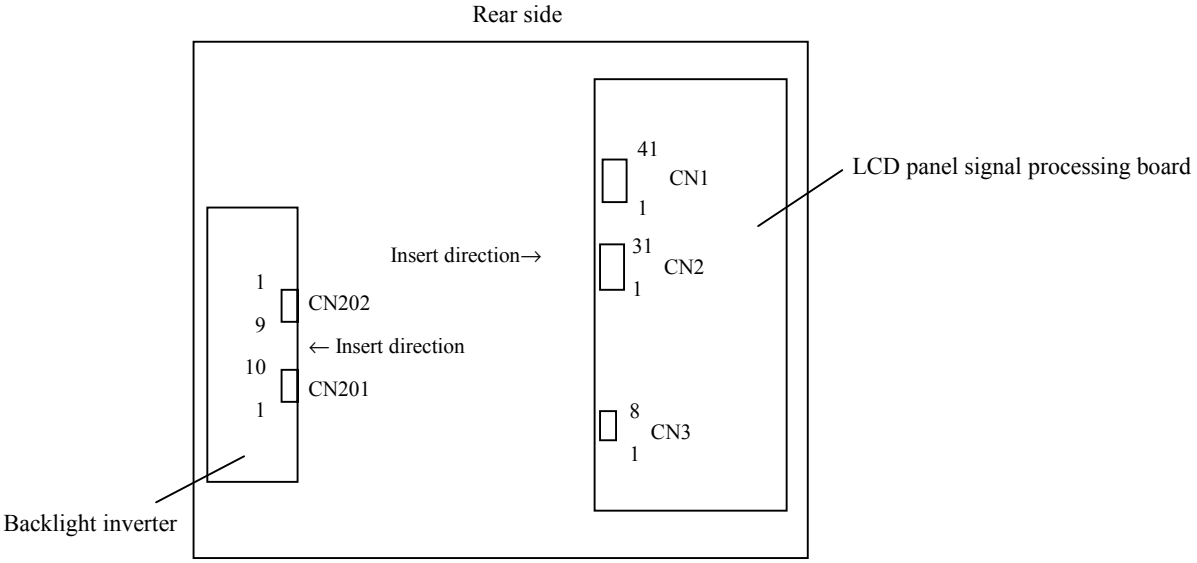
Pin No.	Symbol	Function	Description
1	GNDB	Backlight ground	-
2	GNDB		
3	GNDB		
4	GNDB		
5	VDDB	Power supply	-
6	VDDB		
7	VDDB		
8	VDDB		

CN202 socket (LCD module side): IL-Z-9PL1-SMTY (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: IL-Z-9S-S125C3 (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	GNDB	Backlight ground	-
2	GNDB		
3	N.C.	-	Keep the terminal open.
4	BRTC	Backlight ON/OFF control signal	High or Open: Backlight ON Low: Backlight OFF
5	BRTH	Luminance control signal	Note1
6	BRTI	Luminance control by resistor method or voltage method	
7	BRTP	PWM signal	
8	GNDB	Backlight ground	-
9	PWSEL	Selection of luminance control signal method	Note1, Note2

Note1: See "**4.6.1 Luminance control methods**".
Note2: PWSEL must not be High when VDDB is 0V or BRTC is Low.

4.5.3 Positions of socket

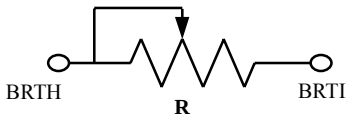


4.6 LUMINANCE CONTROLS

4.6.1 Luminance control methods

<table>
<tr><th>Method</th><th>Adjustment and luminance ratio</th><th>PWSEL signal</th><th>BRTP signal</th></tr>
<tr><td>Variable resistor control

Note1</td><td>• Adjustment

The variable resistor (R) for luminance control should be 10kΩ ±5%, B curve, 1/10W. Minimum point of the resistor is the minimum luminance. Also maximum point of the resistor is the maximum luminance.
 

• Luminance ratio Note3
<table><tr><th>Resistance</th><th>Luminance ratio</th></tr><tr><td>0 Ω</td><td>30% (Minimum)</td></tr><tr><td>10 kΩ</td><td>100% (Maximum)</td></tr></table></td><td rowspan="2">High or Open</td><td rowspan="2">Open</td></tr>
<tr><td>Voltage control

Note1</td><td>• Adjustment

Voltage control method works, when BRTH terminal is 0V and VBI voltage is input between BRTI and BRTH terminal. This control method can carry out continuation adjustment of luminance.

• Luminance ratio Note3
<table><tr><th>BRTI Voltage (VBI)</th><th>Luminance ratio</th></tr><tr><td>0V</td><td>30% (Minimum)</td></tr><tr><td>1.0V</td><td>100% (Maximum)</td></tr></table></td></tr>
<tr><td>Pulse width modulation
Note1
Note2</td><td>• Adjustment

Pulse width modulation (PWM) method works, when PWSEL signal is Low and PWM signal (BRTP signal) is inputted into BRTP terminal. The luminance is controlled by duty ratio of BRTP signal.

• Luminance ratio Note3
<table><tr><th>Duty ratio Note4</th><th>Luminance ratio</th></tr><tr><td>0.2</td><td>30% (Minimum)</td></tr><tr><td>1.0</td><td>100% (Maximum)</td></tr></table></td><td>Low</td><td>PWM signal</td></tr>
</table>

Note1: In case of the resistor control method and the voltage control method, noises may appear on the display image depending on the input signals timing for LCD panel signal processing board.

Use PWM method, if interference noises appear on the display image!

Note2: In case BRTC signal is High or Open, the inverter will stop work when BRTP signal is fixed to Low. In this case, backlight will not turn on, even if BRTP signal is inputted again. This is not out of order. Backlight inverter will start to work when power is supplied again.

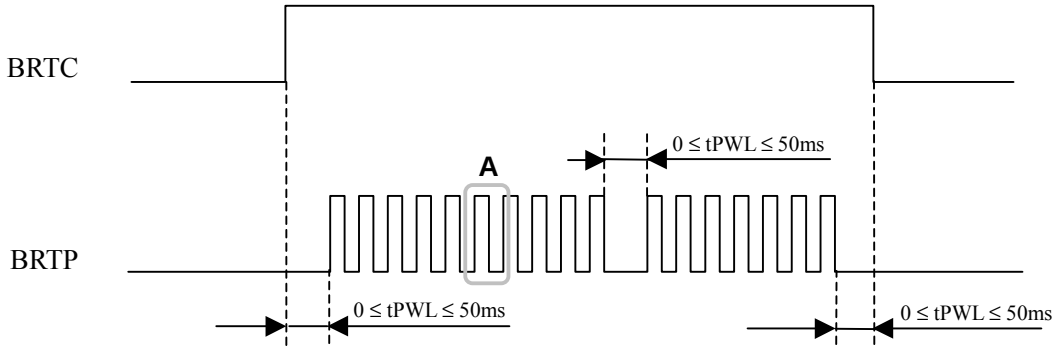
Note3: These data are the target values.

Note4: See "**4.6.2 Detail of PWM timing**".

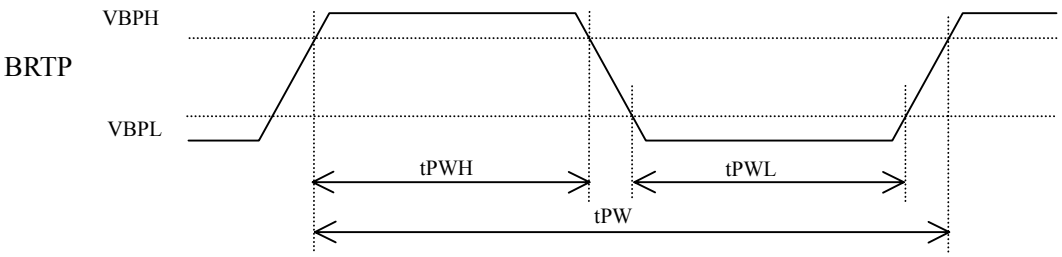
4.6.2 Detail of PWM timing

(1) Timing diagrams

• Outline chart



• Detail of **A** part



(2) Each parameter

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Luminance control frequency	FL	185	-	325	Hz	Note1, Note2
Duty ratio	DL	0.2	-	1.0	-	Note1, Note3
Non signal period	tPWL	0	-	50	ms	Note4

Note1: Definition of parameters is as follows.

$$FL = \frac{1}{tPW} \quad DL = \frac{tPWH}{tPW}$$

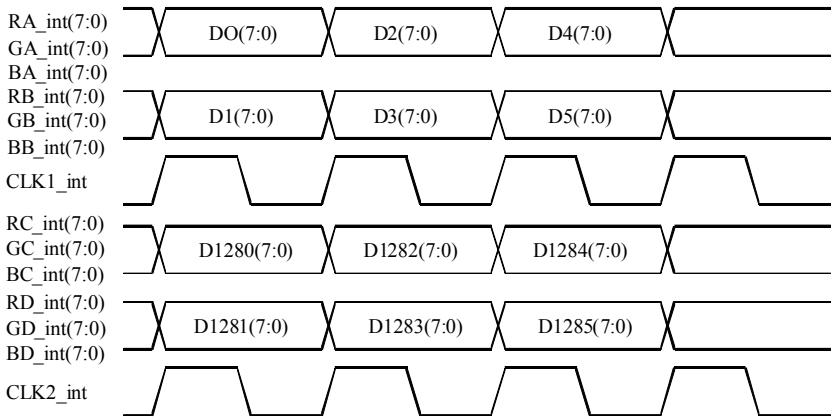
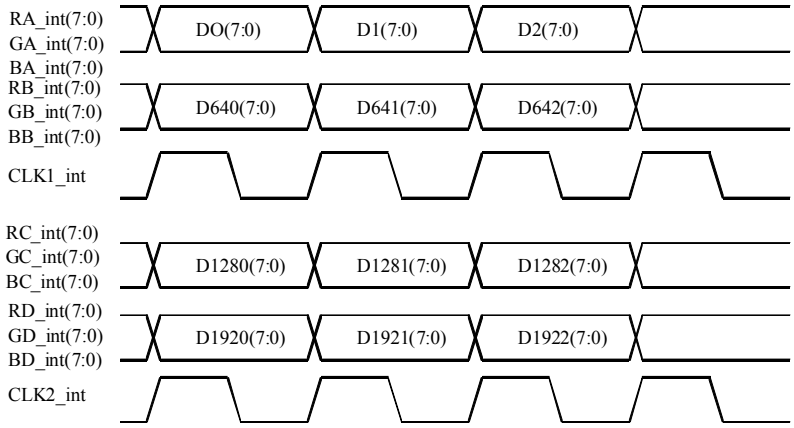
Note2: See the following formula for luminance control frequency.
Luminance control frequency = tv × (n+0.25) [or (n + 0.75)]
n = 1, 2, 3 · · · · · ·
tv: See "**4.13.1 Input signal specifications**".

The interference noise of luminance control frequency and input signal frequency for LCD panel signal processing board may appear on a display. Set up luminance control frequency so that the interference noise does not appear!

Note3: See "**4.6.1 Luminance control methods**".
Note4: If tPWN is more than 50ms, the backlight will be turned off by a protection circuit for inverter.

4.7 LVDS DATA TRANSMISSION MODE

Transmission mode of LVDS data is selectable with MOD0 and MOD1 terminal.

MOD[1:0] Note1		Mode name	data transmission chart
1	0		
H	H	Mode 0 L/R transmission mode	
H	L	Mode 1 4 divided transmission mode	
L	H	Reserved	-
L	L	Reserved	-

Note1: High must be Open.

4.8. METHOD OF CONNECTION FOR LVDS TRANSMITTER

LVDS data bit mapping mode is selectable with BSEL0 and BSEL1 terminal.

	Bit mapping			Transmitter Pin Assignment					CN1	
	BSEL[1:0] Note1			Single type LVDS Tx	Dual type LVDS TX		Output Connector		Pin No.	Signal name
	[H:H] [L:L]	[H:L]	[L:H]		THine THC63LVD823	NS DS90C387				
Pixel data A	R2	R7	R0	TA0	R12	R10	ATA- ATA+			
	R3	R6	R1	TA1	R13	R11				
	R4	R5	R2	TA2	R14	R12		→	40	DA0-
	R5	R4	R3	TA3	R15	R13		→	39	DA0+
	R6	R3	R4	TA4	R16	R14				
	R7	R2	R5	TA5	R17	R15				
	G2	G7	G0	TA6	G12	G10				
	G3	G6	G1	TB0	G13	G11	ATB- ATB+			
	G4	G5	G2	TB1	G14	G12				
	G5	G4	G3	TB2	G15	G13		→	37	DA1-
	G6	G3	G4	TB3	G16	G14		→	36	DA1+
	G7	G2	G5	TB4	G17	G15				
	B2	B7	B0	TB5	B12	B10				
	B3	B6	B1	TB6	B13	B11				
	B4	B5	B2	TC0	B14	B12	ATC- ATC+			
	B5	B4	B3	TC1	B15	B13				
	B6	B3	B4	TC2	B16	B14		→	34	DA2-
	B7	B2	B5	TC3	B17	B15		→	33	DA2+
	Hsync	Hsync	Hsync	TC4	HSYNC	HSYNC				
	Vsync	Vsync	Vsync	TC5	VSYNC	VSYNC				
	DE	DE	DE	TC6	DE	DE				
	R0	R1	R6	TD0	R10	R16	ATD- ATD+			
	R1	R0	R7	TD1	R11	R17				
	G0	G1	G6	TD2	G10	G16		→	28	DA3-
	G1	G0	G7	TD3	G11	G17		→	27	DA3+
	B0	B1	B6	TD4	B10	B16				
	B1	B0	B7	TD5	B11	B17				
	N.C.	N.C.	N.C.	TD6	-	-				
	CLK	CLK	CLK	CLK	CLK	CLK	ATCLK- ATCLK+	→	31	CKA-
								→	30	CKA+
Pixel data B	R2	R7	R0	TA0	R22	R20	BTA- BTA+			
	R3	R6	R1	TA1	R23	R21				
	R4	R5	R2	TA2	R24	R22		→	25	DB0-
	R5	R4	R3	TA3	R25	R23		→	24	DB0+
	R6	R3	R4	TA4	R26	R24				
	R7	R2	R5	TA5	R27	R25				
	G2	G7	G0	TA6	G22	G20				
	G3	G6	G1	TB0	G23	G21	BTB- BTB+			
	G4	G5	G2	TB1	G24	G22				
	G5	G4	G3	TB2	G25	G23		→	22	DB1-
	G6	G3	G4	TB3	G26	G24		→	21	DB1+
	G7	G2	G5	TB4	G27	G25				
	B2	B7	B0	TB5	B22	B20				
	B3	B6	B1	TB6	B23	B21				
	B4	B5	B2	TC0	B24	B22	BTC- BTC+			
	B5	B4	B3	TC1	B25	B23				
	B6	B3	B4	TC2	B26	B24		→	19	DB2-
	B7	B2	B5	TC3	B27	B25		→	18	DB2+
	Hsync	Hsync	Hsync	TC4	HSYNC	HSYNC				
	Vsync	Vsync	Vsync	TC5	VSYNC	VSYNC				
	DE	DE	DE	TC6	DE	DE				
	R0	R1	R6	TD0	R20	R26	BTD- BTD+			
	R1	R0	R7	TD1	R21	R27				
	G0	G1	G6	TD2	G20	G26		→	13	DB3-
	G1	G0	G7	TD3	G21	G27		→	12	DB3+
	B0	B1	B6	TD4	B20	B26				
	B1	B0	B7	TD5	B21	B27				
	N.C.	N.C.	N.C.	TD6	-	-				
	CLK	CLK	CLK	CLK	CLK	CLK	BTCLK- BTCLK+	→	16	CKB-
								→	15	CKB+

Note1: High must be Open.

	BSEL[1:0] Note1			Single type LVDS Tx	Dual type LVDS TX		Output Connector		CN2	
	[H:H] [L:L]	[H:L]	[L:H]		THine THC63LVD823	NS DS90C387			Pin No.	Signal name
Pixel data C	R2	R7	R0	TA0	R12	R10	CTA- CTA+			
	R3	R6	R1	TA1	R13	R11				
	R4	R5	R2	TA2	R14	R12		→	30	DC0-
	R5	R4	R3	TA3	R15	R13		→	29	DC0+
	R6	R3	R4	TA4	R16	R14				
	R7	R2	R5	TA5	R17	R15				
	G2	G7	G0	TA6	G12	G10				
	G3	G6	G1	TB0	G13	G11	CTB- CTB+			
	G4	G5	G2	TB1	G14	G12				
	G5	G4	G3	TB2	G15	G13		→	27	DC1-
	G6	G3	G4	TB3	G16	G14		→	26	DC1+
	G7	G2	G5	TB4	G17	G15				
	B2	B7	B0	TB5	B12	B10				
	B3	B6	B1	TB6	B13	B11				
	B4	B5	B2	TC0	B14	B12	CTC- CTC+			
	B5	B4	B3	TC1	B15	B13				
	B6	B3	B4	TC2	B16	B14		→	24	DC2-
	B7	B2	B5	TC3	B17	B15		→	23	DC2+
	Hsync	Hsync	Hsync	TC4	HSYNC	HSYNC				
	Vsync	Vsync	Vsync	TC5	VSYNC	VSYNC				
	DE	DE	DE	TC6	DE	DE				
	R0	R1	R6	TD0	R10	R16	CTD- CTD+			
	R1	R0	R7	TD1	R11	R17				
	G0	G1	G6	TD2	G10	G16		→	18	DC3-
	G1	G0	G7	TD3	G11	G17		→	17	DC3+
	B0	B1	B6	TD4	B10	B16				
	B1	B0	B7	TD5	B11	B17				
	N.C.	N.C.	N.C.	TD6	-	-				
	CLK	CLK	CLK	CLK	CLK	CLK	CTCLK- CTCLK+	→	21	CKC-
								→	20	CKC+
Pixel data D	R2	R7	R0	TA0	R22	R20	DTA- DTA+			
	R3	R6	R1	TA1	R23	R21				
	R4	R5	R2	TA2	R24	R22		→	15	DD0-
	R5	R4	R3	TA3	R25	R23		→	14	DD0+
	R6	R3	R4	TA4	R26	R24				
	R7	R2	R5	TA5	R27	R25				
	G2	G7	G0	TA6	G22	G20				
	G3	G6	G1	TB0	G23	G21	DTB- DTB+			
	G4	G5	G2	TB1	G24	G22				
	G5	G4	G3	TB2	G25	G23		→	12	DD1-
	G6	G3	G4	TB3	G26	G24		→	11	DD1+
	G7	G2	G5	TB4	G27	G25				
	B2	B7	B0	TB5	B22	B20				
	B3	B6	B1	TB6	B23	B21				
	B4	B5	B2	TC0	B24	B22	DTC- DTC+			
	B5	B4	B3	TC1	B25	B23				
	B6	B3	B4	TC2	B26	B24		→	9	DD2-
	B7	B2	B5	TC3	B27	B25		→	8	DD2+
	Hsync	Hsync	Hsync	TC4	HSYNC	HSYNC				
	Vsync	Vsync	Vsync	TC5	VSYNC	VSYNC				
	DE	DE	DE	TC6	DE	DE				
	R0	R1	R6	TD0	R20	R26	DTD- DTD+			
	R1	R0	R7	TD1	R21	R27				
	G0	G1	G6	TD2	G20	G26		→	3	DD3-
	G1	G0	G7	TD3	G21	G27		→	2	DD3+
	B0	B1	B6	TD4	B20	B26				
	B1	B0	B7	TD5	B21	B27				
	N.C.	N.C.	N.C.	TD6	-	-				
	CLK	CLK	CLK	CLK	CLK	CLK	DTCLK- DTCLK+	→	6	CKD-
								→	5	CKD+

Note1: High must be Open.

4.9 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display in equivalent to 16,777,216 colors in 256 scale. Also the relation between display colors and input data signals is as the following table.

Display colors		Data signal (0: Low level, 1: High level)																							
		RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
		RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	BC7	BC6	BC5	BC4	BC3	BC2	BB1	BB0
		RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	GD7	GD6	GD5	GD4	GD3	GD2	GD1	GD0	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑	:								:								:							
	↓	:								:								:							
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑	:								:								:							
	↓	:								:								:							
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑	:								:								:							
	↓	:								:								:							
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

4.10 10-BIT LOOK UP TABLE FOR GAMMA ADJUSTMENT

Adjustment of gamma characteristics by using built-in 10-bit LUT (look up table) is possible. Gamma characteristics of each RGB color can be adjusted by using Command (See following tables.). 2

Table1: Serial data Composition

DATA	DATA name	Function	Remarks
D31	CMD5	Control Command	See table2.
D30	CMD4	Control Command	
D29	CMD3	Control Command	
D28	CMD2	Control Command	
D27	CMD1	Control Command	
D26	CMD0	Control Command	
D25	ADD9	LUT Address (MSB)	See table3.
D24	ADD8	LUT Address	
D23	ADD7	LUT Address	
D22	ADD6	LUT Address	
D21	ADD5	LUT Address	
D20	ADD4	LUT Address	
D19	ADD3	LUT Address	
D18	ADD2	LUT Address	
D17	ADD1	LUT Address	
D16	ADD0	LUT Address (LSB)	
D15	Dummy	Dummy Data "0"	See table4.
D14	Dummy	Dummy Data "0"	
D13	Dummy	Dummy Data "0"	
D12	Dummy	Dummy Data "0"	
D11	Dummy	Dummy Data "0"	
D10	Dummy	Dummy Data "0"	
D9	DATA9	LUT Data (MSB)	
D8	DATA8	LUT Data	
D7	DATA7	LUT Data	
D6	DATA6	LUT Data	
D5	DATA5	LUT Data	
D4	DATA4	LUT Data	
D3	DATA3	LUT Data	
D2	DATA2	LUT Data	
D1	DATA1	LUT Data	
D0	DATA0	LUT Data (LSB)	

Table2: Command table (CMD5 to CMD0 : 6bit)

DATA name	Parameter	Remarks
CMD5	Must be set "1" for normal operation.	-
CMD4	Must be set "1" for normal operation.	-
CMD3	"1": Word write "0": Sequential write	-
CMD2	Must be set "1" for normal operation.	-
CMD1	"1": Single sub pixel data write "0": Three sub pixel data write	"1": Use ADD9, ADD8 "0": Not use ADD9, ADD8
CMD0	Must be set "0" for normal operation.	-

Table3: Address table (ADD9 to ADD0 : 10bit)

DATA name	Parameter	Remarks
ADD9	Sub pixel Select ADD9:8= 0:0 Red 0:1 Green 1:0 Blue 1:1 Command	-
ADD8		
ADD7	LUT Address (=Input Data) 256 address 00h – FFh	If ADD9:8 = 1:1, must be set ADD7:0 = 00h.
ADD6		
ADD5		
ADD4		
ADD3		
ADD2		
ADD1		
ADD0		

Table4: Data table (DATA15 to DATA0 : 16bit)

DATA	DATA name	Parameter	Remarks
D15	Dummy	Dummy Data Must be set “0”	-
D14	Dummy		
D13	Dummy		
D12	Dummy		
D11	Dummy		
D10	Dummy		
D9	DATA9	10bit LUT Data 000h – 3FFh	Set ADD9:0=300h DATA9:0=000h : Disable LUT (default) DATA9:0=001h : Enable LUT
D8	DATA8		
D7	DATA7		
D6	DATA6		
D5	DATA5		
D4	DATA4		
D3	DATA3		
D2	DATA2		
D1	DATA1		
D0	DATA0		

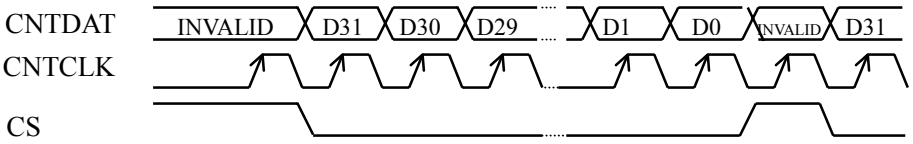
Note1: When writing the LUT control signal, a noise may appear on the display. In order to prevent the noise appearing on the display, following measures should be performed. 2

(1) The LUT data should be rewritten during invalid period of pixel data (See "**4.13 INPUT SIGNAL TIMINGS FOR LCD PANEL SIGNAL PROCESSING BOARD**".).

(2) The LUT data should be rewritten when the LUT data is invalid state.
(Table3: DATA9:0= 000h: Disable LUT)

4.11 LUT SERIAL COMMUNICATION TIMINGS

Write timing

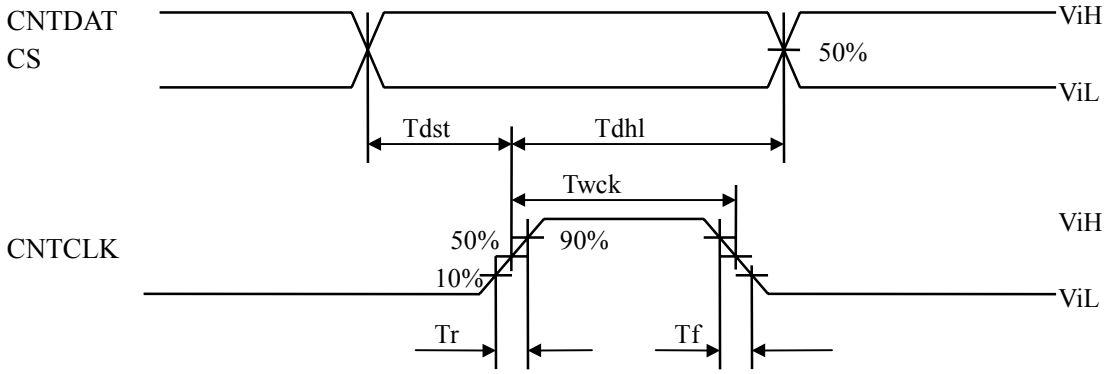


Word write mode

Sequential write mode

Parameter	Symbol	min.	max.	Unit	Remarks
CLK pulse width	Twck	50	-	ns	CNTCLK
CLK frequency	Fclk	-	5	MHz	
DATA,CS set up time	Tdst	50	-	ns	CNTDAT,CS
DATA,CS hold time	Tdhl	50	-	ns	

SERIAL COMMUNICATION WAVEFORM



4.12 DISPLAY POSITIONS

The following table is the coordinates per pixel.

C(0, 0)	C(1, 0)	•••	C(X, 0)	•••	C(2558, 0)	C(2559, 0)
C(0, 1)	C(1, 1)	•••	C(X, 1)	•••	C(2558, 1)	C(2559, 1)
⋮	⋮	⋮	⋮	⋮	⋮	⋮
C(0, Y)	C(1, Y)	•••	C(X, Y)	•••	C(2558, Y)	C(2559, Y)
⋮	⋮	⋮	⋮	⋮	⋮	⋮
C(0, 2046)	C(1, 2046)	•••	C(X, 2046)	•••	C(2558, 2046)	C(2559, 2046)
C(0, 2047)	C(1, 2047)	•••	C(X, 2047)	•••	C(2558, 2047)	C(2559, 2047)

4.13 INPUT SIGNAL TIMINGS FOR LCD PANEL SIGNAL PROCESSING BOARD

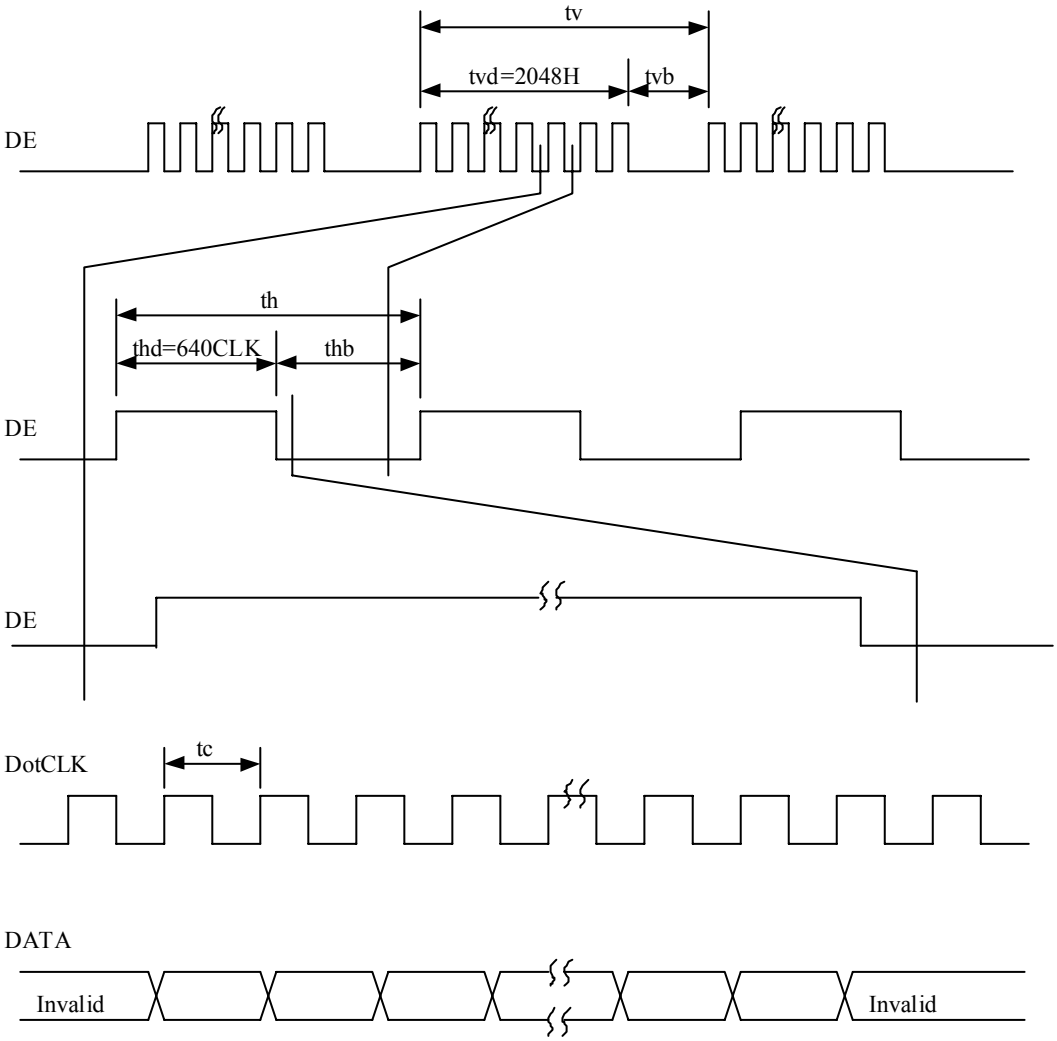
4.13.1 Input signal specifications 2

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency	1/ tc	80.0 -	83.26 12.01	85.0 -	MHz ns	-
	Duty	tcl / tc	Note1			-	-
	Rise, fall	tcrf				ns	-
Hsync	Period	th	7.72 660	8.071 672	- 690	µs CLK	typ.= 123.9kHz Note3
	Display period	thd	640			CLK	-
	Blank	thb	20	32	50	CLK	-
Vsync	Period	tv	- 2053	16.667 2064	- -	ms H	typ.= 60.0Hz
	Display period	tvd	2048			H	-
	Blank	tvb	5	16	-	H	-
DE	CLK-DE set-up	tdes	Note1			ns	-
	CLK-DE hold	tdeh				ns	-
	Raise, fall	tderf				ns	-
DATA	CLK-DATA set-up	tds	Note1			ns	-
	CLK-DATA hold	tdh				ns	-
	Rise, fall	tdrf				ns	-

Note1: Timing specifications are defined by the input signals of LVDS transmitter.
Note2: Both of “time” and “CLK number” of the “th” must keep the Minimum value of specification.
Note3: "th" (CLK number) should be fixed to "16n+k" (n= natural number: 1,2,3···, k=0, 2, 4 or 6). 2
In case "th" is not the specified value, it may cause display deterioration.
e.g.: "th" (CLK number)
At Vsync frequency= 60.0Hz typ.: 660, 662, 672, 674, 676, 678, 688, 690
At Vsync frequency= 50.0Hz typ.: 672, 674, 676, 678, 688, 690, 692, 694

4.13.2 Input signal timing chart

2



4.14 OPTICS

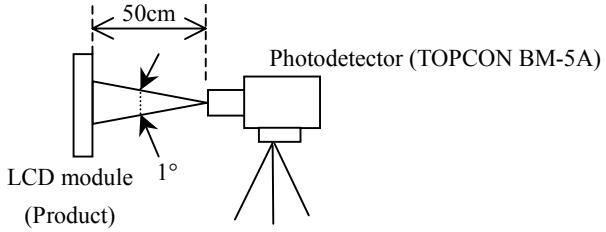
4.14.1 Optical characteristics

Parameter Note1		Condition	Symbol	min.	typ.	max.	Unit	Remarks
Luminance		White at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	L	TBD	220	-	cd/m^2	-
Contrast ratio		White/Black at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	CR	TBD	450	-	-	Note2
Luminance uniformity		-	LU	-	1.1	1.3	-	Note3
Chromaticity	White	**x** coordinate	Wx	-	0.313	-	-	Note4
		y coordinate	Wy	-	0.329	-	-	
	Red	**x** coordinate	Rx	-	TBD	-	-	
		y coordinate	Ry	-	TBD	-	-	
	Green	**x** coordinate	Gx	-	TBD	-	-	
		y coordinate	Gy	-	TBD	-	-	
	Blue	**x** coordinate	Bx	-	TBD	-	-	
		y coordinate	By	-	TBD	-	-	
Color gamut		θR = 0°, θL = 0°, θU = 0°, θD = 0° at center, against NTSC color space	C	60	72	-	%	
Response time		Black to White	Ton	-	TBD	TBD	ms	Note5 Note6
		White to Black	Toff	-	TBD	TBD	ms	
Viewing angle	Right	θU = 0°, θD = 0°, CR = 10	θR	70	85	-	°	Note7
	Left	θU = 0°, θD = 0°, CR = 10	θL	70	85	-	°	
	Up	θR = 0°, θL = 0°, CR = 10	θU	70	85	-	°	
	Down	θR = 0°, θL = 0°, CR = 10	θD	70	85	-	°	

2

Note1: Measurement conditions are as follows.
Ta = 25°C, VDD = 12V, VDDB=12V, Display mode: QSXGA, Horizontal cycle = 123.9kHz, Vertical cycle = 60.0Hz

Optical characteristics are measured at luminance saturation after 20minutes from working the product, in the dark room. Also measurement method for luminance is as follows.



Note2: See "**4.14.2 Definition of contrast ratio**".
Note3: See "**4.14.3 Definition of luminance uniformity**".
Note4: These coordinates are found on CIE 1931 chromaticity diagram.
Note5: Product surface temperature: TopF = TBD°C
Note6: See "**4.14.4 Definition of response times**".
Note7: See "**4.14.5 Definition of viewing angles**".

4.14.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

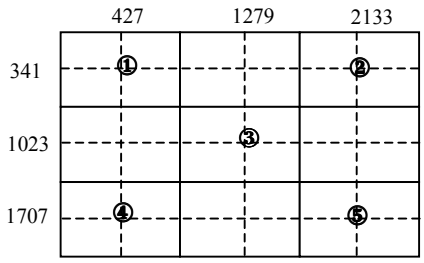
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.14.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

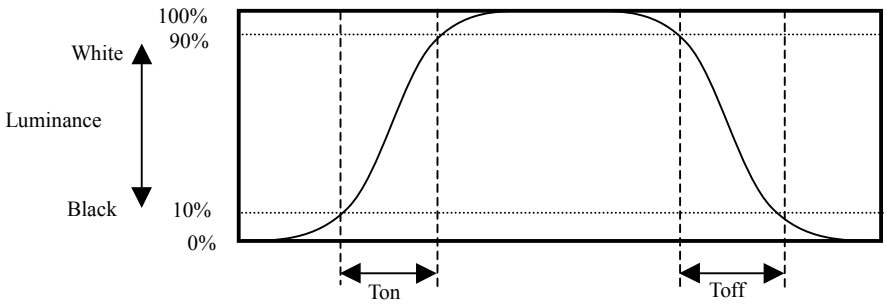
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

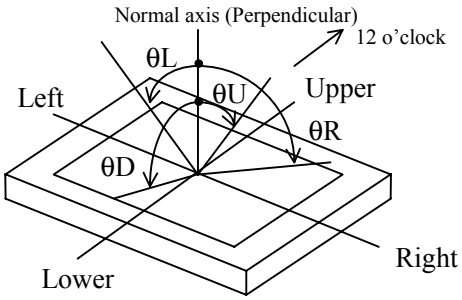


4.14.4 Definition of response times

Response time is measured, the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



4.14.5 Definition of viewing angles



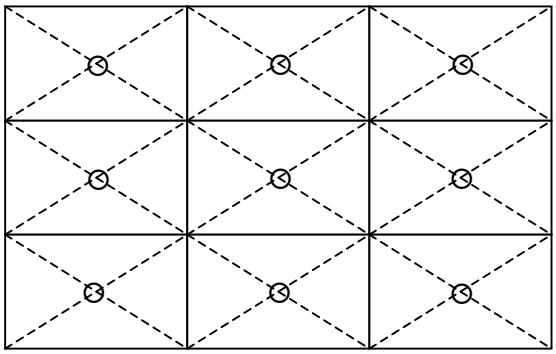
5. RELIABILITY TESTS

2

Test item		Condition	Judgment Note1
High temperature and humidity (Operation)		① 60 ± 2°C, RH = 60%, 240hours ② Display data is white.	No display malfunctions
Heat cycle (Operation)		① 0 ± 3°C…1hour 55 ± 3°C…1hour ② 50cycles, 4hours/cycle ③ Display data is white.	
Thermal shock (Non operation)		① -20 ± 3°C…30minutes 60 ± 3°C…30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s^2 ② 1 minute/cycle ③ X, Y, Z direction ④ 10 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)		① 294m/ s^2, 11ms ② X, Y, Z direction ③ 3 times each directions	
ESD (Operation)		① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	No display malfunctions
Dust (Operation)		① Sample dust: No.15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	
Low pressure	operation	① 53.3 kPa ② 0°C±3°C…24 hours ③ +55°C±3°C…24 hours	
	non-operation	① 15 kPa ② -20°C±3°C…24 hours ③+60°C±3°C…24 hours	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect specification. 2

Note2: See the following figure for discharge points



6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding this contents!**

⚠	This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.
⚡	This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.
✋	This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS

⚡

∗ Do not touch HIGH VOLTAGE PART of the inverter while turn on. Customer will be in danger of an electric shock.

✋

∗ Do not touch the working backlight and IC. Customer will be in danger of burn injury.
∗ Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s^2 and to be not greater 11ms, Pressure: To be not greater 19.6N)

6.3 ATTENTIONS ⚠

6.3.1 Handling of the product

① Take hold of both ends without touch the circuit board cover when customer pulls out products (LCD modules) from inner packing box. If customer touches it, products may be broken down or out of adjustment, because of stress to mounting parts.
② Do not hook cables nor pull connection cables such as lamp cable and so on, for fear of damage.
③ If customer puts down the product temporarily, the product puts on flat subsoil as a display side turns down.
④ Take the measures of electrostatic discharge such as earth band, ionic shower and so on, when customer deals with the product, because products may be damaged by electrostatic.
⑤ The torque for mounting screws must never exceed 0.294N·m. Higher torque values might result in distortion of the bezel.
⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area) except mounting hole portion.
Bends or twist described above and undue stress to any portion except mounting hole portion may cause display un-uniformity.
⑦ Do not press or rub on the sensitive display surface. If customer clean on the panel surface, NEC Corporation recommends using the cloth with ethanolic liquid such as screen cleaner for LCD.
⑧ Do not push-pull the interface connectors while the product is working, because wrong power sequence may break down the product.

⑨ Do not bend or unbend the lamp cable at the near part of the lamp holding rubber, to avoid the damage for high voltage side of the lamp. This damage may cause a lamp breaking and abnormal operation of high voltage circuit.

6.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in antistatic pouch in room temperature, because of avoidance for dusts and sunlight, if customer stores the product.
② In order to prevent dew condensation occurring by temperature difference, the product packing box must be opened after leave under the environment of an unpacking room temperature enough. Because a situation of dew condensation occurring is changed by the environmental temperature and humidity, evaluate the leaving time sufficiently. (Recommendation leaving time: 6 hour or more with packing state)
③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
④ This product is not designed as radiation hardened.
⑤ Use an original protection sheet on the product surface (polarizer). Adhesive type protection sheet should be avoided, because it may change color or properties of the polarizer.

6.3.3 Characteristics

The following items are neither defects nor failures.

① Response time, luminance and color may be changed by ambient temperature.
② The LCD may be seemed luminance non-uniformity, flicker, vertical seam or small spot by display patterns.
③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
⑤ The display color may be changed by viewing angle because of the use of condenser sheet in the backlight.
⑥ Optical characteristics may be changed by input signal timings.
⑦ The interference noise of input signal frequency for this product's signal processing board and luminance control frequency of customer's backlight inverter may appear on a display. Set up luminance control frequency of backlight inverter so that the interference noise does not appear.
⑧ The product may be changed of luminance by voltage variation, even if power source applies recommended voltage to backlight inverter.

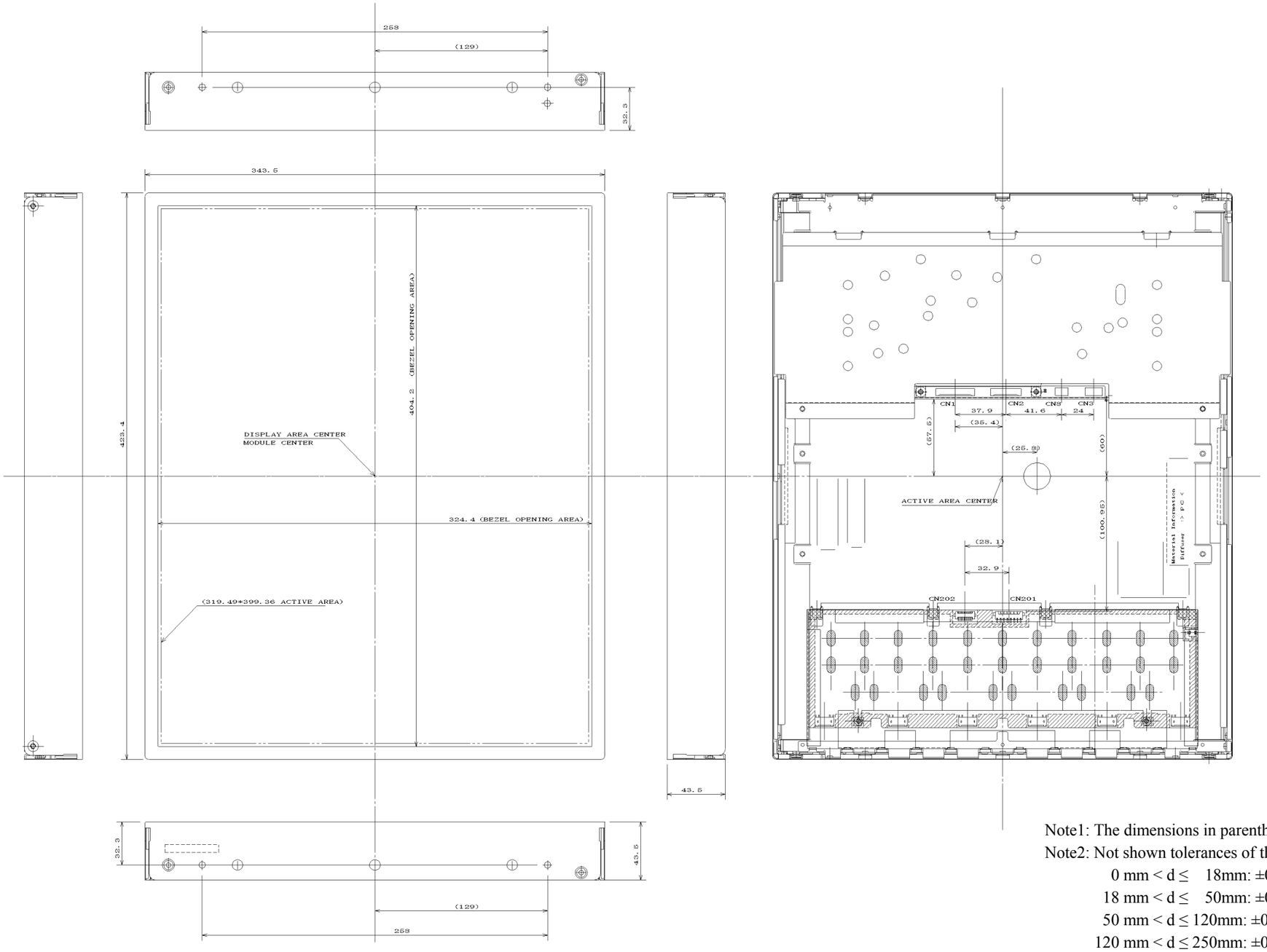
6.3.4 Other

① All GND, GNDB, VDD and VDDB terminals must be used without a non-connected line.
② Do not disassemble a product or adjust volume without permission of NEC Corporation.
③ See "REPLACEMENT MANUAL FOR BACKLIGHT UNIT", if customer would like to replace backlight.
④ Pay attention not to insert waste materials inside of products, if customer uses screwnails.
⑤ Pack the product with original shipping package, because of avoidance of some damages during transportation, when customer returns it to NEC Corporation for repair and so on.
⑥ Not only the module but also the equipment that used the module should be packed and transported as the module becomes vertical. Otherwise, there is the fear that a display dignity decreases by an impact or vibrations."

2

7. OUTLINE DRAWINGS

(Unit: mm)



Note1: The dimensions in parenthesis are for reference.

Note2: Not shown tolerances of the dimensions

0 mm < d ≤ 18mm: ±0.2mm.

18 mm < d ≤ 50mm: ±0.3mm.

50 mm < d ≤ 120mm: ±0.4mm.

120 mm < d ≤ 250mm: ±0.5mm.

250 mm < d : ±0.6mm.

(d: dimension)

REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Prepared date	Revision contents and signature
1st edition	Feb. 03, 2003	**Revision contents** New issue **Signature of writer** *Approved by* T. ITO *Checked by* —— *Prepared by* R. KAWASHIMA
2nd edition	June 11, 2003	**Revision contents** P1 Type name is decided. NL256204AC15-02 P4 Features are revised. P5, P7 • Weight: → 2440 (typ.), 2600 (max.) P5, P28 • Response time: → TBD P5 • Inverter: → 201PW121 P7 Operating temperature - Rear surface: → 0 to +55 °C P8 Power supply current: → 1800 mA max. P9 Backlight inverter current wave is added. P11 Sequence for LCD panel signal processing board - Tr: → 5ms <Tr < 80ms P22 10-bit look up table for gamma adjustment: Explanation is added. P23 Note1 is added. P26 Input signal specifications • Expression of table is revised. • Note3 is changed. P27 Input signal timing chart is revised. Detail of input signals timing chart is deleted. P30 Reliability tests • Expression of table is revised. • Note1 is revised. P32 Precautions • Environment: ④ is added. P33 Outline drawings are revised. **Signature of writer** *Approved by* T. ITO *Checked by* —— *Prepared by* R. KAWASHIMA