NEC

TFT MONOCHROME LCD MODULE

NL256204AM15-01

51cm (20.1 Type)
QSXGA

PRELIMINARY DATA SHEET

(1st edition)

All information is subject to change without notice.
Please confirm the delivery specification before starting to design your system.

INTRODUCTION

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The quality grade of this product is ***"Standard"*** unless otherwise specified in this document. If customers intend to use this product for applications other than those specified for ***"Standard"*** quality grade, they should contact NEC Corporation sales representative in advance.

Anti-radioactive design is not implemented in this product.

CONTENTS

1. OUTLINE

NL256204AM15-01 is a TFT (thin film transistor) active matrix monochrome liquid crystal display (LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight with an inverter.

This product has a 51cm (20.1 inches) display area by a diagonal, and contains 2560×2048 pixels in it. Also it can display 256 gray scale per one sub-pixel.

2. FEATURES

- Ultra-wide viewing angle (with lateral electric field) (Super Advanced SFT Panel)
- High resolution
- Low reflection
- LVDS interface
- High luminance
- Small fool print
- Incorporated direct type backlight (twelve lamps in backlight unit with an inverter)
- Replaceable backlight unit (part No. : TBD)
- Replaceable inverter (part No. : TBD)

3. APPLICATION

- EWS monitors
- Monitors for CAD system
- Monitors for medical system

4. PRINCIPLE AND STRUCTURE

A monochrome TFT (thin film transistor) LCD module is composed of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. The TFT liquid crystal panel structure is injected liquid crystal material into the narrow gap between a TFT array glass substrate. Also, LCD module is connected the driver LSIs with a TFT liquid crystal panel structure, and then the backlight assembly is attached to the backside of the panel.

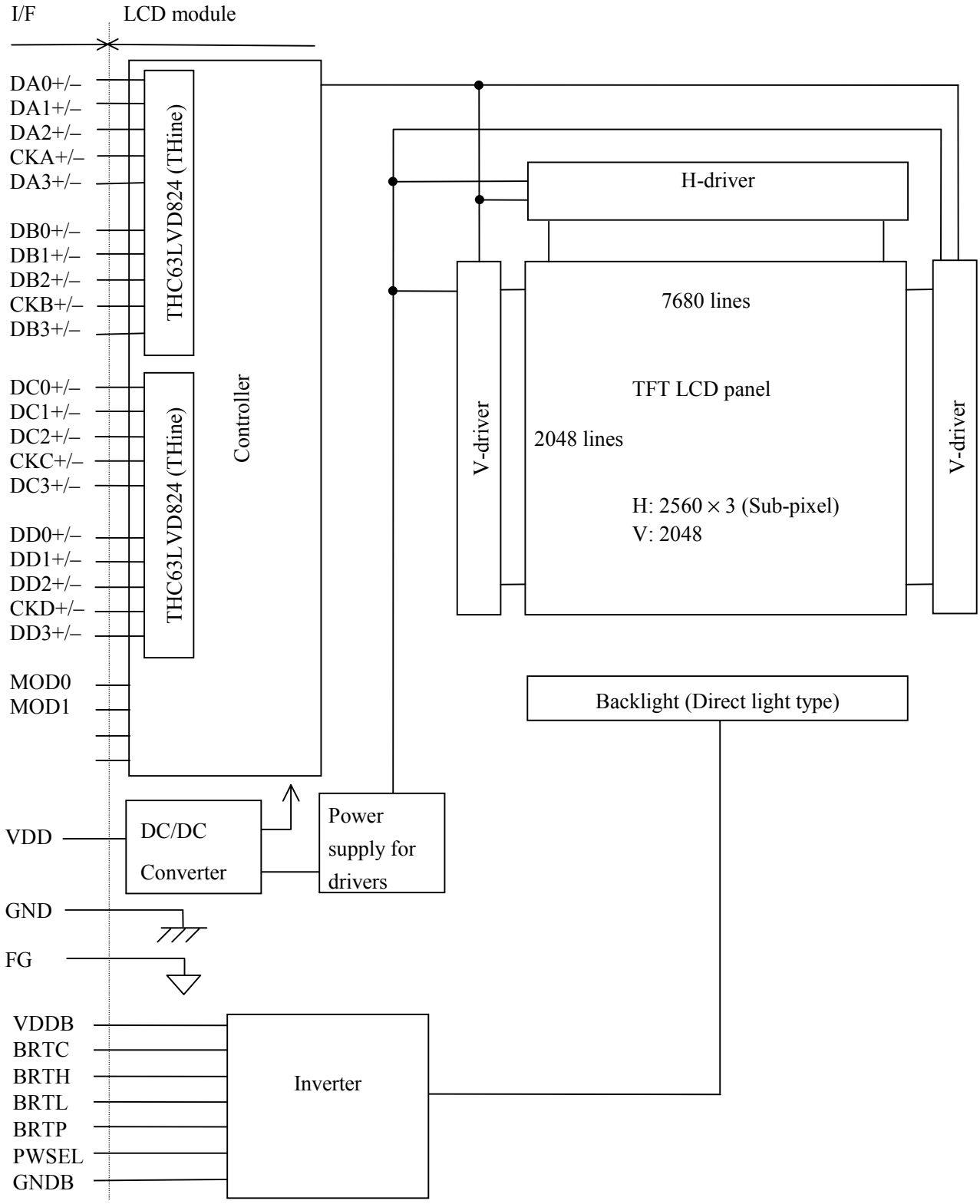
Gray scale data signals from a source system are modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.

Working as an electro-optical switch, each TFT cell regulates transmitted light from the backlight assembly when worked by the data source.

5. OUTLINE OF CHARACTERISTICS (at room temperature)

Display area	399.36 (H) × 319.49 (V) mm
Drive system	a-Si TFT active matrix
Display gray scale	256
Number of pixels	2560 (H) × 2048 (V)
Pixel arrangement	Sub-pixel Vertical stripe
Pixel pitch	0.156 (H) × 0.156 (V) mm
Module size (Include an i-guard sensor)	423.4 (H, Typ.) × 346.5 (V, Typ.) × 43.5 (D, Typ.) mm
Weight	2600 g (Typ.)
Contrast ratio	600:1(Typ.)
Viewing angle (more than the contrast ratio of 10:1)	- Horizontal: 85° (Typ., left side, right side) - Vertical: 85° (Typ., up side, down side)
Designed viewing direction	- Optimum grayscale (γ=DICOM): perpendicular
Polarizer Pencil-hardness	3 H (Min., at JIS K5400)
Response time	30 ms (Typ.), (Ton + Toff)
Luminance	850 cd/m^2 (Typ.)
Polarizer type	(Antiglare)
Signal system	4 ports LVDS interface (THC63LV824×2pcs, THine Electronics, Inc.) RGB 8-bit signals, Data enable signal (DE) THC63LVD823 (THine Electronics, Inc.) are preferable.
Supply voltage	12V (Logic, LCD driving), 12V (Backlight)
Backlight	Direct light type: twelve cold cathode fluorescent lamps with an inverter [Replaceable parts] - Backlight unit: TBD - Inverter: TBD
Power consumption	75.6 W (Typ.) (at maximum luminance)

6. BLOCK DIAGRAM



Note1: GND is signal ground for logic and LCD driving. GND is not connected to FG (Frame Ground) and GNDB (Backlight ground) in the LCD module. These grounds should be connected in customer equipment.

7. GENERAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	423.4 (H) × 346.5 (V) × 43.5 (D) (Include an i-guard sensor)	mm
Display area	399.36 (H) × 319.488 (V) [Diagonal display size: 51cm (Type 20.1)]	mm
Number of pixels	2560 (H) × 2048 (V)	pixel
Dot pitch	0.052 (H) × 0.156 (V)	mm
Pixel pitch	0.156 (H) × 0.156 (V)	mm
Pixel arrangement	3 sub-pixel vertical stripe	-
Display gray scale	256 (per one sub-pixel)	gray scale
Weight	2600 (Typ.)	g

8. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remarks
Supply voltage	VDD	-0.3 to +15.0	V	Ta = 25°C
	VDDB	-0.3 to +15.0	V	
LVDS input voltage (LCD)	Vi	-0.3 to 3.6	V	Ta = 25°C, VDD=12V
Control logic input voltage (MOD0,MOD1,MOD2)	ViC	-0.3 to +3.9	V	
Backlight logic input voltage (BRTC,BRTP,PWSEL)	ViB1,2	-0.3 to +5.5	V	Ta = 25°C VDDB=12V
BRTL input voltage (BRTL)	ViB3	-0.3 to +1.5	V	
Storage temperature	Tst	-20 to +60	°C	-
Operating temperature	TopF	0 to +55	°C	Module surface Note1
	TopR	0 to +55	°C	Module rear surface Note2
Relative humidity Note3	RH	≤ 95	%	Ta≤40°C
		≤ 85	%	40°C<Ta≤50°C
		≤ 70	%	50°C<Ta≤55°C
Absolute humidity Note3	AH	≤ 73 Note4	g/m^3	Ta>55°C

Note1: Measured at the LCD panel surface center (including self-heat)

Note2: Measured at center of the rear shield (including self-heat)

Note3: No condensation

Note4: Ta = 55°C, RH = 70%

9. ELECTRICAL CHARACTERISTICS

(1) Controller / LCD driving

(Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	VDD	10.8	12.0	13.2	V	-
Ripple voltage	VRP	-	-	100	mV	for VDD
Differential input "L" Threshold voltage	ViTL	-100	-	-	mV	at VCM=1.2V VCM: Common mode voltage for LVDS driver
Differential input "H" Threshold voltage	ViTH	-	-	+100	mV	
Input voltage width	Vi	0	-	2.4	V	-
Terminating resistor	RT	-	100	-	Ω	-
Logic input "L" level	ViCL	0	-	0.8	V	MOD0,MOD1,MOD2
Logic input "L" current	IiCL	-10	-	-10	μA	
Supply current	IDD	-	(2300) Note1	2700 Note2	mA	at VDD=12.0V, MODE1 is selected.

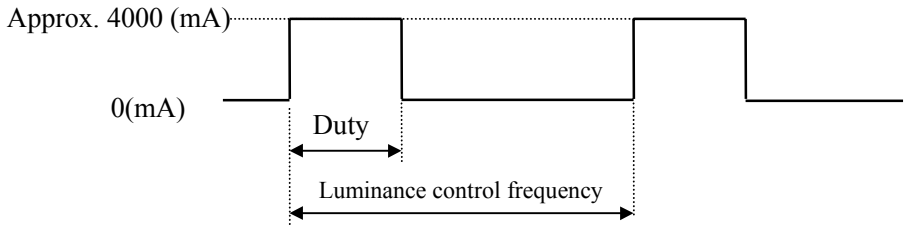
Note1: Checkered flag pattern (by EIAJ ED-2522)
Note2: Pattern for maximum current

(2) Backlight

(Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	VDDB	-	12.0	-	V	backlight power supply
Logic input “L” level	ViBL1	0	-	0.8	V	for BRTP
Logic input “H” level	ViBH1	2	-	5.25	V	
Logic input “L” level	ViBL2	0	-	0.8	V	for BRTC, PWSEL
Logic input “H” level	ViBH2	2	-	5.25	V	
Logic input “L” current	IiBL1	-1.6	-	-	mA	for BRTP
Logic input “H” current	IiBH1	-	-	3.5	mA	
Logic input “L” current	IiBL2	-610	-	-	μA	for BRTC, PWSEL
Logic input “H” current	IiBH2	-	-	440	μA	
Supply current	IDDB	-	4000	4800	mA	VDDB=12.0V at Max. luminance

(3) Inverter current wave



Maximum luminance control : 100%
Minimum luminance control : 20%
Luminance control frequency : 285Hz (Typ.)

Note1: The power supply lines (VDDB and GNDB) have large ripple voltage while dimming. There is the possibility that the ripple voltage produces an acoustic noise and signal wave noise in a system circuit (e.g. audio circuit). If the noise occurred in a circuit system, put an aluminum electrolytic capacitor (5,000 to 6,000μF) between the power source lines (VDDB and GNDB), and the capacitor will be able to reduce the noise.

Note2: Luminance control frequency indicate the input pulse frequency, when select the external pulse control. See '11.INTERFACE PIN CONECTIONS AND FUNCTIONS, (4) External pulse control for luminance'.

(4) Fuses

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	(CCF1NTE8)	KOA Corporation	(8A) (60V)	TBD A	Note1
VDDB	(R451007)	Littelfuse Inc.	(7A) (63V)	TBD A	

Note1: The power supply capacity should be more than the fusing current. If the power supply capacity is less than the fusing current, the fuse may not blow for a short time, and then nasty smell, smoking and so on may occur.

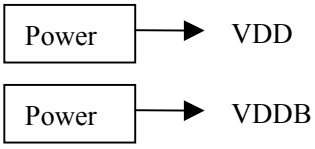
(5) Ripple of supply supply voltage

Supply voltage	VDD (for logic and LCD driver)	VDDB (for backlight)
Acceptable level Note1	≤ 100mVp-p	≤ 200mVp-p

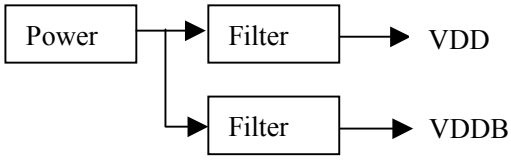
Note1: The acceptable level of ripple voltage includes spike noise.

Example of the power supply connection

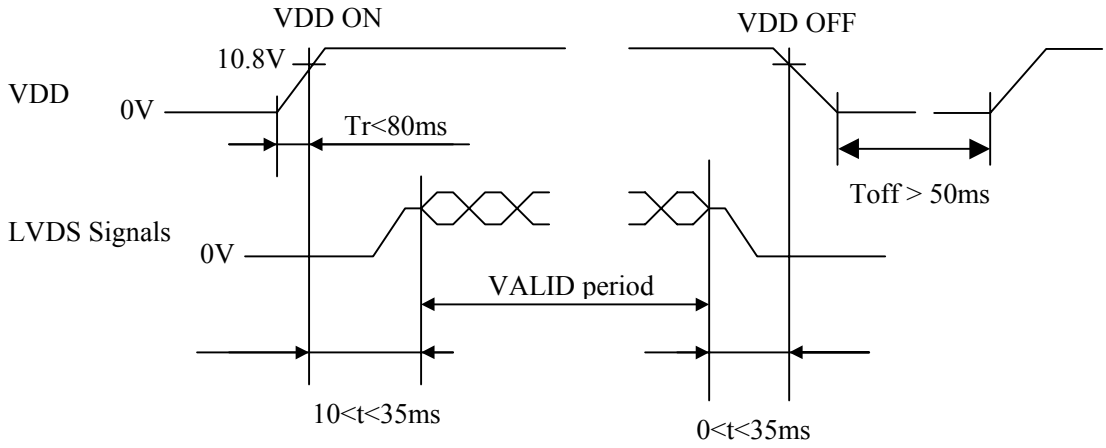
a) Separate the power supply

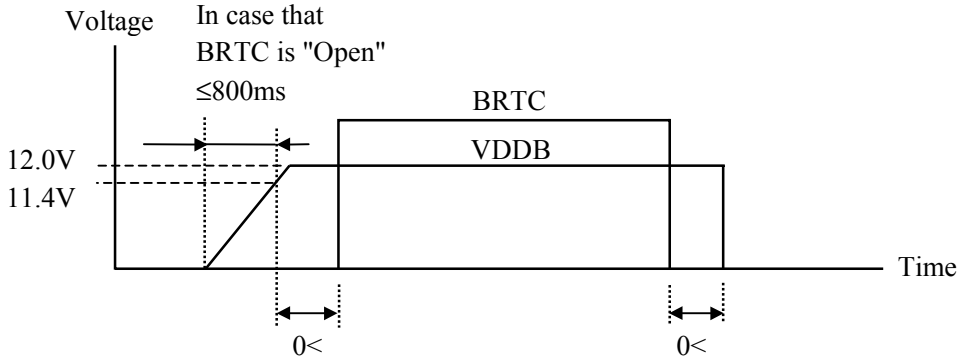


b) Put in the filter



10. POWER SUPPLY VOLTAGE SEQUENCE





Note1: LVDS signals should be measured at the terminal of 100Ω resistor.

Note2: In terms of voltage variation (voltage drop) while VDD rising edge is below 10.8V, a protection circuit may work, and then this product may not work.

Note3: The backlight power supply voltage should be inputted within the valid period of LVDS signals, in order to avoid unstable data display.

Note4: Rising time of backlihght power supply (12V) should be less the 800ms, otherwise, the protection circuit will work, and backlight will be turned off.

Note5: When "L" period of BRTP is more than 50 ms, the backlight will be turned off by safety circuit.

Note6: PWSEL must not be "H" while VDDB is 0V or BRTC is "L".

11. INTERFACE PIN CONNECTIONS AND FUNCTIONS

(1) Interface connector for signal and power

CN1 socket: FI-W41P-HF
Adaptable plug: FI-W41S
Supplier: Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Function	Description
1	GND	ground	signal ground
2	CSR	Chip Select R	LUT control signal
3	CSL	Chip Select L	
4	SCLK	Serial Clock	
5	SDAT	Serial Data	
6	MOD0	mode select	LVDS transmission mode select
7	MOD1		
8	BSEL0	bit mapping select	LVDS bit mapping select
9	BSEL1		
10	TEST	test terminal	keep connect Open
11	GND	ground	signal ground
12	DB3+	pixel data B3	LVDS differential signal
13	DB3-		
14	GND	ground	signal ground
15	CKB+	pixel clock B	LVDS differential signal
16	CKB-		
17	GND	ground	signal ground
18	DB2+	pixel data B2	LVDS differential signal
19	DB2-		
20	GND	ground	signal ground

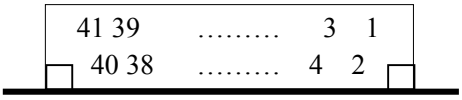
Pin No.	Symbol	Function	Description
21	DB1+	pixel data B1	LVDS differential signal
22	DB1-		
23	GND	ground	signal ground
24	DB0+	pixel data B0	LVDS differential signal
25	DB0-		
26	GND	ground	signal ground
27	DA3+	pixel data A3	LVDS differential signal
28	DA3-		
29	GND	ground	signal ground
30	CKA+	pixel clock A	LVDS differential signal
31	CKA-		
32	GND	ground	signal ground
33	DA2+	pixel data A2	LVDS differential signal
34	DA2-		
35	GND	ground	signal ground
36	DA1+	pixel data A1	LVDS differential signal
37	DA1-		
38	GND	ground	signal ground
39	DA0+	pixel data A0	LVDS differential signal
40	DA0-		
41	GND	ground	signal ground

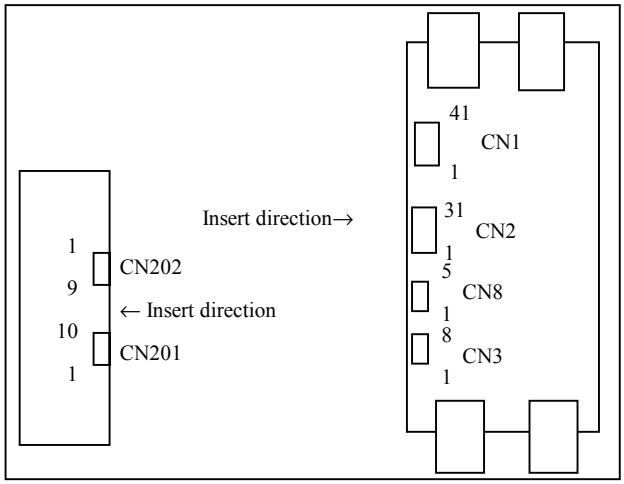
Note1: GND is signal ground for Controller. GND is not connected to FG (Frame Ground) and GNDB (Backlight ground) in the LCD module. These grounds should be connected to system ground in customer equipment.

Note2: Use 100Ω twist pair wires for the cable.

Note3: All GND terminals should be used.

CN1: Figure of socket





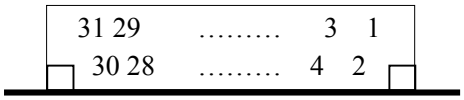
CN2 socket: FI-W31P-HF
Adaptable plug: FI-W31S
Supplier: Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Function	Description
1	GND	ground	signal ground
2	DD3+	pixel data D3	LVDS differential signal
3	DD3-		
4	GND	ground	signal ground
5	CKD+	pixel clock D	LVDS differential signal
6	CKD-		
7	GND	ground	signal ground
8	DD2+	pixel data D2	LVDS differential signal
9	DD2-		
10	GND	Ground	signal ground
11	DD1+	pixel data D1	LVDS differential signal
12	DD1-		
13	GND	Ground	signal ground
14	DD0+	pixel data D0	LVDS differential signal
15	DD0-		

Pin No.	Symbol	Function	Description
16	GND	Ground	signal ground
17	DC3+-	pixel data C3	LVDS differential signal
18	DC3-		
19	GND	Ground	signal ground
20	CKC+	pixel clock C	LVDS differential signal
21	CKC-		
22	GND	Ground	signal ground
23	DC2+	pixel data C2	LVDS differential signal
24	DC2-		
25	GND	Ground	signal ground
26	DC1+	pixel data C1	LVDS differential signal
27	DC1-		
28	GND	Ground	signal ground
29	DC0+	pixel data C0	LVDS differential signal
30	DC0-		
31	GND	Ground	signal ground

Note1: GND is signal ground for Controller. GND is not connected to FG (Frame Ground) and GNDB (Backlight ground) in the LCD module. These grounds should be connected to system ground in customer equipment.
Note2: Use 100Ω twist pair wires for the cable.
Note3: All GND terminals should be used.

CN2: Figure of socket

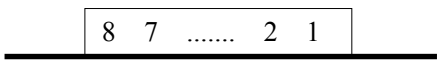


CN3 socket: IL-Z-8PL-SMTY
Adaptable plug: IL-Z-8S-S125C
Supplier: Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Function	Description
1	VDD	12V power supply	+12V±10%
2	VDD		
3	VDD		
4	VDD		
5	GND	ground	signal ground
6	GND		
7	GND		
8	GND		

Note1: GND is signal ground for Controller. GND is not connected to FG (Frame Ground) and GNDB (Backlight ground) in the LCD module. These grounds should be connected to system ground in customer equipment.
Note2: All GND and VDD terminals should be used.

CN3: Figure of socket

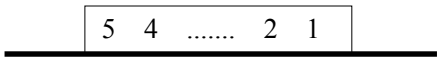


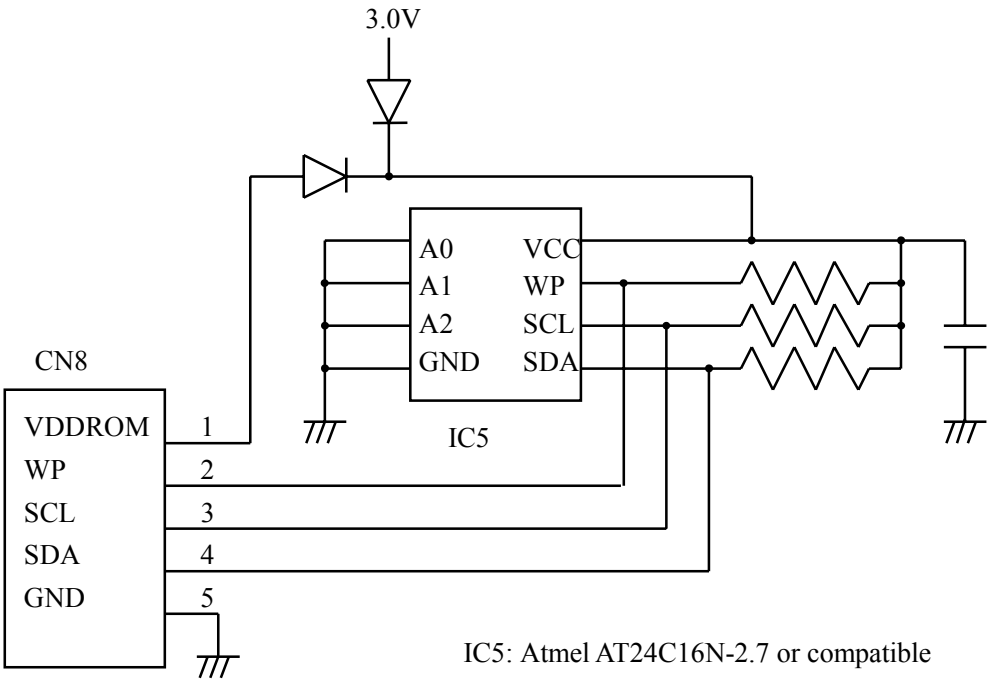
CN8 socket: IL-Z-5PL-SMTY
Adaptable plug: IL-Z-5S-S125C
Supplier: Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Function	Description
1	VDDROM	Power supply for E2PROM	+2.7 to +5.0V
2	WP	Write protect	Write protect for E2PROM "Open" Write protect "L" Write enable
3	SCL	Serial clock	I2C Serial clock
4	SDA	Serial data	I2C Serial Data
5	GND	ground	Signal ground

Note1: GND is signal ground for Controller. GND is not connected to FG (Frame Ground) and GNDB (Backlight ground) in the LCD module. These grounds should be connected to system ground in customer equipment.

CN8: Figure of socket





IC5: Atmel AT24C16N-2.7 or compatible

Block Diaglam

(2) Connector for backlight unit

CN201 socket: DF3-8P-2H
Adaptable plug: DF3-8S-2C
Supplier: HIROSE ELECTRIC Co,.Ltd.

Pin No.	Symbol	Function	Description
1	GNDB	Ground for backlight	Note1
2	GNDB		
3	GNDB		
4	GNDB		
5	VDDB	12V power supply	+12V
6	VDDB		
7	VDDB		
8	VDDB		

Note1: GNDB should be connected to system ground in customer equipment.
Note2: All GNDB and VDDB terminals should be used

CN201: Figure of socket

1 2 ..... 7 8

CN202 socket: IL-Z-9PL1-SMTY
Adaptable plug: IL-Z-9S-S125C3
Supplier: Japan Aviation Electronics Industry Limited (JAE)

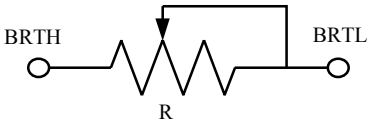
Pin No.	Symbol	Function	Description
1	GNDB	Ground for backlight	Note1
2	GNDB		
3	N.C.	Non-connection	Keep the terminal open
4	BRTC	Backlight ON/OFF control signal	"H" or "Open": Backlight on "L": Backlight off
5	BRTH	Luminance control signal	-
6	BRTL	Luminance control signal	
7	BRTP	Luminance control signal	-
8	GNDB	Ground for backlight	Note1
9	PWSEL	Luminance control select signal	-

Note1: All GNDB terminals should be used.

CN202: Figure of socket

9 8 ……. 2 1

(3) Luminance control

Control method	Function and adjustment	PWSEL	BRTP signal
PWM	Luminance controlled by BRTP signal. See "(4) External pulse control for luminance".	"L"	Input
Variable resistor Note1	The variable resistor for luminance control should be 10kΩ type, and zero point of the resistor corresponds to the minimum of luminance.  Max. luminance (100%): R=10kΩ Min. luminance (30%): R=0Ω Mating variable resistor: 10kΩ ±5%,B curve, 1/10W	"H" or "OPEN"	"OPEN"
Voltage Note1	BRTH should be fixed to 0V, and input to BRTL as follows. Max. Luminance (100%): 1V(Typ.) Min. Luminance (30%): 0V		

Note1: Luminance control may be overlap noises on the display image depending on input signal timing. In this case, keep off the interference between input signal and backlight driving signal, by PWM method.

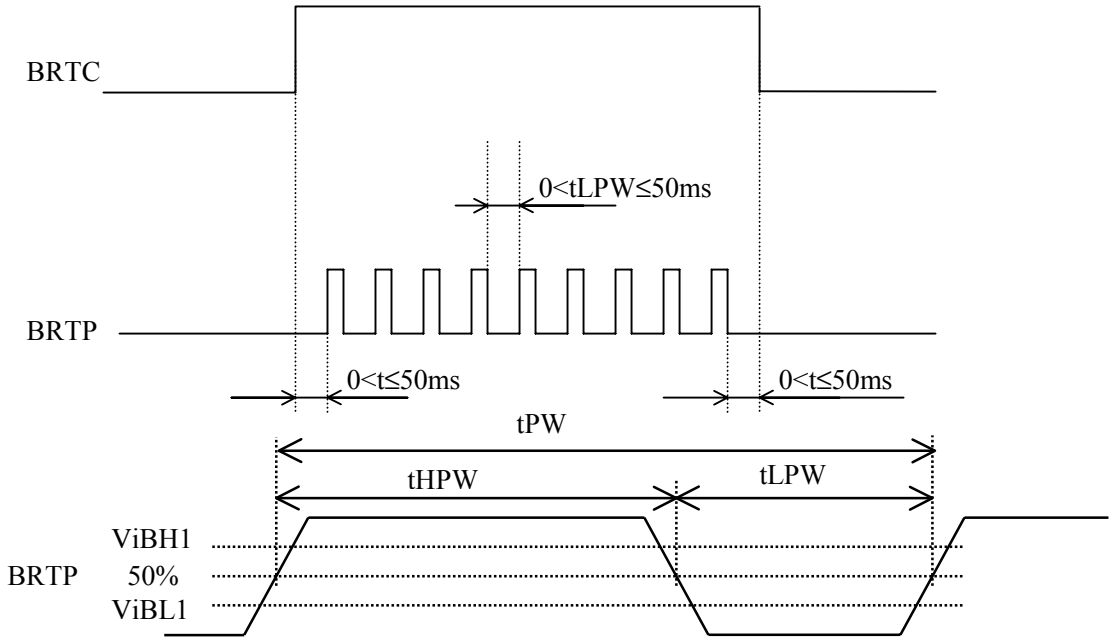
(4) External pulse control for luminance

Luminance control with external pulse is valid, when PWSWL is "L" and external pulse signal is inputted to BRTP. This luminance control is controlled by duty ratio, and luminance is as follows.

Duty ratio=100%: Max. luminance

Duty ratio=20%: Min. luminance

In case of BRTC = High or Open, the inverter will stop work when BRTP terminal is fixed to Low in the condition of PWSEL = Low. In this case, backlight will not turn on, even if external pulse signal is put to BRTP again. This is no damage. Inverter will start to work when power is supplied again.



Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Frequency	1/tPW	185	-	325	Hz	Note1
"L" period	tLPW	-	-	50	ms	Note2
Pulse-width	tHPW/tPW	20	-	100	%	Note3
Luminance ratio	-	-	30 to 100	-	%	-
Input voltage	ViBL1	0	-	0.8	V	-
	ViBH1	2.0	-	5.25	V	-

Note1: See the following formula for luminance control frequency.

Luminance control frequency = Vsync frequency × (n+0.25) [or (n + 0.75)]

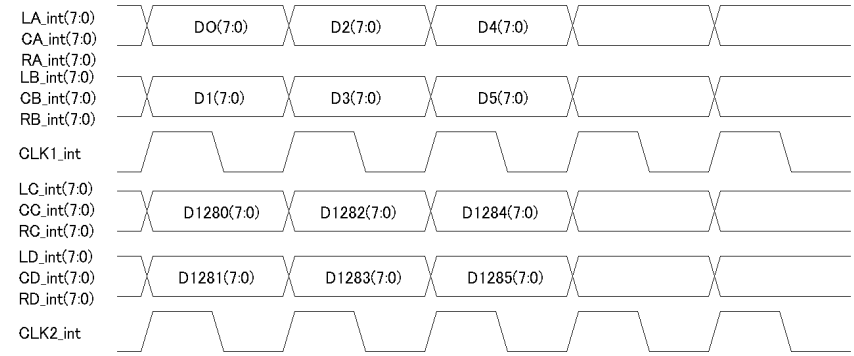
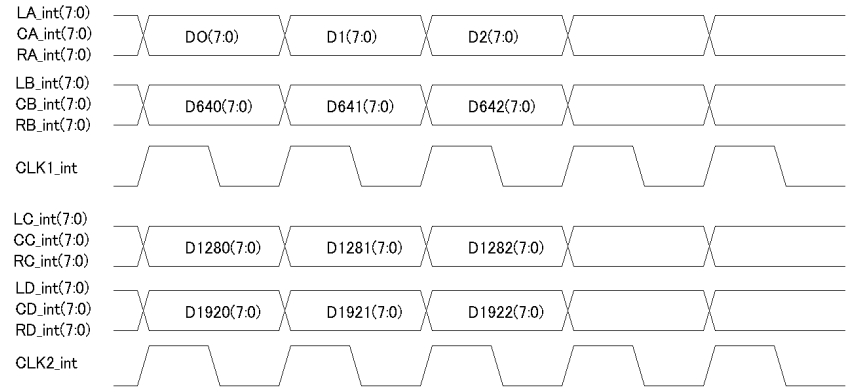
Note2: In case tLPW exceeds 50ms, backlight will turn off by its protection circuits.

Note3: Max. Luminance at 100%

Attention: External pulse control for luminance may be disturbed the display image when set up frequency is interfered with internal signal frequency.

(5) LVDS data transmission mode

LVDS data transmission mode is selectable with MOD0, and MOD1 terminal.

MOD0 to 1 Terminal Note1		mode name	data transmission chart
1	0		
H	H	mode 0 L/R transmission mode	
H	L	mode 1 4divided transmission mode	
L	H	Reserved	---
L	L	Reserved	---

Note1: "H" must be "OPEN"

12. METHOD OF CONNECTION FOR LVDS TRANSMITTER

LVDS data bit mapping mode is selectable with BSEL0, and BSEL1 terminal.

	Bit mapping			Transmitter Pin Assign				CN1	
	BSEL[1:0]			Singl type LVDS Tx	Dual type LVDS TX		Output Connector	Pin No.	Signal name
	[H:H]	[H:L]	[L:H]		Thine THC63LVD823	NS DS90C387			
pixel data A	L2	L7	L0	TA0	R12	R10	ATA- ATA+		
	L3	L6	L1	TA1	R13	R11			
	L4	L5	L2	TA2	R14	R12		40	DA0-
	L5	L4	L3	TA3	R15	R13		39	DA0+
	L6	L3	L4	TA4	R16	R14			
	L7	L2	L5	TA5	R17	R15			
	C2	C7	C0	TA6	G12	G10			
	C3	C6	C1	TB0	G13	G11	ATB- ATB+		
	C4	C5	C2	TB1	G14	G12			
	C5	C4	C3	TB2	G15	G13		37	DA1-
	C6	C3	C4	TB3	G16	G14		36	DA1+
	C7	C2	C5	TB4	G17	G15			
	R2	R7	R0	TB5	B12	B10			
	R3	R6	R1	TB6	B13	B11			
	R4	R5	R2	TC0	B14	B12	ATC- ATC+		
	R5	R4	R3	TC1	B15	B13			
	R6	R3	R4	TC2	B16	B14		34	DA2-
	R7	R2	R5	TC3	B17	B15		33	DA2+
	Hsync	Hsync	Hsync	TC4	HSYNC	HSYNC			
	Vsync	Vsync	Vsync	TC5	VSYNC	VSYNC			
	DE	DE	DE	TC6	DE	DE			
	L0	L1	L6	TD0	R10	R16	ATD- ATD+		
	L1	L0	L7	TD1	R11	R17			
	C0	C1	C6	TD2	G10	G16		28	DA3-
	C1	C0	C7	TD3	G11	G17		27	DA3+
	R0	R1	R6	TD4	B10	B16			
	R1	R0	R7	TD5	B11	B17			
	NC	NC	NC	TD6	-	-			
	CLK	CLK	CLK	CLK	CLK	CLK	ATCLK- ATCLK+	31	CKA-
								30	CKA+
pixel data B	L2	L7	L0	TA0	R22	R20	BTA- BTA+		
	L3	L6	L1	TA1	R23	R21			
	L4	L5	L2	TA2	R24	R22		25	DB0-
	L5	L4	L3	TA3	R25	R23		24	DB0+
	L6	L3	L4	TA4	R26	R24			
	L7	L2	L5	TA5	R27	R25			
	C2	C7	C0	TA6	G22	G20			
	C3	C6	C1	TB0	G23	G21	BTB- BTB+		
	C4	C5	C2	TB1	G24	G22			
	C5	C4	C3	TB2	G25	G23		22	DB1-
	C6	C3	C4	TB3	G26	G24		21	DB1+
	C7	C2	C5	TB4	G27	G25			
	R2	R7	R0	TB5	B22	B20			
	R3	R6	R1	TB6	B23	B21			
	R4	R5	R2	TC0	B24	B22	BTC- BTC+		
	R5	R4	R3	TC1	B25	B23			
	R6	R3	R4	TC2	B26	B24		19	DB2-
	R7	R2	R5	TC3	B27	B25		18	DB2+
	Hsync	Hsync	Hsync	TC4	HSYNC	HSYNC			
	Vsync	Vsync	Vsync	TC5	VSYNC	VSYNC			
	DE	DE	DE	TC6	DE	DE			
	L0	L1	L6	TD0	R20	R26	BTD- BTD+		
	L1	L0	L7	TD1	R21	R27			
	C0	C1	C6	TD2	G20	G26		13	DB3-
	C1	C0	C7	TD3	G21	G27		12	DB3+
	R0	R1	R6	TD4	B20	B26			
	R1	R0	R7	TD5	B21	B27			
	NC	NC	NC	TD6	-	-			
	CLK	CLK	CLK	CLK	CLK	CLK	BTCLK- BTCLK+	16	CKB-
								15	CKB+

	BSEL[1:0]			Singl type LVDS Tx	Dual type LVDS TX		Output Connector	CN2	
	[H:H]	[H:L]	[L:H]		Thine THC63LVD823	NS DS90C387		Pin No.	Signal name
pixel data C	L2	L7	L0	TA0	R12	R10	CTA- CTA+		
	L3	L6	L1	TA1	R13	R11			
	L4	L5	L2	TA2	R14	R12		30	DC0-
	L5	L4	L3	TA3	R15	R13		29	DC0+
	L6	L3	L4	TA4	R16	R14			
	L7	L2	L5	TA5	R17	R15			
	C2	C7	C0	TA6	G12	G10			
	C3	C6	C1	TB0	G13	G11	CTB- CTB+		
	C4	C5	C2	TB1	G14	G12			
	C5	C4	C3	TB2	G15	G13		27	DC1-
	C6	C3	C4	TB3	G16	G14		26	DC1+
	C7	C2	C5	TB4	G17	G15			
	R2	R7	R0	TB5	B12	B10			
	R3	R6	R1	TB6	B13	B11			
	R4	R5	R2	TC0	B14	B12	CTC- CTC+		
	R5	R4	R3	TC1	B15	B13			
	R6	R3	R4	TC2	B16	B14		24	DC2-
	R7	R2	R5	TC3	B17	B15		23	DC2+
	Hsync	Hsync	Hsync	TC4	HSYNC	HSYNC			
	Vsync	Vsync	Vsync	TC5	VSYNC	VSYNC			
	DE	DE	DE	TC6	DE	DE			
	L0	L1	L6	TD0	R10	R16	CTD- CTD+		
	L1	L0	L7	TD1	R11	R17			
	C0	C1	C6	TD2	G10	G16		18	DC3-
	C1	C0	C7	TD3	G11	G17		17	DC3+
	R0	R1	R6	TD4	B10	B16			
	R1	R0	R7	TD5	B11	B17			
	NC	NC	NC	TD6	-	-			
	CLK	CLK	CLK	CLK	CLK	CLK	CTCLK- CTCLK+	21	CKC-
								20	CKC+
Pixel data D	L2	L7	L0	TA0	R22	R20	DTA- DTA+		
	L3	L6	L1	TA1	R23	R21			
	L4	L5	L2	TA2	R24	R22		15	DD0-
	L5	L4	L3	TA3	R25	R23		14	DD0+
	L6	L3	L4	TA4	R26	R24			
	L7	L2	L5	TA5	R27	R25			
	C2	C7	C0	TA6	G22	G20			
	C3	C6	C1	TB0	G23	G21	DTB- DTB+		
	C4	C5	C2	TB1	G24	G22			
	C5	C4	C3	TB2	G25	G23		12	DD1-
	C6	C3	C4	TB3	G26	G24		11	DD1+
	C7	C2	C5	TB4	G27	G25			
	R2	R7	R0	TB5	B22	B20			
	R3	R6	R1	TB6	B23	B21			
	R4	R5	R2	TC0	B24	B22	DTC- DTC+		
	R5	R4	R3	TC1	B25	B23			
	R6	R3	R4	TC2	B26	B24		9	DD2-
	R7	R2	R5	TC3	B27	B25		8	DD2+
	Hsync	Hsync	Hsync	TC4	HSYNC	HSYNC			
	Vsync	Vsync	Vsync	TC5	VSYNC	VSYNC			
	DE	DE	DE	TC6	DE	DE			
	L0	L1	L6	TD0	R20	R26	DTD- DTD+		
	L1	L0	L7	TD1	R21	R27			
	C0	C1	C6	TD2	G20	G26		3	DD3-
	C1	C0	C7	TD3	G21	G27		2	DD3+
	R0	R1	R6	TD4	B20	B26			
	R1	R0	R7	TD5	B21	B27			
	NC	NC	NC	TD6	-	-			
	CLK	CLK	CLK	CLK	CLK	CLK	DTCLK- DTCLK+	6	CKD-
								5	CKD+

13. DISPLAY GRAYSCALES vs. INPUT DATA SIGNALS

Display colors		Data signal (0: Low level, 1: High level)																									
		LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
		LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
		LC7	LC6	LC5	LC4	LC3	LC2	LC1	LC0	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	RC7	RC6	RC5	RC4	RC3	RC2	RR1	RR0
		LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
Left grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑	:								:								:							
	↓	:								:								:							
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Center grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑	:								:								:							
	↓	:								:								:							
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	White	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Right grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑	:								:								:							
	↓	:								:								:							
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	White	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note1: The combination of 8-bit signals results in equivalent to 256 grayscale.

14. 10BIT LOOK UP TABLE FOR GAMMA ADJUSTMENT

Table1: Serial data Composition

DATA	DATA name	Function	Remarks
D31	CMD5	Control Command	See table2.
D30	CMD4	Control Command	
D29	CMD3	Control Command	
D28	CMD2	Control Command	
D27	CMD1	Control Command	
D26	CMD0	Control Command	
D25	ADD9	LUT Address (MSB)	See table3.
D24	ADD8	LUT Address	
D23	ADD7	LUT Address	
D22	ADD6	LUT Address	
D21	ADD5	LUT Address	
D20	ADD4	LUT Address	
D19	ADD3	LUT Address	
D18	ADD2	LUT Address	
D17	ADD1	LUT Address	
D16	ADD0	LUT Address (LSB)	
D15	Dummy	Dummy Data “0”	See table4.
D14	Dummy	Dummy Data “0”	
D13	Dummy	Dummy Data “0”	
D12	Dummy	Dummy Data “0”	
D11	Dummy	Dummy Data “0”	
D10	Dummy	Dummy Data “0”	
D9	DATA9	LUT Data (MSB)	
D8	DATA8	LUT Data	
D7	DATA7	LUT Data	
D6	DATA6	LUT Data	
D5	DATA5	LUT Data	
D4	DATA4	LUT Data	
D3	DATA3	LUT Data	
D2	DATA2	LUT Data	
D1	DATA1	LUT Data	
D0	DATA0	LUT Data (LSB)	

Table2: Command table (CMD5 to CMD0 : 6bit)

DATA name	Parameter	Remarks
CMD5	Must be set “1” for normal operation	-
CMD4	Must be set “1” for normal operation	-
CMD3	“1”: Word write “0”: Sequential write	-
CMD2	Must be set “1” for normal operation	-
CMD1	“1”: Single sub pixel data write “0”: Three sub pixel data write	“1”: Use ADD9,ADD8 “0”: Not use ADD9,ADD8
CMD0	Must be set “0” for normal operation	-

Table2: Address table (ADD9 to ADD0 : 10bit)

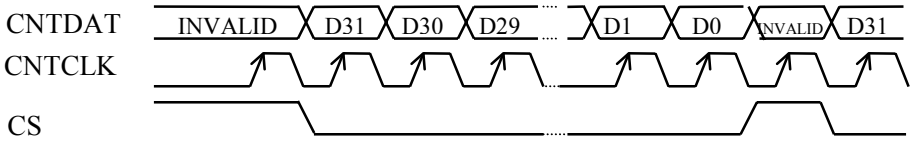
DATA name	Parameter	Remarks
ADD9	Sub pixel Select ADD9:8= 0:0 Left 0:1 Center 1:0 Right 1:1 Command	-
ADD8		
ADD7	LUT Address (=Input Data) 256 address 00h – FFh	If ADD9:8 = 1:1. Must be set ADD7:0 = 00h.
ADD6		
ADD5		
ADD4		
ADD3		
ADD2		
ADD1		
ADD0		

Table3: Data table (DATA15 to DATA0 : 16bit)

DATA	DATA name	Parameter	Remarks
D15	Dummy	Dummy Data Must be set “0”	-
D14	Dummy		
D13	Dummy		
D12	Dummy		
D11	Dummy		
D10	Dummy		
D9	DATA9	10bit LUT Data 000h – 3FFh	Set ADD9:0=300h DATA9:0=000h : Disable LUT (default) DATA9:0=001h : Enable LUT
D8	DATA8		
D7	DATA7		
D6	DATA6		
D5	DATA5		
D4	DATA4		
D3	DATA3		
D2	DATA2		
D1	DATA1		
D0	DATA0		

15. LUT SERIAL COMMUNICATION TIMINGS

Write timing

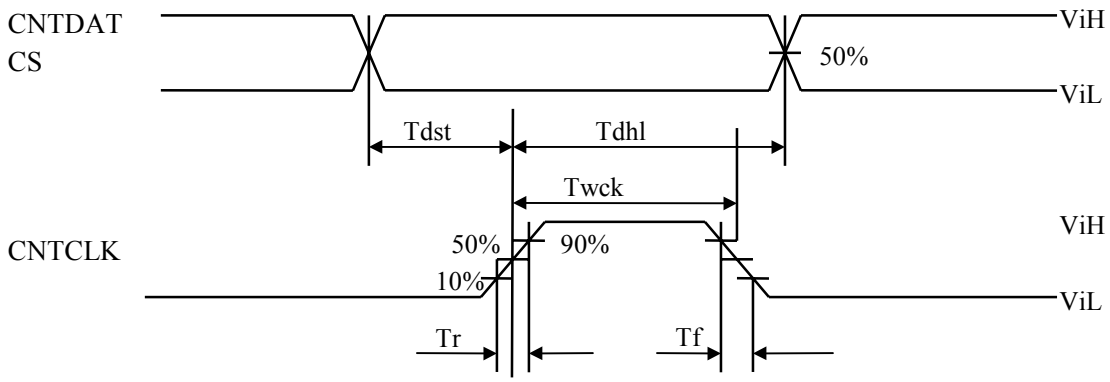


Word write mode

Sequential write mode

Parameter	Symbol	Min.	Max.	Unit	Remarks
CLK pulse-width	Twck	50	-	ns	CNTCLK
CLK frequency	Fclk	-	5	MHz	
DATA,CS set-up-time	Tdst	50	-	ns	CNTDAT,CS
DATA,CS hold-time	Tdhl	50	-	ns	

SERIAL COMMUNICATION WAVEFORM



16. INPUT SIGNAL TIMINGS

(1) Input signal specifications

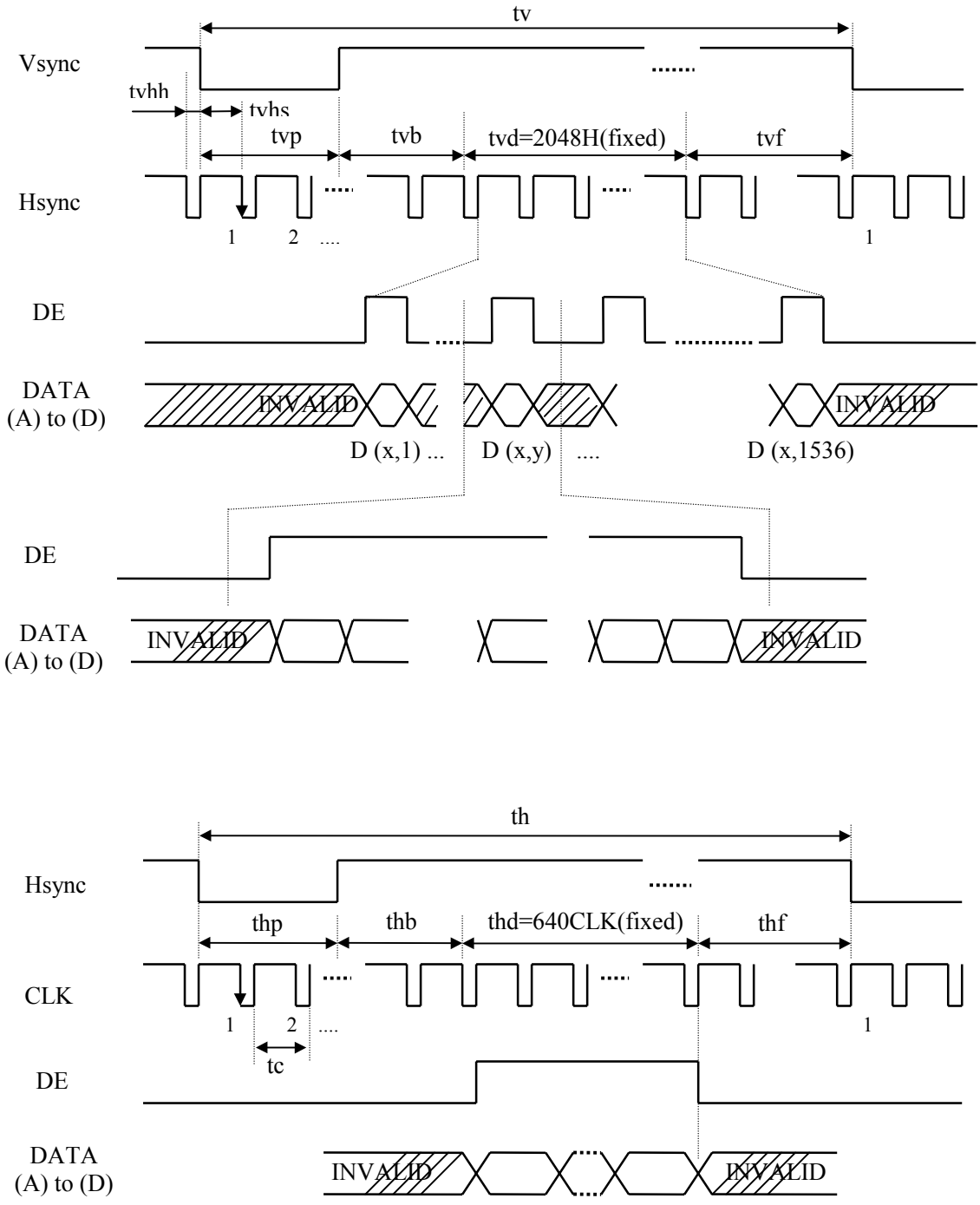
Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency	1/ tc	80.0 -	83.26 12.01	85.0 -	MHz ns	-
	Duty	tc / tcl	Note1			-	-
	Rise, fall	tcrf				ns	-
Hsync	Period	th	7.72 660	8.071 672	- 690	µs CLK	Typ=123.9kHz Note3
	Display period	thd	640			CLK	-
	Blank	thp+thb+thf	20	32	50	CLK	-
Vsync	Period	tv	- 2053	16.667 2064	- -	ms H	Typ=60.0Hz
	Display period	tvd	2048			H	-
	Blank	tvp+tvb+tvf	5	16	-	H	-
DE	CLK-DE set-up	tdes	Note1			ns	-
	CLK-DE hold	tdeh				ns	-
	Raise,fall	tderf				ns	-
DATA	CLK-DATA set-up	tds	Note1			ns	-
	CLK-DATA hold	tdh				ns	-
	Rise, fall	tdrf				ns	-

Note1: Timing specifications are defined by the input signals of LVDS transmitter.
THC63LVD823 (THine) or equivalent products are recommended for LVDS transmitter.

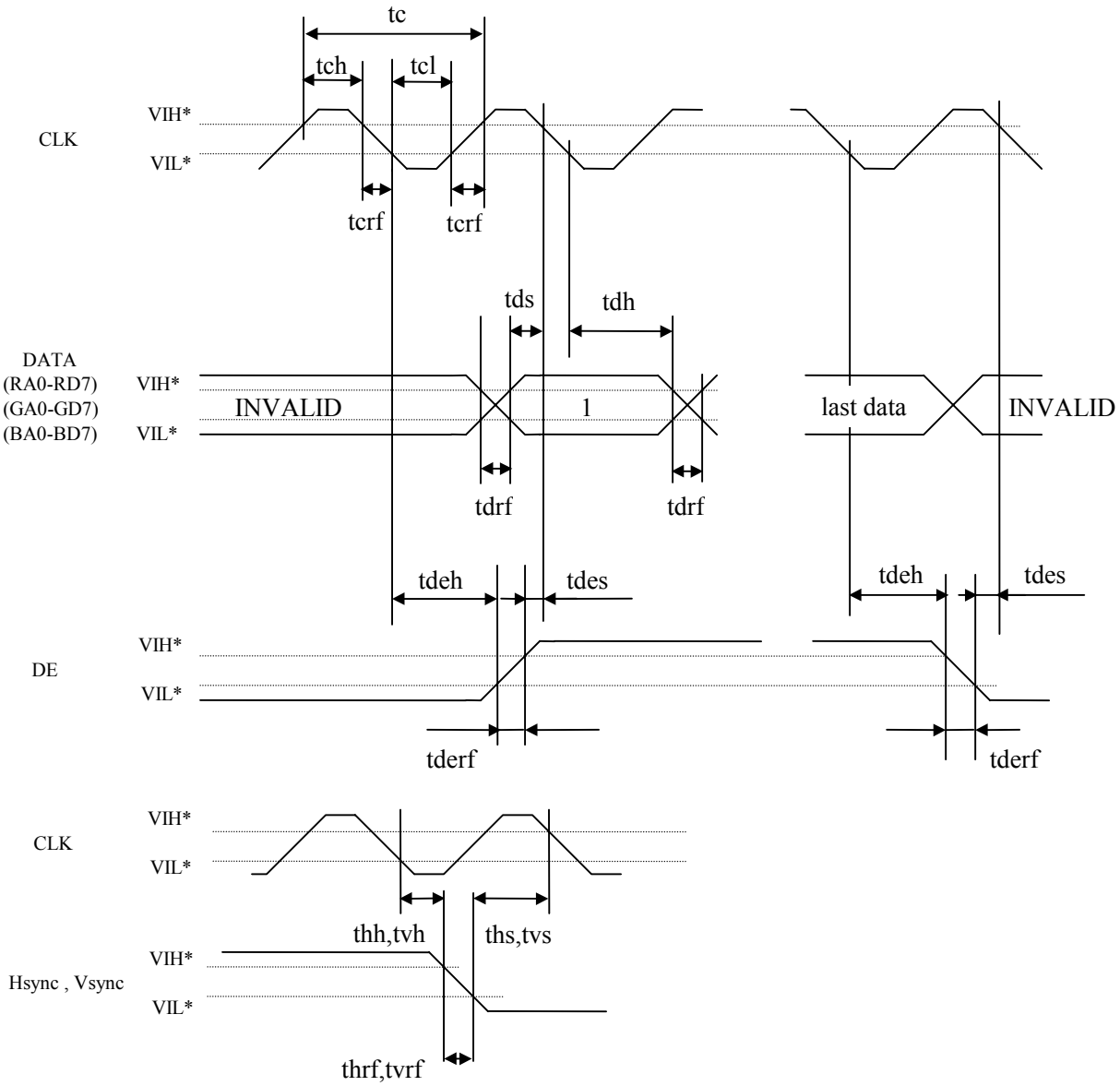
Note2: Both of “time” and “CLK number” of the “th” must keep the Minimum value of specification.

Note3: "th" (CLK number) should be fixed to 2n (n= natural number: 1,2,3···). In case "th" is not the specified value, it may cause display deterioration.
e.g.: "th" (CLK number)
660, 662, 664, ··· 672, 674, ··· 688, 690

(2) Input signals timing chart



[Detail of input signals timing chart]

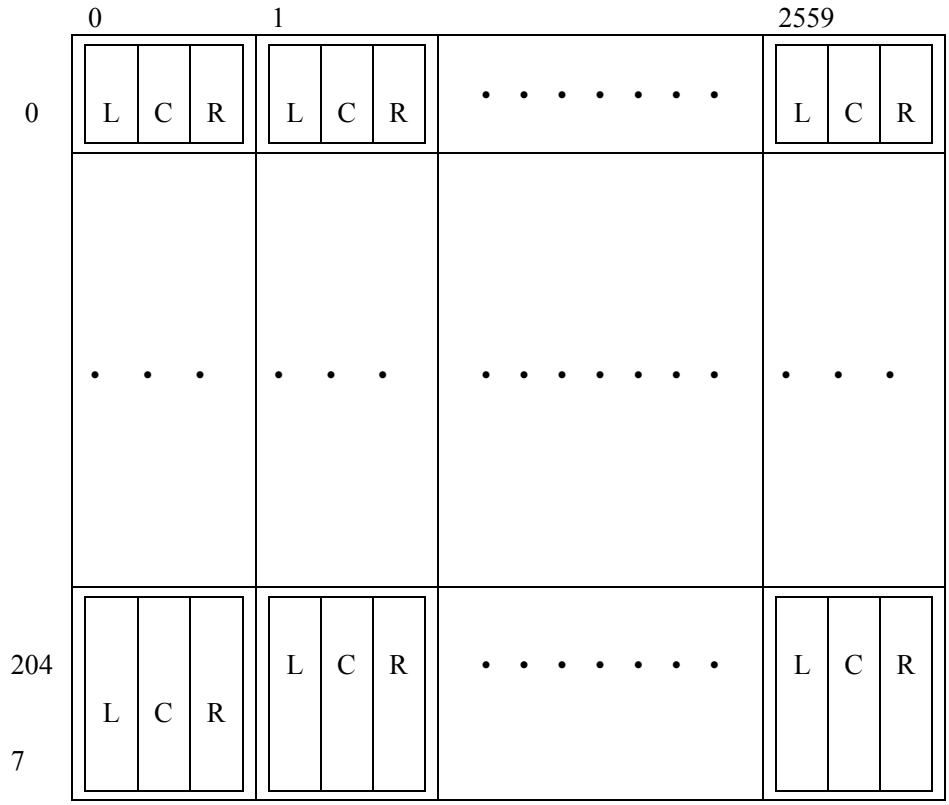


* See the specifications of LVDS manufactures for detailed design.

(3) Display positions of input data

D(0,0)	D(1,0)	•••	D(2559,0)
D(0,1)	D(1,1)	•••	D(2559,1)
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
D(0,2047)	D(1,2047)	•••	D(2559,2047)

(4) Pixel Arrangement



17. OPTICAL CHARACTERISTICS

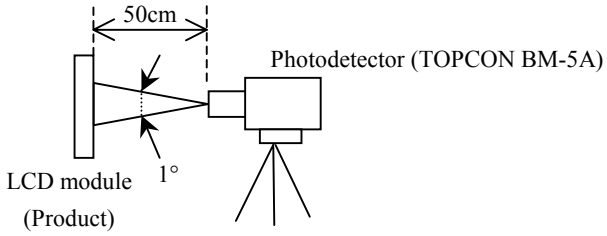
(Note1)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Remarks
Contrast ratio	CR	Note2		-	600	-	-	Note3
Luminance	L	White, Note2		-	850	-	cd/m^2	-
Luminance uniformity	LU	Max. / Min.		-	1.1	1.3	-	Note6
Chromaticity Coordinates	-	White (x, y)		-	(0.255, 0.310)	-	-	Note2
Viewing angle range	θx+	CR > 10, White/Black θy±=0°		-	85	-	deg.	Note4
	θx-			-	85	-	deg.	
	θy+	CR > 10, White/Black θx±=0°		-	85	-	deg.	
	θy-			-	85	-	deg.	
Response time (Module surface temperature :TBD)	Ton	Black to White	10% → 90%	-	15	-	ms	Note5
	Toff	White to Black	90% → 10%	-	15	-	ms	Note5
Luminance control range	-	Maximum luminance: 100%		-	30 to 100	-	%	-

Note1: Measurement conditions are as follows.

Ta = 25°C, VDD = 12V, VDDB=12V, Display mode: QSXGA, Horizontal cycle = 123.9kHz, Vertical cycle = 60.0Hz

Optical characteristics are measured at luminance saturation after 20minutes from working the product, in the dark room. Also measurement method for luminance is as follows.

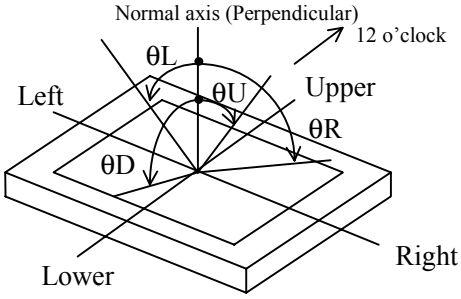


Note2: Viewing angle is θx = ±0°, θy = ±0°. at center.

Note3: The contrast ratio is calculated by using the following formula.

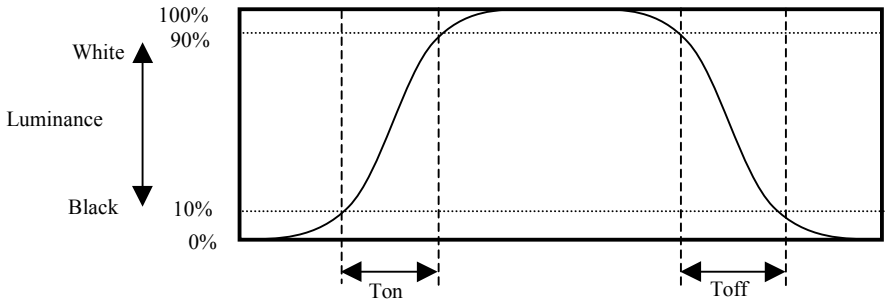
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in “white”}}{\text{Luminance with all pixels in “black”}}$$

Note4: Definition of viewing angles



Note5: Definition of response times

Response time is measured, the luminance changes from " black " to " white ", or " white " to " black " on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).

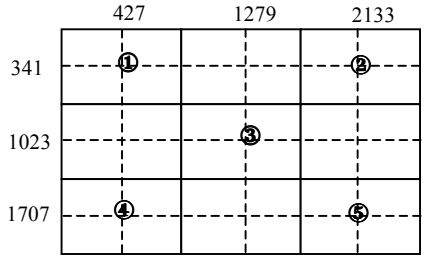


Note6: Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

$$\text{Luminance uniformity} = \frac{\text{Maximum Luminance}}{\text{Minimum Luminance}}$$

The luminance is measured at near the 5 points shown below.

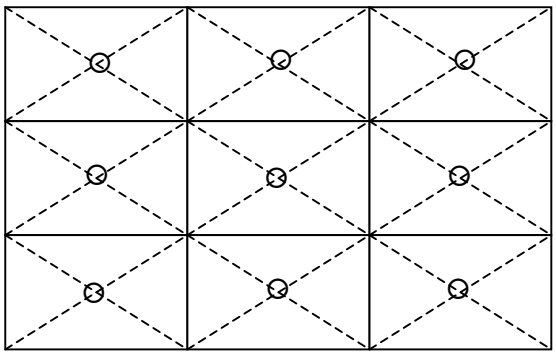


18. RELIABILITY TESTS

Test item		Condition	Judgment
High temperature and humidity (Operation)		① 60 ± 2°C, RH = 60%, 240hours ② Display data is white.	No display malfunctions Note1
Heat cycle (Operation)		① 0 ± 3°C…1hour 55 ± 3°C…1hour ② 50cycles, 4hours/cycle ③ Display data is white.	No display malfunctions Note1
Thermal shock (Non operation)		① -20 ± 3°C…30minutes 60 ± 3°C…30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	No display malfunctions Note1
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s^2 ② 1 minute/cycle ③ X, Y, Z direction ④ 10 times each directions	No display malfunctions Note1 No physical damages
Mechanical shock (Non operation)		① 294m/ s^2, 11ms ② X, Y, Z direction ③ 3 times each directions	No display malfunctions Note1 No physical damages
ESD (Operation)		① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	No display malfunctions Note1
Dust (Operation)		① Sample dust: No.15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	No display malfunctions Note1
Low pressure	operation	① 53.3 kPa ② 0°C±3°C…24 hours ③ 55°C±3°C…24 hours	No display malfunctions Note1
	non-operation	① 15 kPa ② -20°C±3°C…24 hours ③ -60°C±3°C…24 hours	

Note1: Display functions are checked under the same conditions as product inspection.

Note2: See the following figure for discharge points



19. PRECAUTIONS

19.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "19.2 CAUTIONS", after understanding this contents!**

⚠CAUTION	This sign has a meaning that customer will be injured himself and/or the product will sustain a damage, if customer makes a mistake in operations.

This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.

This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

19.2 CAUTIONS

Do not touch HIGH VOLTAGE PART of the inverter while turn on. Customer will be in danger of an electric shock.

∗ Pay attention to burn injury for the working IC! It may be over 35°C from ambient temperature.

∗ Do not shock and press the LCD panel and the backlight lamp! There is a danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s^2 and to be not greater 11ms, Pressure: To be not greater 19.6N)

19.3 ATTENTIONS

(1) Handling of the product

① Take hold of both ends without touch the circuit board when customer pulls out products (LCD modules) from inner packing box. If customer touches it, products may be broken down or out of adjustment, because of stress to mounting parts.

② If customer puts down the product temporarily, the product puts on flat subsoil as a display side turns down.

③ Take the measures of electrostatic discharge such as earth band, ionic shower and so on, when customer deals with the product, because products may be damaged by electrostatic.

④ The torque for mounting screws must never exceed 0.34N·m. Higher torque values might result in distortion of the bezel.

⑤ Do not press or rub on the sensitive display surface. If customer clean on the panel surface, NEC Corporation recommends using the cloth with ethanolic liquid such as screen cleaner for LCD.

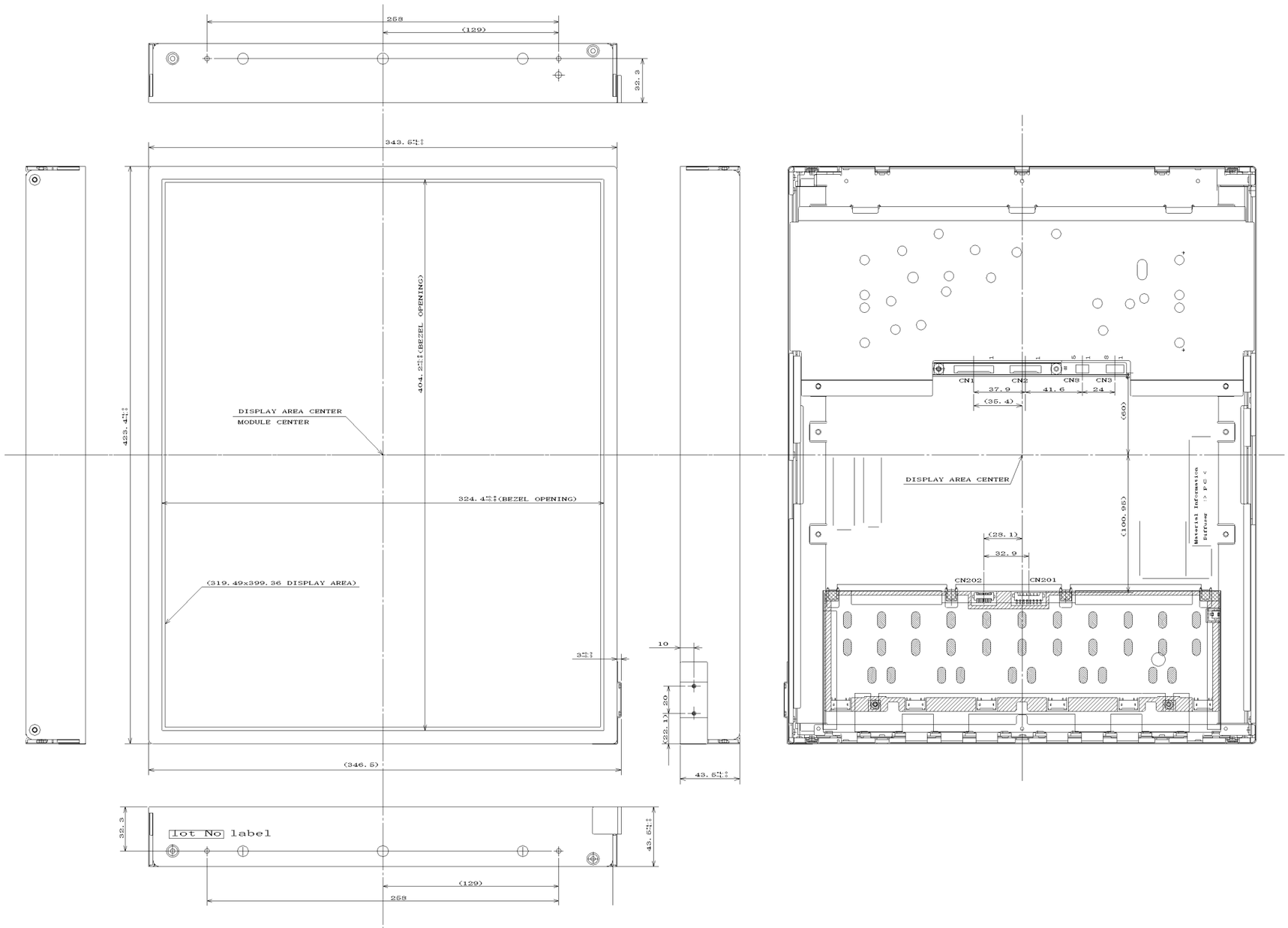
⑥ Do not push-pull the interface connectors while the product is working, because wrong power sequence may break down the product.
⑦ Do not hook cables nor pull connection cables such as flexible cable and so on, for fear of damage.

(2) Environment
① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in antistatic pouch in room temperature, because of avoidance for dusts and sunlight, if customer stores the product.
② Do not operate in high magnetic field. Circuit boards may be broken down by it.
③ Use an original protection sheet on the product surface (polarizer). Adhesive type protection sheet should be avoided, because it may change color or properties of the polarizer.

(3) Characteristics
① Response time, luminance and color may be changed by ambient temperature.
② The LCD may be seemed luminance non-uniformity, flicker, vertical seam or small spot by display patterns.
③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
⑤ The display color may be changed by viewing angle because of the use of condenser sheet in the backlight unit.
⑥ Optical characteristics may be changed by input signal timings.
⑦ The interference noise of input signal frequency for this product's signal processing board and luminance control frequency of customer's backlight inverter may appear on a display. Set up luminance control frequency of backlight inverter so that the interference noise does not appear.
⑧ The product may be changed of luminance by voltage variation, even if power source applies recommended voltage to backlight inverter.
⑨ Optical characteristics may be changed by input signal timings.

(4) Other
① All GND, GNDB, VDD and VDDB terminals should be connected without a non-connected signal line.
② Do not disassemble a product or adjust volume without permission of NEC Corporation.
③ See "REPLACEMENT MANUAL FOR LAMPHOLDER SET", if customer would like to replace backlight lamps.
④ Pay attention not to insert waste materials inside of products, if customer uses screwnails.
⑤ When customer returns product for repair and so on, pack it with original shipping package because of avoidance of some damages during transportation.
⑥ Not only the module but also the equipment that used the module should be packed and transported as the module becomes vertical.Otherwise, there is the fear that a display dignity decreases by an impact or vibrations."

20. OUTLINE DRAWINGS



Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The dimensions in parenthesis are for reference.

Unit: mm

REVISION HISTORY

Edition	Document number	Prepared date	Revision contents and signature
1st edition	DOD-M-1167	Sep. 25, 2002	**Revision contents** New issue **Signature of writer** *Approved by* T. ITO *Checked by* *Prepared by* R. KAWASHIMA