Low Voltage Single Supply SPDT Analog Switch

NL5S4599, NL5ST4599

The NL5S4599 and NL5ST4599 are advanced high speed CMOS single pole − double throw (SPDT) analog switches fabricated with silicon gate CMOS technology. These achieve high speed propagation delays and low ON resistances while maintaining low power dissipation. These switches control analog and digital voltages that may vary across the full power-supply range (from V_{CC} to GND).

These devices have been designed so the ON resistance (R_{ON}) is much lower and more linear over the input voltage range than R_{ON} of typical CMOS analog switches.

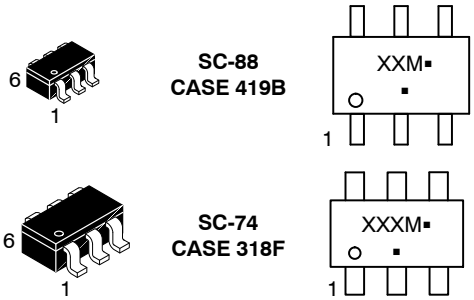
The channel select input structures of these devices provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. These input structures help prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc.

The NL5S4599 has CMOS level channel select input while the NL5ST4599 has TTL level channel select input.

Features

- Channel Select Input Over-Voltage Tolerant to 5.5 V
- Fast Switching and Propagation Speeds
- Break-Before-Make Circuitry
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25 °C
- Diode Protection Provided on Channel Select Input
- Improved Linearity and Lower ON Resistance Over Input Voltage
- ESD Performance: Human Body Model > 4000 V
- Chip Complexity: 38 FETs
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS-Compliant

MARKING DIAGRAMS



XX = Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

FUNCTION TABLE

Select	ON Channel
L	NC
H	NO

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 9 of this data sheet.

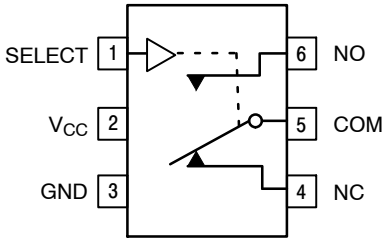


Figure 1. Pinout (Top View)

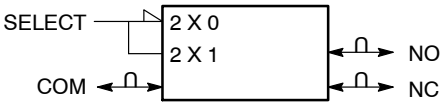


Figure 2. Logic Symbol

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MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		−0.5 to +6.5	V
V_{IS}	Analog I/O Voltage		−0.5 to V_{CC} + 0.5	V
V_{IN}	Select Pin Voltage		−0.5 to +6.5	V
I_{IN}	DC Current, In or Out of Any Pin		±128	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)	SC-88 SC-74	377 320	°C/W
P_D	Power Dissipation in Still Air at 25 °C	SC-88 SC-74	332 390	mW
MSL	Moisture Sensitivity		Level 1	–
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	–
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	4000 2000	V
$I_{LATCHUP}$	Latchup Performance (Note 3)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10mm-by-1inch, 2 ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
3. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		2.0	5.5	V
V_{IN}	Select Input Voltage (Note 4)		0	5.5	V
V_{IS}	Analog I/O Voltage (NC, CO, COM)		0	V_{CC}	V
T_A	Operating Free-Air Temperature		−55	+125	°C
t_r, t_f	Select Input Rise or Fall Time	V_{CC} = 3.0 V to 3.6 V V_{CC} = 4.5 V to 5.5 V	0 0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Select input must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). It must not float.

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DC ELECTRICAL CHARACTERISTICS – SELECT Input and Supply

Symbol	Parameter	Conditions	V_{CC} (V)	Maximum			Unit
				–55 to 25 °C	<85 °C	<125 °C	
NL5S4599							
V_{IH}	Minimum High-Level Input Voltage, SELECT Input		2.0 2.5 3.0 4.5 5.5	1.5 1.9 2.1 3.15 3.85	1.5 1.9 2.1 3.15 3.85	1.5 1.9 2.1 3.15 3.85	V
V_{IL}	Maximum Low-Level Input Voltage, SELECT Input		2.0 2.5 3.0 4.5 5.5	0.5 0.6 0.9 1.35 1.65	0.5 0.6 0.9 1.35 1.65	0.5 0.6 0.9 1.35 1.65	V
NL5ST4599							
V_{IH}	Minimum High-Level Input Voltage, SELECT Input		3.0 4.5 5.5	1.5 2.0 2.0	1.5 2.0 2.0	1.5 2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage, SELECT Input		3.0 4.5 5.5	0.5 0.8 0.8	0.5 0.8 0.8	0.5 0.8 0.8	V
NL5S4599 and NL5ST4599							
I_{IN}	Maximum Input Leakage Current, SELECT Input	V_{IN} = 5.5 V or GND	5.5	±0.1	±1.0	±1.0	μA
I_{OFF}	Power Off Leakage Current, SELECT Input	V_{IN} = 5.5 V or GND	0	±10	±10	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} and V_{IS} = V_{CC} or GND	5.5	1.0	1.0	2.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DC ELECTRICAL CHARACTERISTICS – Analog

Symbol	Parameter	Conditions	V_{CC} (V)	Maximum			Unit
				–55 to 25 °C	<85 °C	<125 °C	
R_{ON}	Switch "ON" Resistance (Figures 17 – 23)	V_{IS} = V_{CC} $\|I_{IN}\|$ = 10.0 mA	2.5 3.0 4.5 5.5	85 60 30 25	95 65 35 30	105 70 40 35	Ω
R_{FLAT}	ON Resistance Flatness (Figures 17 – 23)	V_{IS} = V_{CC} $\|I_{IN}\|$ = 10.0 mA	4.5	6	6	7	Ω
ΔR_{ON}	ON Resistance Match Between Channels	V_{IS} = 3.5 V $\|I_{IN}\|$ = 10.0 mA	4.5	4	4	5	Ω
$I_{NC(OFF)}$ $I_{NO(OFF)}$	NO or NC Switch Off Leakage Current (Figure 9)	V_{IN} = V_{IL} or V_{IH} V_{NO} or V_{NC} = 1.0 V V_{COM} = 4.5 V	5.5	1	10	100	nA
$I_{COM(ON)}$	NO or NC Switch ON Leakage Current (Figure 9)	V_{IN} = V_{IL} or V_{IH} V_{NO} = 1.0 V or 4.5 V with NC floating V_{NC} = 1.0 V or 4.5 V with NO floating V_{COM} = 1.0 V or 4.5 V	5.5	1	10	100	nA

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	V_{IS} (V)	−55 to 25 °C			<85 °C		<125 °C		Unit
					Min	Typ*	Max	Min	Max	Min	Max	
t_{ON}	Turn-On Time (Figures 12, 13)	R_L = 300 Ω, C_L = 35 pF (Figures 5, 6)	2.5 3.0 4.5 5.5	2.0 2.0 3.0 3.0	5 5 2 2	13 11 9 8	28 21 16 14	5 5 2 2	30 25 20 20	5 5 2 2	30 25 20 20	ns
t_{OFF}	Turn-Off Time (Figures 12, 13)	R_L = 300 Ω, C_L = 35 pF (Figures 5, 6)	2.5 3.0 4.5 5.5	2.0 2.0 3.0 3.0	1 1 1 1	7 7 6 6	12 10 9 8	1 1 1 1	15 15 12 12	1 1 1 1	15 15 12 12	ns
t_{BBM}	Break-Before-Make Time	R_L = 300 Ω, C_L = 35 pF, V_{IS} = 3.0 V (Figure 4)	2.5 3.0 4.5 5.5	2.0 2.0 3.0 3.0	1 1 1 1	7 5 4 4		1 1 1 1		1 1 1 1		ns

*Typical Characteristics are at 25 °C.

CAPACITANCE CHARACTERISTICS

Symbol	Parameter	Test Condition	V_{CC} (V)	Typical (T_A = 25 °C)	Unit
C_{IN}	SELECT Input Capacitance		5.0	8	pF
C_{NO} or C_{NC}	Analog I/O (Switch OFF)		5.0	10	pF
C_{ON}	Feedthrough (Switch ON)		5.0	26	pF
C_{COM}	Common I/O		5.0	20	pF

ADDITIONAL APPLICATION CHARACTERISTICS

Symbol	Parameter	Test Condition	V_{CC} (V)	Typical (T_A = 25 °C)	Unit
BW	ON-Channel −3 dB Bandwidth (Figure 10)	V_{IN} = 0 dBm, V_{IN} centered between V_{CC} and GND (Figure 7)	3.0 4.5 5.5	170 200 200	MHz
V_{ONL}	Feedthrough ON Loss	V_{IN} = 0 dBm @ 100 kHz to 50 MHz, V_{IN} centered between V_{CC} and GND (Figure 7)	3.0 4.5 5.5	−3.0 −2.0 −2.0	dB
V_{ISO}	Off-Channel Isolation (Figure 10)	f = 100 kHz, V_{IS} = 1 V_{RMS}, V_{IN} centered between V_{CC} and GND (Figure 7)	3.0 4.5 5.5	−93 −93 −93	dB
Q	Charge Injection, SELECT to Common I/O (Figure 15)	V_{IN} = V_{CC} to GND, f_{IS} = 20 kHz, t_r = t_f = 3 ns, R_{IS} = 0 Ω, C_L = 1000 pF, Q = C_L * ΔV_{OUT} (Figure 8)	3.0 5.5	1.5 3.0	pC
THD+N	Total Harmonic Distortion + Noise (Figure 14)	f_{IS} = 20 Hz to 100 kHz, R_L = R_{gen} = 600 Ω, C_L = 50 pF, V_{IS} = 5.0 V_{PP} sine wave	5.5	0.1	%

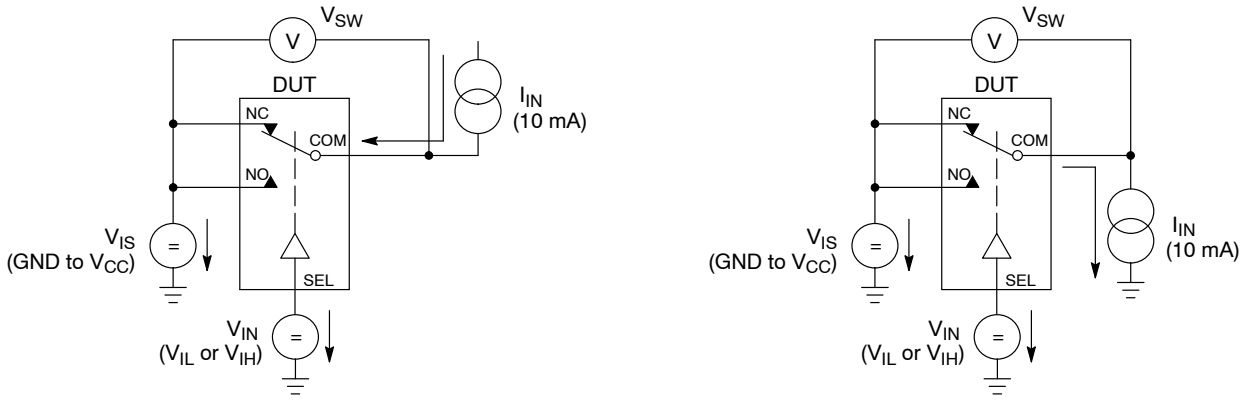

Figure 3. R_{ON} (ON Resistance)

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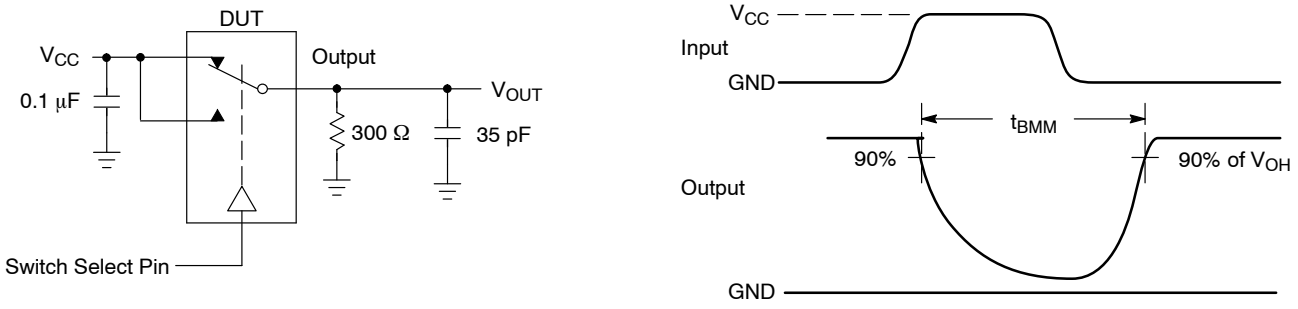

Figure 4. t_{BBM} (Break-Before-Make Time)

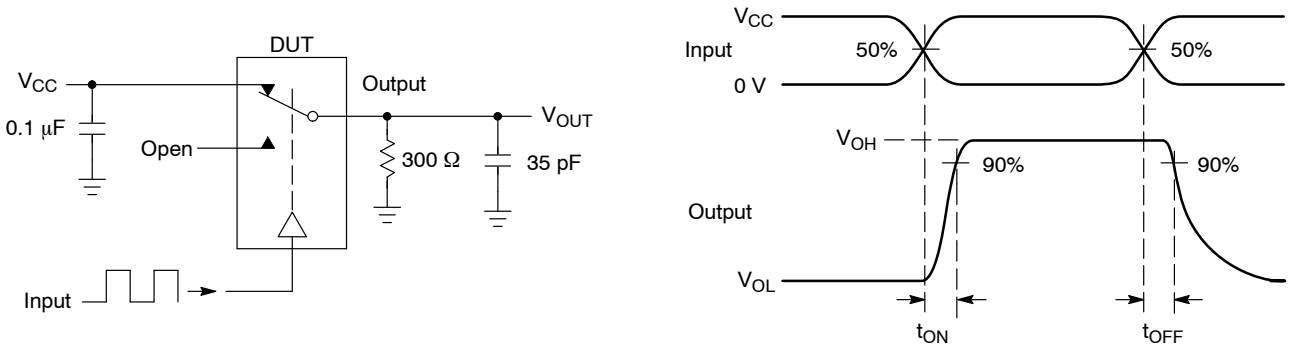

Figure 5. t_{ON}/t_{OFF}

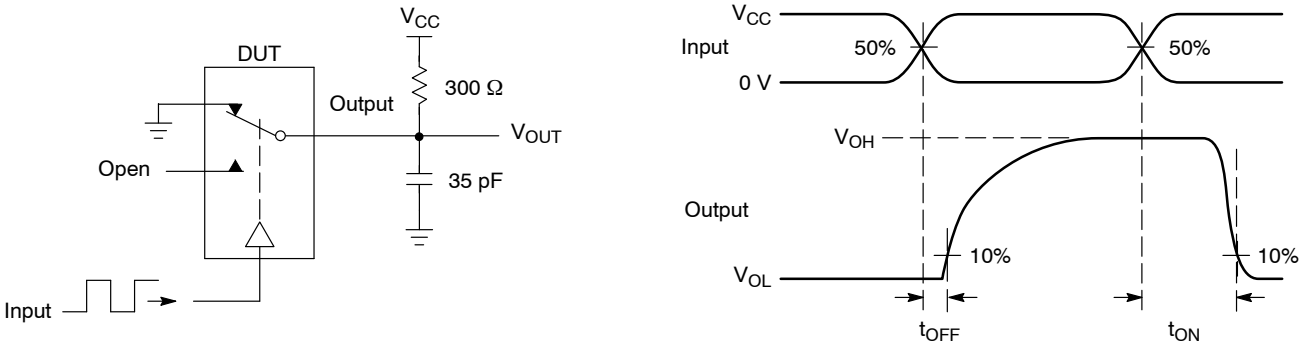

Figure 6. t_{ON}/t_{OFF}

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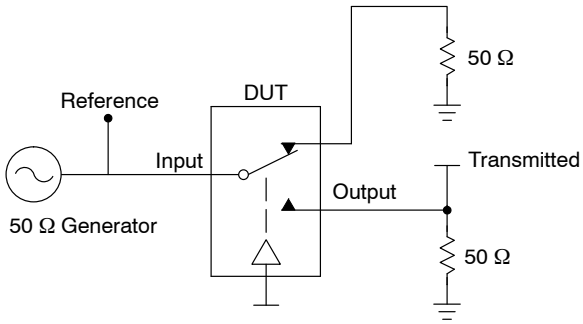

Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.

V_{ISO} = Off Channel Isolation = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz

V_{ONL} = On Channel Loss = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

Figure 7. V_{ISO} / V_{ONL} / BW

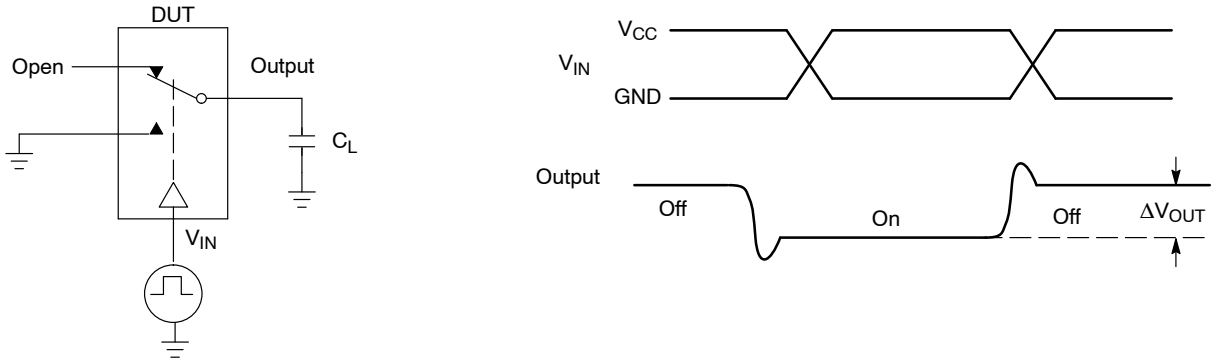

Figure 8. Charge Injection

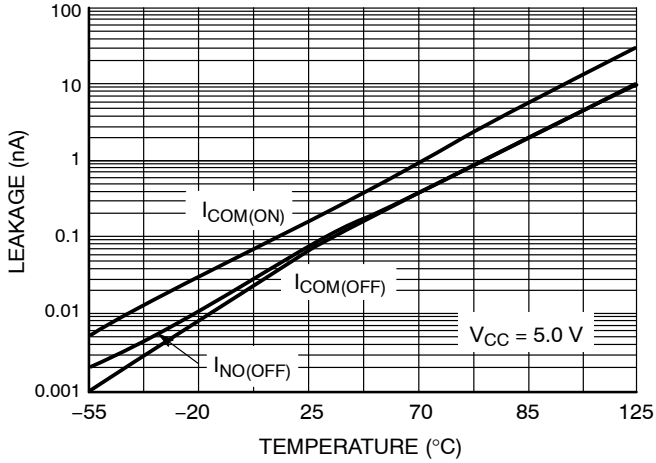

Figure 9. Switch Leakage vs. Temperature

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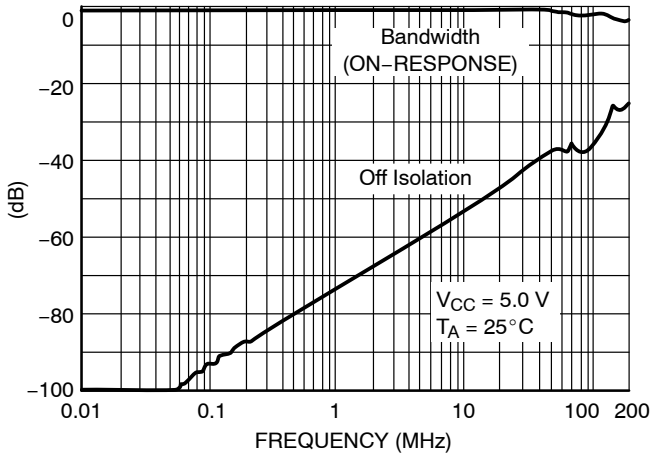

Figure 10. Bandwidth and Off−Channel Isolation

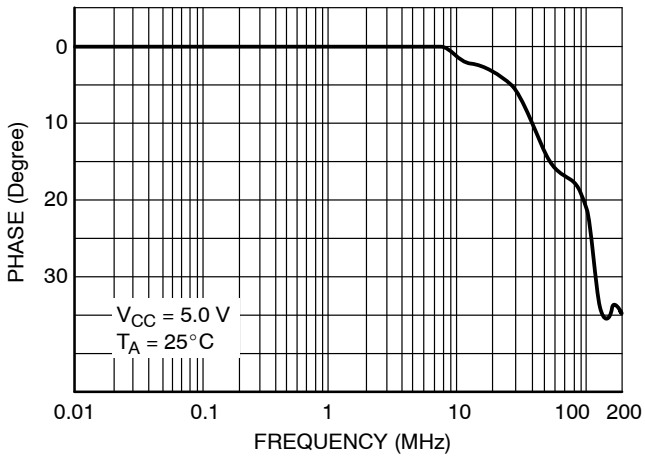

Figure 11. Phase vs. Frequency

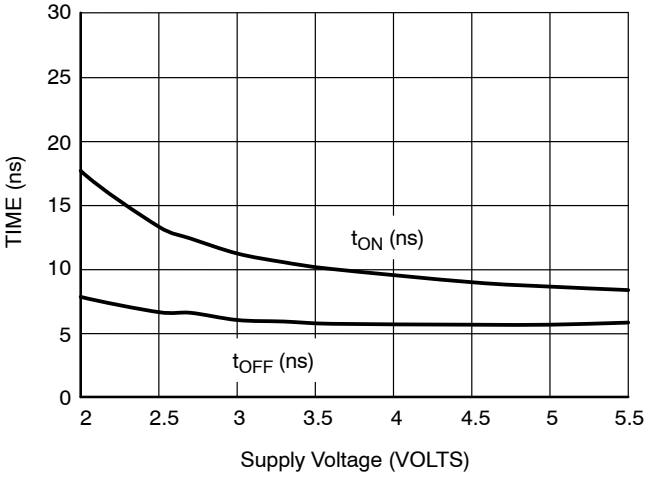

Figure 12. t_{ON} and t_{OFF} vs. V_{CC} at 25 °C

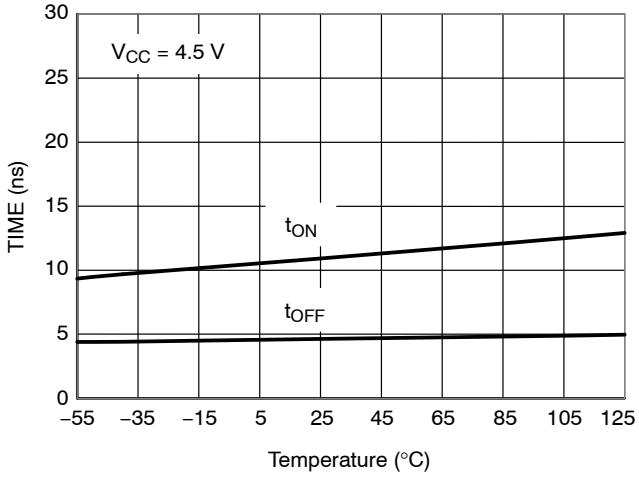

Figure 13. t_{ON} and t_{OFF} vs. Temperature

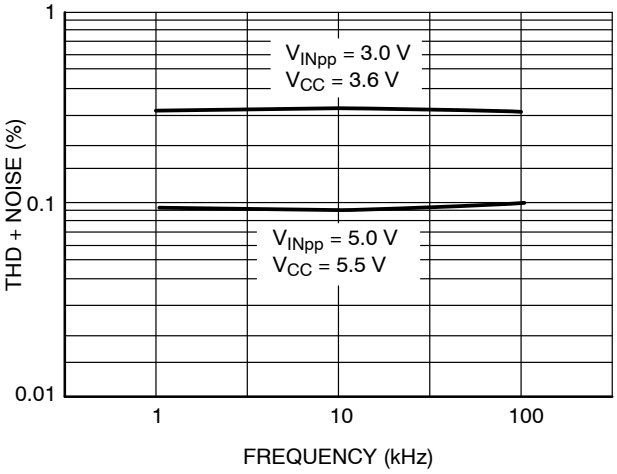

Figure 14. Bandwidth and Off-Channel Isolation

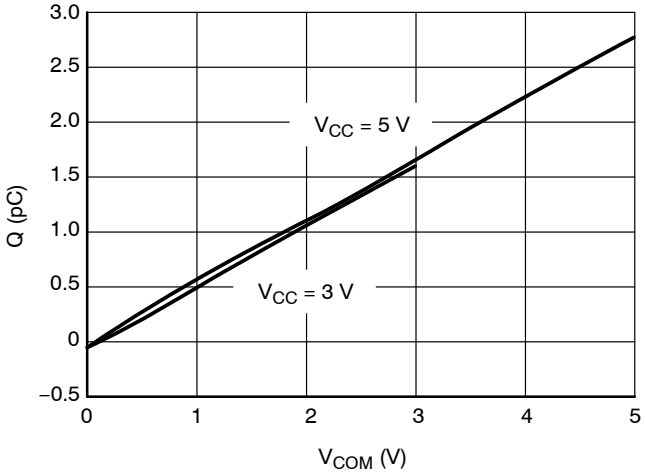

Figure 15. Charge Injection vs. COM Voltage

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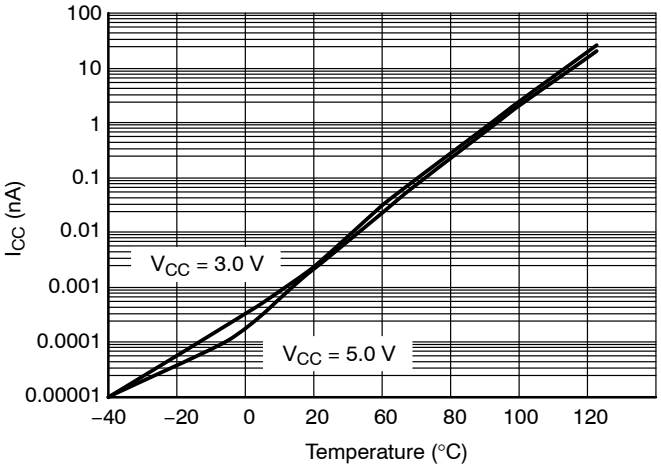

Figure 16. I_{CC} vs. Temp, V_{CC} = 3 V & 5 V

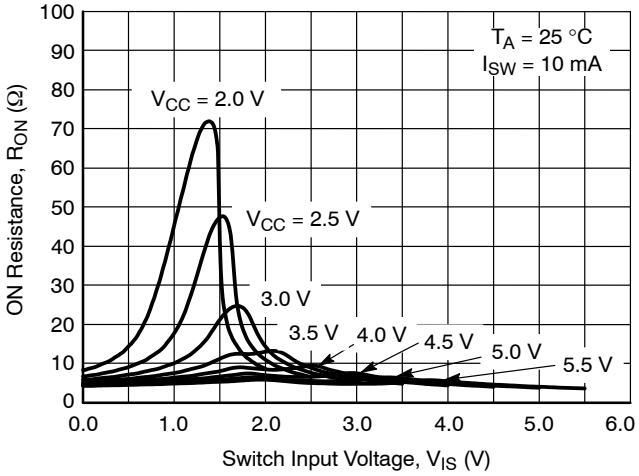

Figure 17. R_{ON} vs. V_{IS}, T_A = 25°C

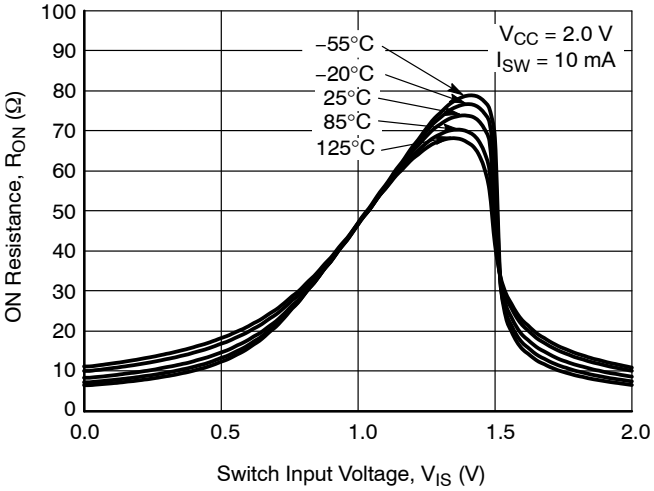

Figure 18. R_{ON} vs V_{IS}, V_{CC} = 2.0 V

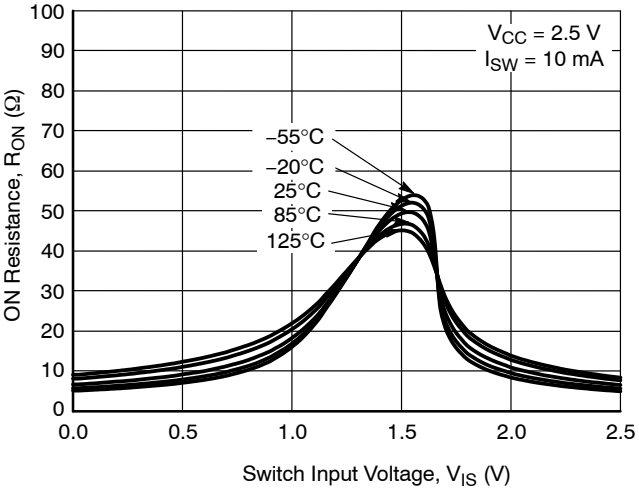

Figure 19. R_{ON} vs. V_{IS}, V_{CC} = 2.5 V

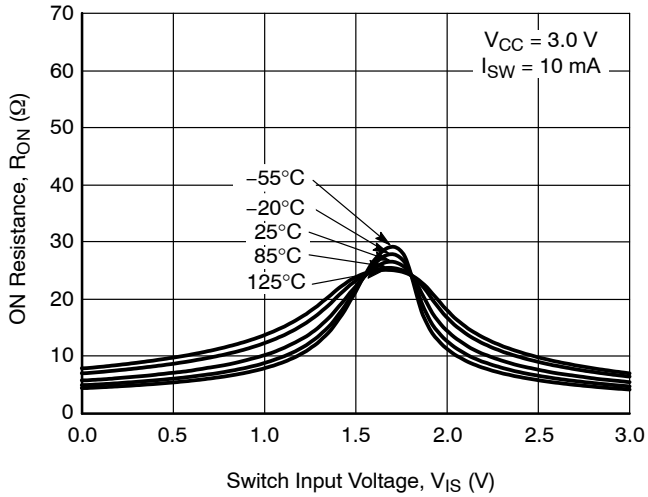

Figure 20. R_{ON} vs. V_{IS}, V_{CC} = 3.0 V

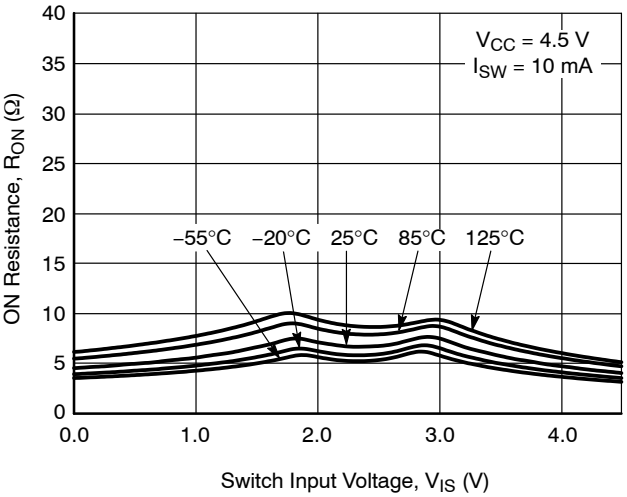

Figure 21. R_{ON} vs. V_{IS}, V_{CC} = 4.5 V

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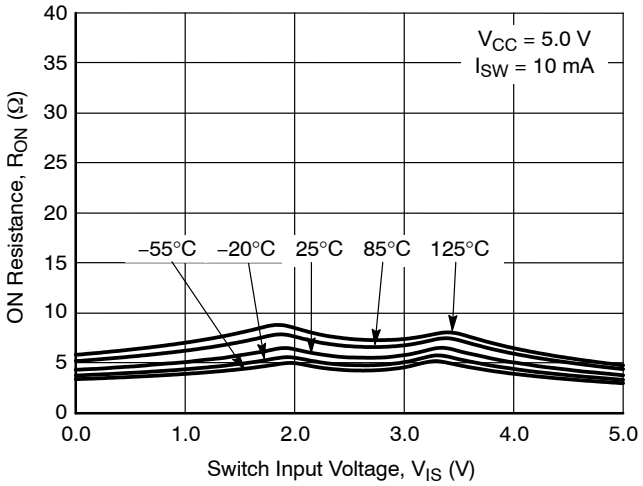


Figure 22. R_{ON} vs. V_{IS}, V_{CC} = 5.0 V

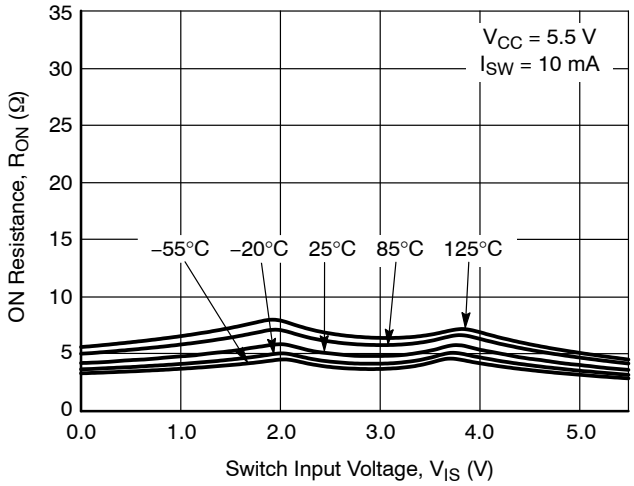


Figure 23. R_{ON} vs. V_{IS}, V_{CC} = 5.5 V

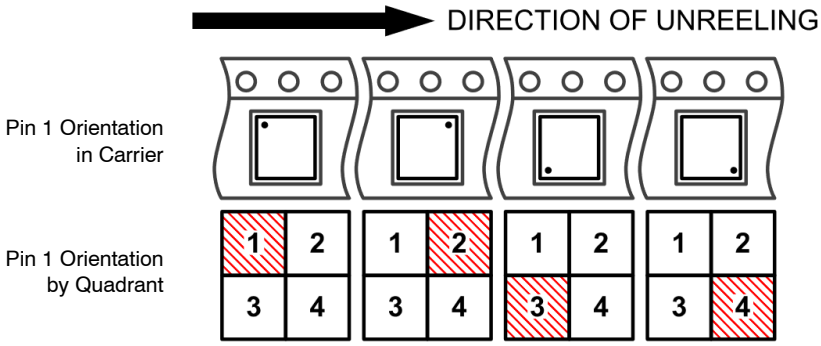
ORDERING INFORMATION

Device	Package	Marking	Pin 1 Quadrant	Shipping†
NL5S4599DFT2G	SC−88	A2	3	3000 / Tape & Reel
NL5S4599DFT2G−Q*	SC−88	A2	3	3000 / Tape & Reel
NL5S4599DBVT1G	SC−74	A2	3	3000 / Tape & Reel
NL5S4599DBVT1G−Q*	SC−74	A2	3	3000 / Tape & Reel
NL5ST4599DFT2G	SC−88	A3	3	3000 / Tape & Reel
NL5ST4599DFT2G−Q*	SC−88	A3	3	3000 / Tape & Reel
NL5ST4599DBVT1G	SC−74	A3	3	3000 / Tape & Reel
NL5ST4599DBVT1G−Q*	SC−74	A3	3	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel



REVISION HISTORY

Revision	Description of Changes	Date
P0	Initial Preliminary Document release.	9/12/2025
P1	Corrected parameter and conditions text in DC table on page 3.	12/15/2025
0	Initial Document release.	2/10/2026

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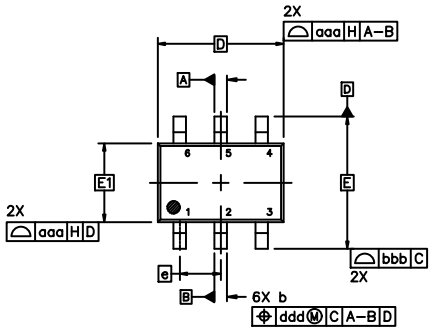
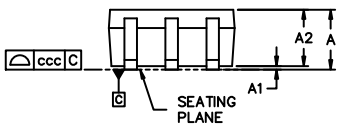
PACKAGE DIMENSIONS

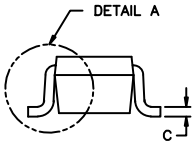
SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z



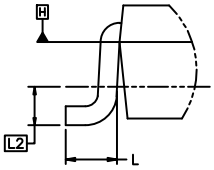
TOP VIEW



SIDE VIEW



END VIEW

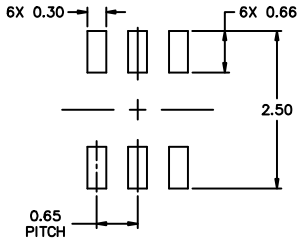


DETAIL A
SCALE 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.00	---	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00 BSC		
E	2.10 BSC		
E1	1.25 BSC		
e	0.65 BSC		
L	0.26	0.36	0.46
L2	0.15 BSC		
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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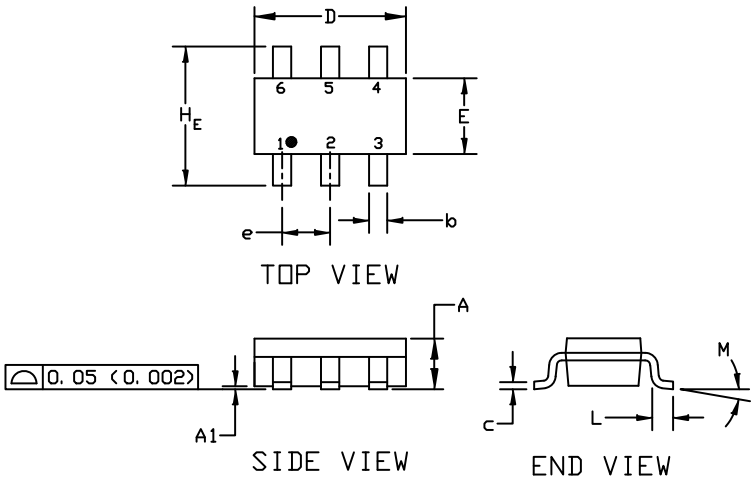
Your Opinion Matters

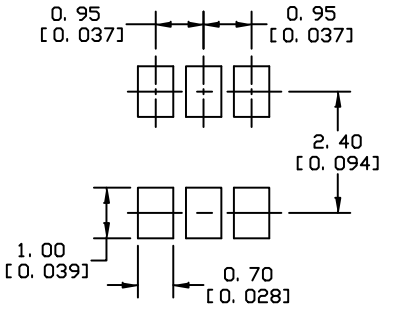
PACKAGE DIMENSIONS

SC−74
CASE 318F
ISSUE P



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994
2. CONTROLLING DIMENSION: INCHES
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
H_E	2.50	2.75	3.00	0.099	0.108	0.118
L	0.20	0.40	0.60	0.008	0.016	0.024
M	0°	---	10°	0°	---	10°



* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOLDERING FOOTPRINT

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