NLA16T245

16-Bit (Dual 8-Bit) Configurable Dual-Supply Translating Transceiver with 3-State Outputs

The NLA16T245 is a 16−bit (dual 8−bit) configurable dual−supply translating bidirectional transceiver with 3−state outputs. The A− and B−ports are designed to track two different power supply rails, V_{CCA} and V_{CCB} respectively. Both supply rails are configurable from 0.9 V to 4.5 V allowing universal bidirectional voltage translation between the A− and B−ports.

The Direction inputs, 1DIR and 2DIR, determine the direction of data flow. 1DIR and 2DIR are independent of each other. When 1DIR or 2DIR is High, data flows from 1An to 1Bn or 2An to 2Bn respectively. When 1DIR or 2DIR is Low, data flows from 1Bn to 1An or 2Bn to 2An respectively. The Output Enable inputs, and , when High, disables both A− and B−ports by putting them in 3−state. The 1DIR, 2DIR, and signals are all designed to track V_{CCA}.

Features

- Wide V_{CCA} and V_{CCB} Operating Range: 0.9 V to 4.5 V
- Output Noise Reduction through Dynamic Output Impedance Change
- Drive Capability: ±12 mA @ 3.0 V V_{CC}
- Input/Output Pins OVT to 5.5 V
- Control Inputs Track V_{CCA}
- Non−preferential V_{CC} Sequencing
- Outputs at 3−State until Active V_{CC} is reached
- Power−Off Protection
- Outputs Switch to 3−State with either V_{CC} at GND
- Pb−Free Packaging: TSSOP−48
- This is a Pb−Free Device

Typical Applications

- Mobile Phones, PDAs, Other Portable Devices

Important Information

- ESD Protection for All Pins:
  Human Body Model (HBM) > 2000 V
  Machine Model (MM) > 200 V

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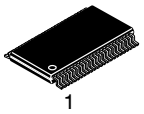


TSSOP−48
DT SUFFIX
CASE1201

MARKING DIAGRAM

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NLA16T245DTR2G	TSSOP−48 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

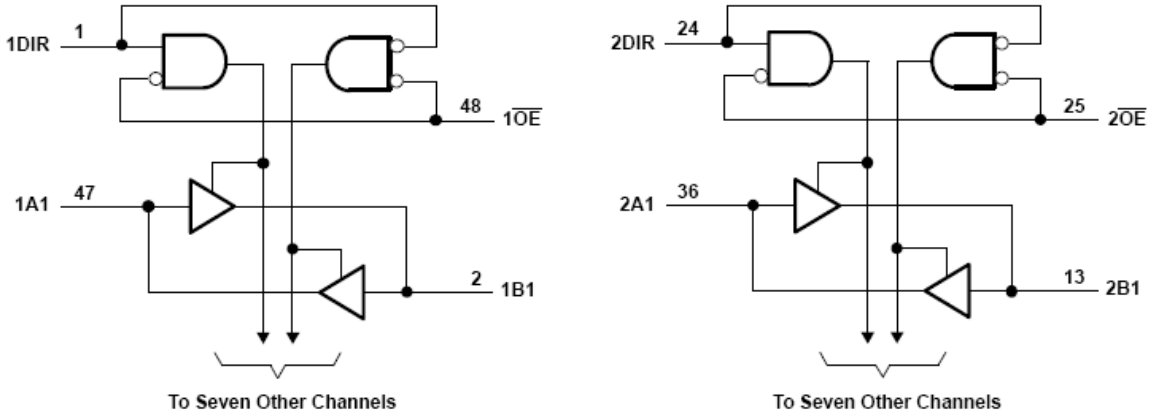


Figure 1. Logic Diagram

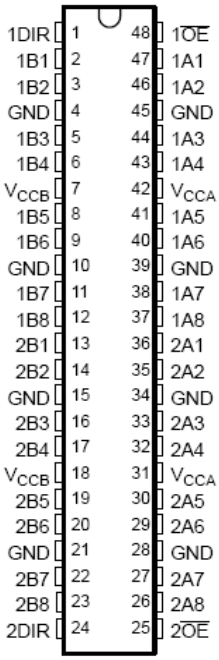


Figure 2. Pin Assignment

Pin Names

Pins	Description
V_{CCA}	A−Port DC Power Supply
V_{CCB}	B−Port DC Power Supply
GND	Ground
$\overline{1OE}$, $\overline{2OE}$	Output Enable Pins
1DIR, 2DIR	Direction Select Pins
$1A_n$, $2A_n$	A−Port I/O
$1B_n$, $2B_n$	B−Port I/O

Function table

$\overline{nOE}$	nDIR	Operating Mode
L	L	nB to nA
L	H	nA to nB
H	X	nA and nB Ports at Hi−Z

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V_{CCA}, V_{CCB}	DC Supply Voltage	−0.5 to +5.5		V
V_I	Input Voltage $\overline{nOE}$, nDIR, nA	−0.5 to +4.6	V_{CCA} = 0 V	V
		−0.5 to +5.5	$V_{CCA} \geq$ 0.9 V	
	nB	−0.5 to +4.6	V_{CCB} = 0 V	
		−0.5 to +5.5	$V_{CCB} \geq$ 0.9 V	
V_O	Output Voltage (Power−Off Mode) nA, nB	−0.5 to +5.5	V_{CCA} or V_{CCB} = 0	V
	(3−State Mode) nA, nB	−0.5 to +5.5	V_{CCA}, $V_{CCB} \geq$ 0.9 V	
	(Active Mode − High or Low State) nA	−0.5 to V_{CCA} + 0.5	V_{CCA}, $V_{CCB} \geq$ 0.9 V	
	(Active Mode − High or Low State) nB	−0.5 to V_{CCB} + 0.5		
I_{IK}	DC Input Diode Current $\overline{nOE}$, nDIR	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +125		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CCA}, V_{CCB}	Positive DC Supply Voltage	0.9	4.5	V
V_I	Input Voltage	GND	4.5	V
V_O	Output Voltage (Power Down) nA, nB	GND	4.5	V
	(3−State Mode) nA, nB	GND	4.5	
	(Active Mode − High or Low State) nA	GND	V_{CCA}	
	(Active Mode − High or Low State) nB	GND	V_{CCB}	
T_A	Operating Temperature Range	−55	+115	°C
$\Delta t/\Delta V$	Input Transition Rise or Rate V_I, V_{IO} from 30% to 70% of V_{CC}; V_{CC} =3.3 V ± 0.3 V	0	10	nS

DC ELECTRICAL CHARACTERISTICS (INPUT)

Symbol	Parameter	Test Conditions	V_{CCI} (Note 1) (V)	V_{CCO} (Note 2) (V)	−55°C to +115°C		Unit
					Min	Max	
V_{IH}	Input HIGH Voltage, Data Inputs		3.6 – 4.5	0.9 – 4.5	2.2		V
			2.7 – 3.6		2.0		
			1.95 – 2.7		1.7		
			1.2 – 1.95		0.65 * V_{CCI}		
			0.9 – 1.2		0.9 * V_{CCI}		
V_{IL}	Input LOW Voltage, Data Inputs		3.6 – 4.5	0.9 – 4.5		0.8	V
			2.7 – 3.6			0.8	
			1.95 – 2.7			0.7	
			1.2 – 1.95			0.35 * V_{CCI}	
			0.9 – 1.2			0.1 * V_{CCI}	
V_{IH}	Input HIGH Voltage, Control Inputs	Referenced to V_{CCA}	3.6 – 4.5		2.2		V
			2.7 – 3.6		2.0		
			1.95 – 2.7		1.6		
			1.2 – 1.95		0.65 * V_{CCA}		
			0.9 – 1.2		0.9 * V_{CCA}		
V_{IL}	Input LOW Voltage, Control Inputs	Referenced to V_{CCA}	3.6 – 4.5			0.8	V
			2.7 – 3.6			0.8	
			1.95 – 2.7			0.7	
			1.2 – 1.95			0.35 * V_{CCA}	
			0.9 – 1.2			0.1 * V_{CCA}	

NOTE: Connect ground before applying supply voltage V_{CCA} or V_{CCB}. This device is designed with the feature that the power−up sequence of V_{CCA} and V_{CCB} will not damage the IC.

1. V_{CCI} is the V_{CC} associated with the input port.
2. V_{CCO} is the V_{CC} associated with the output port.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		V_{CCA} (V)	V_{CCB} (V)	−55°C to +115°C		Unit
						Min	Max	
V_{OH}	Output HIGH Voltage	I_{OH} = −100 μA; V_I = V_{IH}		0.9 – 4.5	0.9 – 4.5	V_{CCO} – 0.2		V
		I_{OH} = −0.5 mA; V_I = V_{IH}		0.9	0.9	0.75 * V_{CCO}		
		I_{OH} = −2 mA; V_I = V_{IH}		1.4	1.4	1.05		
		I_{OH} = −4 mA; V_I = V_{IH}		1.65	1.65	1.2		
		I_{OH} = −8 mA; V_I = V_{IH}		2.3	2.3	1.75		
		I_{OH} = −12 mA; V_I = V_{IH}		3.0	3.0	2.3		
		I_{OH} = −12 mA; V_I = V_{IH}		4.5	4.5	4.0		
V_{OL}	Output LOW Voltage	I_{OL} = 100 μA; V_I = V_{IL}		0.9 – 4.5	0.9 – 4.5		0.2	V
		I_{OL} = 0.5 mA; V_I = V_{IL}		0.9	0.9		0.25 * V_{CCO}	
		I_{OL} = 2 mA; V_I = V_{IL}		1.4	1.4		0.35	
		I_{OL} = 4 mA; V_I = V_{IL}		1.65	1.65		0.45	
		I_{OL} = 8 mA; V_I = V_{IL}		2.3	2.3		0.55	
		I_{OL} = 12 mA; V_I = V_{IL}		3.0	3.0		0.7	
		I_{OL} = 12 mA; V_I = V_{IL}		4.5	4.5		0.75	
I_I	Input Leakage Current	V_I = V_{CCA} or GND	$\overline{nOE}$	0.9 – 4.5	0.9 – 4.5		±2.5	μA
I_{OFF}	Power−Off Leakage Current	V_I or V_O = 0 to 4.5 V,	nA	0	0 – 4.5		±10.0	μA
			nB	0 – 4.5	0		±10.0	
I_{OZ}(3)	3−State Output Leakage Current	V_I = V_{IH} or V_{IL}, V_O = V_{CCO} or GND, $\overline{nOE}$ = V_{IH}	nA, nB	3.6	3.6		±12.5	μA
		V_I = V_{IH} or V_{IL}, V_O = V_{CCO} or GND, $\overline{nOE}$ = don't care	nA	3.6	0		±12.5	
			nB	0	3.6		±12.5	
I_{CCA}	Quiescent Supply Current	V_I = V_{CCI} or GND; I_O = 0		0.9	0.9		20	μA
				1.6	1.6		20	
				1.95	1.95		20	
				2.7	2.7		30	
				0	3.6		−40	
				3.6	0		40	
				3.6	3.6		40	
				0	4.5		−40	
				4.5	0		40	
				4.5	4.5		40	
I_{CCB}	Quiescent Supply Current	V_I = V_{CCI} or GND; I_O = 0		0.9	0.9		20	μA
				1.6	1.6		20	
				1.95	1.95		20	
				2.7	2.7		30	
				0	3.6		−40	
				3.6	0		40	
				3.6	3.6		40	
				0	4.5		−40	
				4.5	0		40	
				4.5	4.5		40	

NOTE: Connect ground before applying supply voltage V_{CCA} or V_{CCB}. This device is designed with the feature that the power−up sequence of V_{CCA} and V_{CCB} will not damage the IC.

3. V_{CCI} is the V_{CC} associated with the input port.
4. V_{CCO} is the V_{CC} associated with the output port.
5. For I/O ports, the parameter IOZ includes the input leakage current.

AC ELECTRICAL CHARACTERISTICS – See Figure 3

Symbol	Parameter	From	To	–55°C to +115°C										Unit
				V_{CCB} (V)										
				4.0 – 4.5		3.0 – 3.6		2.3 – 2.7		1.65 – 1.95		1.4 – 1.6		
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V_{CCA} = 4.0 – 4.5 V														
t_{PD}	Propagation Delay	A	B	0.5	3.2	0.3	3.2	0.7	3.5	0.8	4.2	0.4	4	ns
		B	A	0.3	4.5	0.5	5.8	0.5	6	0.7	6.3	1.2	6.8	
t_{EN}	Output Enable		A	0.2	9.5	1.0	7.7	0.9	8	1.0	9	0.8	8.5	ns
			B	0.8	4.5	1.2	4.8	1.4	6.7	1.8	7	1.6	7.5	
t_{DIS}	Output Disable		A	0.8	5.6	1.0	5.6	1.1	5.6	1.1	5.7	1.2	5.7	ns
			B	1.2	6	1.2	6.1	1.1	6	2.6	9.2	2.3	9.6	
t_{OSK}	Output to Output Skew				0.15		0.15		0.15		0.15		0.15	ns
V_{CCA} = 3.0 – 3.6 V														
t_{PD}	Propagation Delay	A	B	0.5	3.5	0.5	3.1	0.5	3.7	0.7	5.4	0.5	5.9	ns
		B	A	0.6	5.5	0.4	5.5	0.7	5.5	0.7	5.8	1.0	6.5	
t_{EN}	Output Enable		A	0.8	10	1.0	8	1.3	8.0	1.4	9.2	1.3	8.7	ns
			B	1.0	5	1.9	4.9	2.0	5.4	1.9	6.7	0.8	7.4	
t_{DIS}	Output Disable		A	1.5	6	1.5	5.4	1.2	5.8	1.6	5.2	1.4	5.4	ns
			B	1.7	6.4	1.5	6.1	1.1	5.8	1.7	8.5	1.2	8.8	
t_{OSK}	Output to Output Skew				0.15		0.15		0.15		0.15		0.15	ns
V_{CCA} = 2.3 – 2.7 V														
t_{PD}	Propagation Delay	A	B	0.7	4	0.5	3.4	0.4	4.0	0.7	5.6	0.2	6.0	ns
		B	A	0.6	4.7	0.5	5.3	0.6	5.0	1.2	5.8	1.0	6.1	
t_{EN}	Output Enable		A	0.9	12	2.0	9.0	1.7	7.0	1.6	7.9	1.6	8.0	ns
			B	0.7	5.7	1.5	5.3	2.2	6.1	2.2	7.0	1.2	7.8	
t_{DIS}	Output Disable		A	2	6.8	1.6	6.2	0.7	6.5	1.5	6.0	2.0	6.5	ns
			B	1.2	6	1.4	6.0	1.0	5.6	1.7	8.2	0.9	9.0	
t_{OSK}	Output to Output Skew				0.15		0.15		0.15		0.15		0.15	ns
V_{CCA} = 1.65 – 1.95 V														
t_{PD}	Propagation Delay	A	B	1.1	4.2	0.8	4.3	0.9	4.7	1.0	6.0	0.6	6.4	ns
		B	A	1.2	4.5	1.3	5.5	0.9	5.8	1.8	6.7	1.4	6.5	
t_{EN}	Output Enable		A	2.2	9.7	2.0	8.5	2.2	8.9	2.1	9.5	2.5	10.0	ns
			B	0.5	8.2	2.7	8.1	2.7	8.1	2.7	8.3	1.8	9.0	
t_{DIS}	Output Disable		A	2	9.3	1.8	8.0	1.5	8.0	2.5	8.8	2.1	8.6	ns
			B	1.8	6.2	2.0	6.1	1.0	5.5	2.5	8.3	2.1	8.8	
t_{OSK}	Output to Output Skew				0.15		0.15		0.15		0.15		0.15	ns
V_{CCA} = 1.4 – 1.6 V														
t_{PD}	Propagation Delay	A	B	1.2	5	1.3	5.8	1.0	5.5	1.5	6.3	1.7	6.7	ns
		B	A	1	5.5	0.7	7.3	0.9	7.6	1.5	7.4	1.8	6.8	

AC ELECTRICAL CHARACTERISTICS – See Figure 3

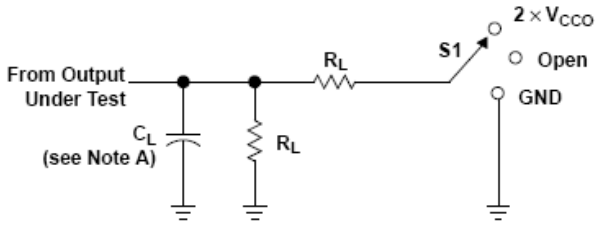
Symbol	Parameter	From	To	−55°C to +115°C										Unit
				V_{CCB} (V)										
				4.0 – 4.5		3.0 – 3.6		2.3 – 2.7		1.65 – 1.95		1.4 – 1.6		
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V_{CCA} = 1.4 – 1.6 V														
t_{EN}	Output Enable		A	3	11.5	2.1	10.5	2.3	10.5	2.7	12.0	2.6	12.8	ns
			B	2	10	3.2	10.7	3.2	10.8	3.2	10.2	2.7	10.6	
t_{DIS}	Output Disable		A	3	12	2.0	10.5	1.7	10.5	2.5	9.5	2.1	9.7	ns
			B	1.2	6	1.3	6.4	1.1	6.5	2.5	8.5	2.1	8.8	
t_{OSK}	Output to Output Skew				0.15		0.15		0.15		0.15		0.15	ns

CAPACITANCES

Symbol	Parameter	Output State	Test Conditions	Typ (Note 6)	Unit
C_{IN}	Control Pin Input Capacitance		V_I = 3.3 V or GND	3.5	pF
$C_{I/O}$	I/O Pin Input Capacitance		V_O = 3.3 V or GND	5.0	pF
C_{PDA} (Note 7)	Power Dissipation Capacitance per	Enabled	C_L = 0 pF, f = 10 MHz	14.0	pF
	Transceiver, A−Port Input, B−Port Output	Disabled		7.0	
	Power Dissipation Capacitance per	Enabled		20.0	
	Transceiver, B−Port Input, A−Port Output	Disabled		7.0	
C_{PDB} (Note 7)	Power Dissipation Capacitance per	Enabled	C_L = 0 pF, f = 10 MHz	14.0	pF
	Transceiver, A−Port Input, B−Port Output	Disabled		7.0	
	Power Dissipation Capacitance per	Enabled		20.0	
	Transceiver, B−Port Input, A−Port Output	Disabled		7.0	

6. Typical values are at V_{CCA} = V_{CCB} = 3.3 V, T_A = +25°C.
7. C_{PD} is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from: $I_{CC}(operating) \approx C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$ where $I_{CC} = I_{CCA} + I_{CCB}$ and N_{SW} = total number of outputs switching.

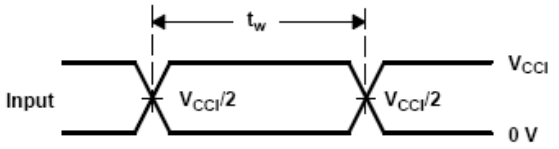
PARAMETER MEASUREMENT INFORMATION



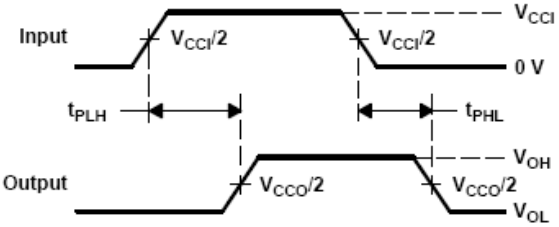
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

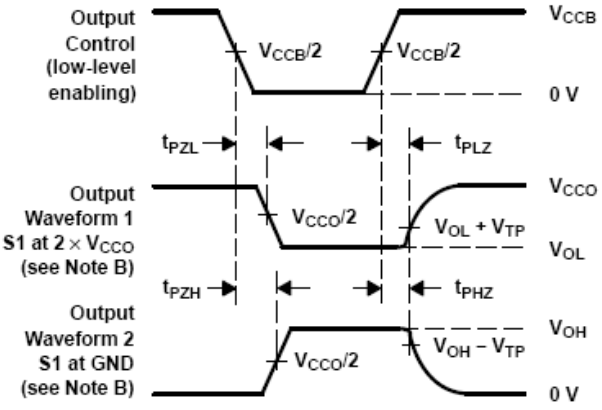
V_{CCO}	C_L	R_L	V_{TP}
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	30 pF	500 Ω	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



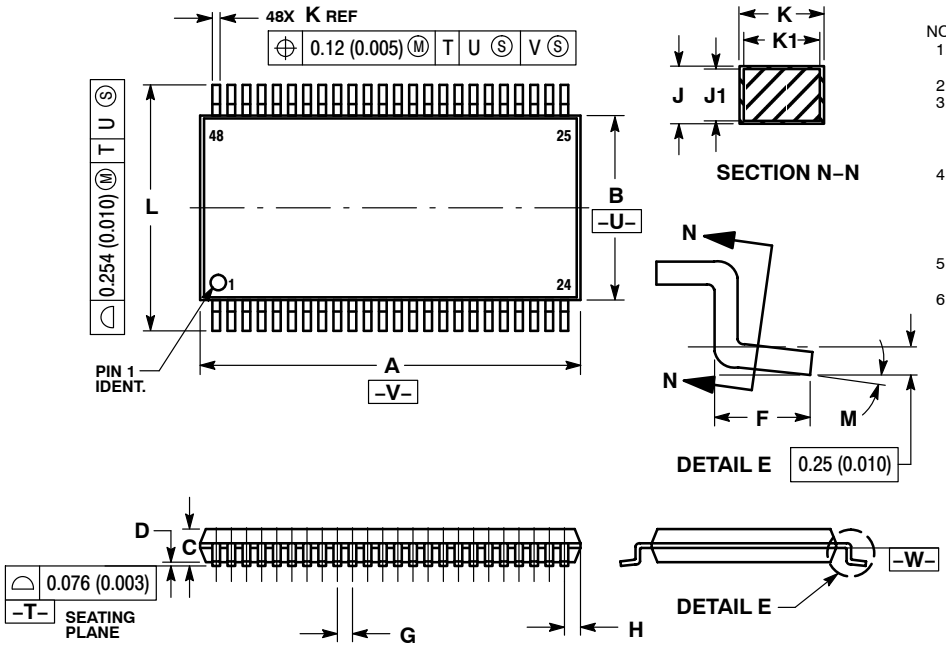
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

Figure 3. Load Circuit and Voltage Waveforms

PACKAGE DIMENSIONS

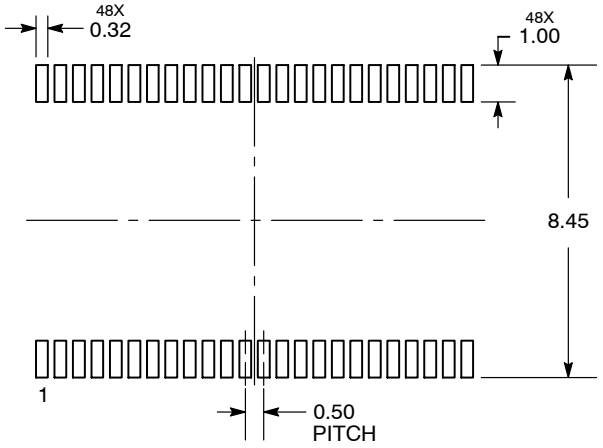
TSSOP−48
CASE 1201
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	−−−	1.10	−−−	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	−−−	0.015	−−−
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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