

# NLAS4051S

## Analog Multiplexer/ Demultiplexer

### TTL Compatible, Single-Pole, 8-Position Plus Common Off

The NLAS4051S is an improved version of the MC14051 and MC74HC4051 fabricated in sub-micron Silicon Gate CMOS technology for lower  $R_{DS(on)}$  resistance and improved linearity with low current. This device may be operated either with a single supply or dual supply up to  $\pm 3.0$  V to pass a 6.0 V<sub>PP</sub> signal without coupling capacitors.

When operating in single supply mode, it is only necessary to tie V<sub>EE</sub>, pin 7 to ground. For dual supply operation, V<sub>EE</sub> is tied to a negative voltage, not to exceed maximum ratings.

#### Features

- Improved  $R_{DS(on)}$  Specifications
- Pin for Pin Replacement for MAX4051 and MAX4051A
  - ◆ One Half the Resistance Operating at 5.0 V
- Single or Dual Supply Operation
  - ◆ Single 2.5–5.0 V Operation, or Dual  $\pm 3.0$  V Operation
  - ◆ With V<sub>CC</sub> of 3.0 to 3.3 V, Device Can Interface with 1.8 V Logic, No Translators Needed
  - ◆ Address and Inhibit Logic are Over-Voltage Tolerant and May Be Driven Up +6.0 V Regardless of V<sub>CC</sub>
- Improved Linearity Over Standard HC4051 Devices
- Space Saving TSSOP Package
- This is a Pb-Free Device

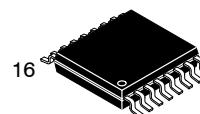


**Figure 1. Pin Connection**  
(Top View)



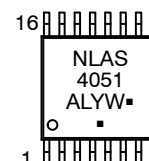
**ON Semiconductor®**

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**TSSOP-16**  
**DT SUFFIX**  
**CASE 948F**

#### MARKING DIAGRAM



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

Device	Package	Shipping†
NLAS4051SDTR2G	TSSOP-16 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## TRUTH TABLE

Inhibit	Address			ON SWITCHES*
	C	B	A	
1	X don't care	X don't care	X don't care	All switches open
0	0	0	0	COM-NO <sub>0</sub>
0	0	0	1	COM-NO <sub>1</sub>
0	0	1	0	COM-NO <sub>2</sub>
0	0	1	1	COM-NO <sub>3</sub>
0	1	0	0	COM-NO <sub>4</sub>
0	1	0	1	COM-NO <sub>5</sub>
0	1	1	0	COM-NO <sub>6</sub>
0	1	1	1	COM-NO <sub>7</sub>

\*NO and COM pins are identical and interchangeable. Either may be considered an input or output; signals pass equally well in either direction.

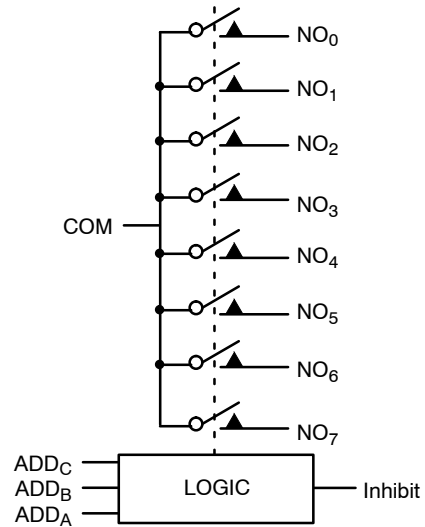


Figure 2. Logic Diagram

## MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Negative DC Supply Voltage (Referenced to GND)	$V_{EE}$	-7.0 to +0.5	V
Positive DC Supply Voltage (Note 1) (Referenced to GND) (Referenced to $V_{EE}$ )	$V_{CC}$	-0.5 to +7.0 -0.5 to +7.0	V
Analog Input Voltage	$V_{IS}$	$V_{EE} - 0.5$ to $V_{CC} + 0.5$	V
Digital Input Voltage (Referenced to GND)	$V_{IN}$	-0.5 to 7.0	V
DC Current, Into or Out of Any Pin	I	± 50	mA
Storage Temperature Range	$T_{STG}$	-65 to +150	°C
Lead Temperature, 1 mm from Case for 10 Seconds	$T_L$	260	°C
Junction Temperature under Bias	$T_J$	+150	°C
Thermal Resistance	$\theta_{JA}$	164	°C/W
Power Dissipation in Still Air	$P_D$	450	mW
Moisture Sensitivity	MSL	Level 1	
Flammability Rating Oxygen Index: 30% - 35%	$F_R$	UL 94 V-0 @ 0.125 in	
ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	$V_{ESD}$	> 2000 > 200 > 1000	V
Latchup Performance Above $V_{CC}$ and Below GND at 125°C (Note 5)	$I_{LATCHUP}$	± 300	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The absolute value of  $V_{CC} \pm |V_{EE}| \leq 7.0$ .
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

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## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Negative DC Supply Voltage (Referenced to GND)	$V_{EE}$	-5.5	GND	V
Positive DC Supply Voltage (Referenced to GND) (Referenced to $V_{EE}$ )	$V_{CC}$	2.5 2.5	5.5 6.6	V
Analog Input Voltage	$V_{IS}$	$V_{EE}$	$V_{CC}$	V
Digital Input Voltage (Note 6) (Referenced to GND)	$V_{IN}$	0	5.5	V
Operating Temperature Range, All Package Types	$T_A$	-55	125	°C
Input Rise/Fall Time (Channel Select or Enable Inputs)	$t_r, t_f$	0 0	100 20	ns/V

6. Unused digital inputs may not be left open. All digital inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

## DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Parameter	Condition	Symbol	$V_{CC}$ V	Guaranteed Limit			Unit
				-55 to 25°C	≤ 85°C	≤ 125°C	
Minimum High-Level Input Voltage, Address and Inhibit Inputs		$V_{IH}$	2.5	1.75	1.75	1.75	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			5.5	3.85	3.85	3.85	
Maximum Low-Level Input Voltage, Address and Inhibit Inputs		$V_{IL}$	2.5	.45	.45	.45	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			5.5	1.65	1.65	1.65	
Maximum Input Leakage Current, Address or Inhibit Inputs	$V_{IN} = 6.0$ or GND	$I_{IN}$	0 V to 6.0 V	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Current (per Package)	Address, Inhibit and $V_{IS} = V_{CC}$ or GND	$I_{CC}$	6.0	4.0	40	80	µA

## DC ELECTRICAL CHARACTERISTICS – Analog Section

Parameter	Test Conditions	Symbol	$V_{CC}$ V	$V_{EE}$ V	Guaranteed Limit			Unit
					-55 to 25°C	≤ 85°C	≤ 125°C	
Maximum "ON" Resistance (Note 7)	$V_{IN} = V_{IL}$ or $V_{IH}$ $V_{IS} = (V_{EE} \text{ to } V_{CC})$ $ I_S  = 10$ mA (Figures 4 thru 9)	$R_{ON}$	3.0	0	86	108	120	Ω
			4.5	0	37	46	55	
			3.0	-3.0	26	33	37	
Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{IN} = V_{IL}$ or $V_{IH}$ , $V_{IS} = 2.0$ V $V_{IS} = \frac{1}{2}(V_{CC} - V_{EE})$ , $V_{IS} = 3.0$ V $ I_S  = 10$ mA, $V_{IS} = 2.0$ V	$\Delta R_{ON}$	3.0	0	15	20	20	Ω
			4.5	0	13	18	18	
			3.0	-3.0	10	15	15	
ON Resistance Flatness	$ I_S  = 10$ mA $V_{COM} = 1, 2, 3.5$ V $V_{COM} = 2, 0, 2$ V	$R_{flat(ON)}$	4.5 3.0	3.0	4 2	4 2	5 3	Ω
Maximum Off-Channel Leakage Current	Switch Off $V_{IN} = V_{IL}$ or $V_{IH}$ $V_{IO} = V_{CC} - 1.0$ V or $V_{EE} + 1.0$ V (Figure 17)	$I_{NC(OFF)}$	6.0	0	0.1	5.0	100	nA
		$I_{NO(OFF)}$	3.0	-3.0	0.1	5.0	100	
Maximum On-Channel Leakage Current, Channel- to-Channel	Switch On $V_{IO} = V_{CC} - 1.0$ V or $V_{EE} + 1.0$ V (Figure 17)	$I_{COM(ON)}$	6.0 3.0	0 -3.0	0.1 0.1	5.0 5.0	100 100	nA

7. At supply voltage ( $V_{CC}$ ) approaching 2.5 V the analog switch on-resistance becomes extremely non-linear. Therefore, for low voltage operation it is recommended that these devices only be used to control digital signals.

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## AC CHARACTERISTICS (Input $t_r = t_f = 3$ ns)

Parameter	Test Conditions	Symbol	$V_{CC}$ V	$V_{EE}$ V	Guaranteed Limit				Unit
					-55 to 25°C		≤ 85°C	≤ 125°C	
					Min	Typ*			
Minimum Break-Before-Make Time	$V_{IN} = V_{IL}$ or $V_{IH}$ $V_{IS} = V_{CC}$ $R_L = 300 \Omega$ , $C_L = 35$ pF (Figure 19)	$t_{BBM}$	3.0	0.0	1.0	6.5	-	-	ns
			4.5	0.0	1.0	5.0	-	-	
			3.0	-3.0	1.0	3.5	-	-	

\*Typical Characteristics are at 25°C.

## AC CHARACTERISTICS ( $C_L = 35$ pF, Input $t_r = t_f = 3$ ns)

Parameter	Symbol	$V_{CC}$ V	$V_{EE}$ V	Guaranteed Limit						Unit	
				-55 to 25°C			≤ 85°C		≤ 125°C		
				Min	Typ	Max	Min	Max	Min		Max
Transition Time (Address Selection Time) (Figure 18)	$t_{TRANS}$	2.5	0		22	40		45		50	ns
		3.0	0		20	28		30		35	
		4.5	0		16	23		25		30	
		3.0	-3.0		16	23		25		28	
Turn-on Time (Figures 14, 15, 20, and 21) Inhibit to $N_O$ or $N_C$	$t_{ON}$	2.5	0		22	40		45		50	ns
		3.0	0		18	28		30		35	
		4.5	0		16	23		25		30	
		3.0	-3.0		16	23		25		28	
Turn-off Time (Figures 14, 15, 20, and 21) Inhibit to $N_O$ or $N_C$	$t_{OFF}$	2.5	0		22	40		45		50	ns
		3.0	0		18	28		30		35	
		4.5	0		16	23		25		30	
		3.0	-3.0		16	23		25		28	
<b>Typical @ 25°C, <math>V_{CC} = 5.0</math> V</b>											
Maximum Input Capacitance, Select Inputs	$C_{IN}$			8						pF	
Analog I/O	$C_{NO}$ or $C_{NC}$			10							
Common I/O	$C_{COM}$			10							
Feedthrough	$C_{(ON)}$			1.0							

## ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Parameter	Condition	Symbol	$V_{CC}$ V	$V_{EE}$ V	Typ	Unit
					25°C	
Maximum On-Channel Bandwidth or Minimum Frequency Response	$V_{IS} = \frac{1}{2}(V_{CC} - V_{EE})$ Source Amplitude = 0 dBm (Figures 10 and 22)	BW	3.0	0.0	80	MHz
			4.5	0.0	90	
			6.0	0.0	95	
			3.0	-3.0	95	
Off-Channel Feedthrough Isolation	$f = 100$ kHz; $V_{IS} = \frac{1}{2}(V_{CC} - V_{EE})$ Source = 0 dBm (Figures 12 and 22)	$V_{ISO}$	3.0	0.0	-93	dB
			4.5	0.0	-93	
			6.0	0.0	-93	
			3.0	-3.0	-93	
Maximum Feedthrough On Loss	$V_{IS} = \frac{1}{2}(V_{CC} - V_{EE})$ Source = 0 dBm (Figures 10 and 22)	$V_{ONL}$	3.0	0.0	-2	dB
			4.5	0.0	-2	
			6.0	0.0	-2	
			3.0	-3.0	-2	
Charge Injection	$V_{IN} = V_{CC}$ to $V_{EE}$ , $f_{IS} = 1$ kHz, $t_r = t_f = 3$ ns $R_{IS} = 0 \Omega$ , $C_L = 1000$ pF, $Q = C_L * \Delta V_{OUT}$ (Figures 16 and 23)	Q	5.0	0.0	9.0	pC
			3.0	-3.0	12	
Total Harmonic Distortion THD + Noise	$f_{IS} = 1$ MHz, $R_L = 10$ K $\Omega$ , $C_L = 50$ pF, $V_{IS} = 5.0$ V <sub>PP</sub> sine wave $V_{IS} = 6.0$ V <sub>PP</sub> sine wave (Figure 13)	THD	6.0	0.0	0.10	%
			3.0	-3.0	0.05	

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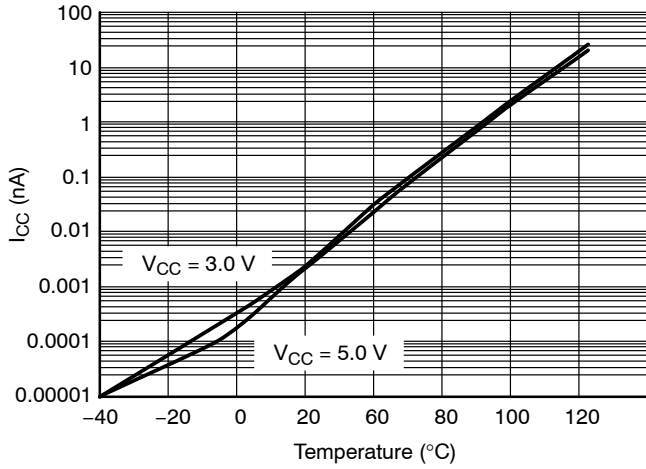


Figure 3.  $I_{CC}$  versus Temp,  $V_{CC} = 3\text{ V}$  and  $5\text{ V}$

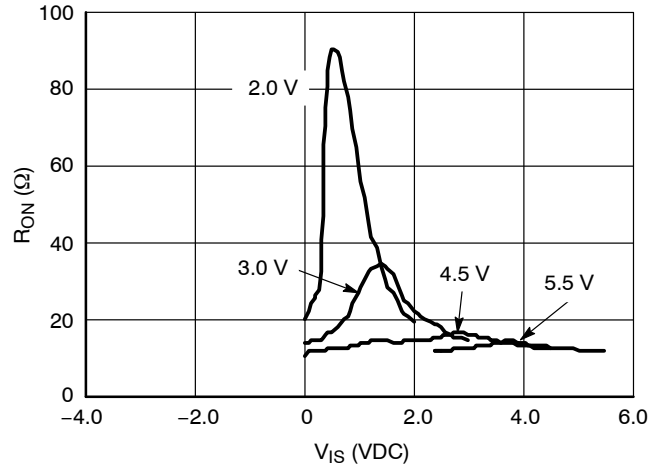


Figure 4.  $R_{ON}$  versus  $V_{CC}$ , Temp =  $25^{\circ}\text{C}$

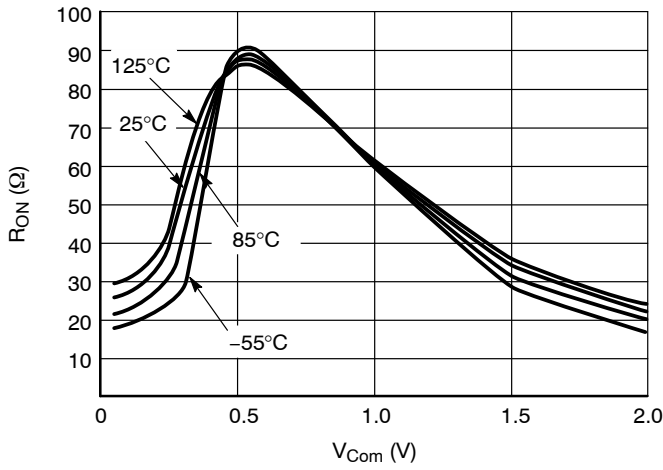


Figure 5. Typical On Resistance  
 $V_{CC} = 2.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$

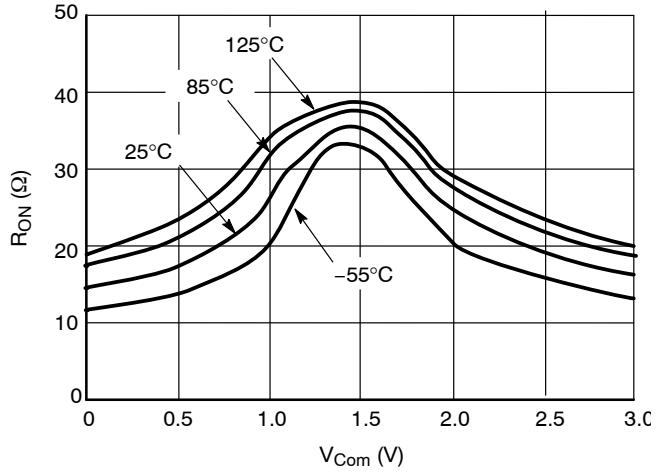


Figure 6. Typical On Resistance  
 $V_{CC} = 3.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$

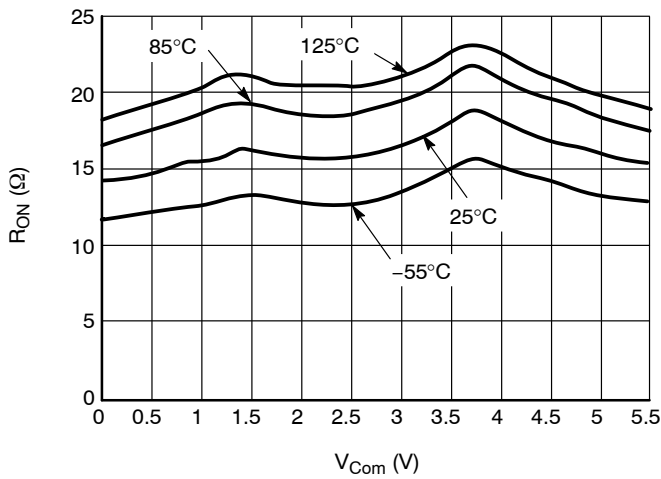


Figure 7. Typical On Resistance  
 $V_{CC} = 4.5\text{ V}$ ,  $V_{EE} = 0\text{ V}$

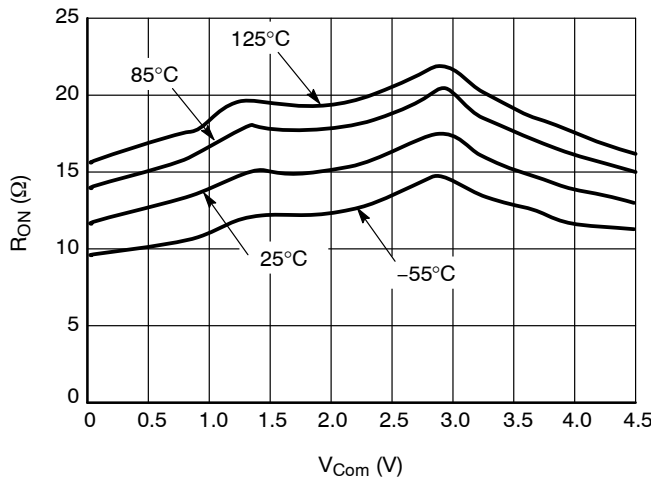
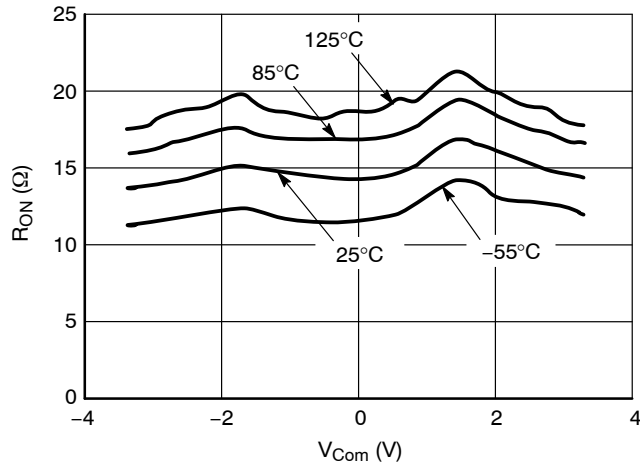
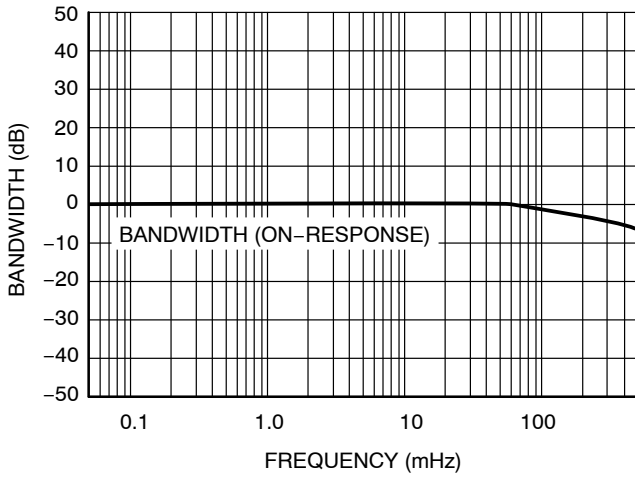


Figure 8. Typical On Resistance  
 $V_{CC} = 5.5\text{ V}$ ,  $V_{EE} = 0\text{ V}$

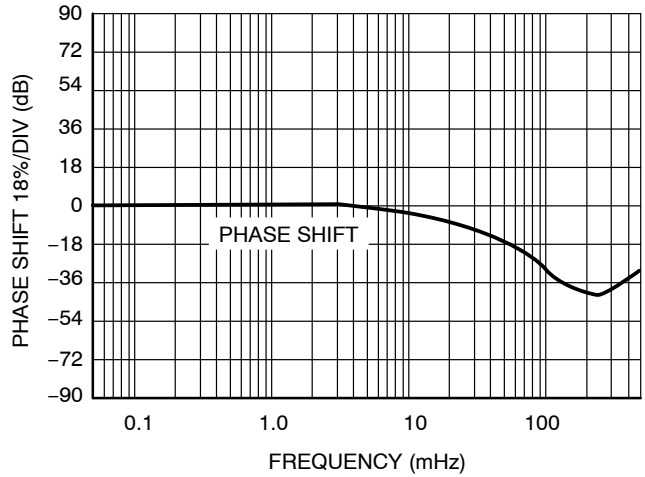
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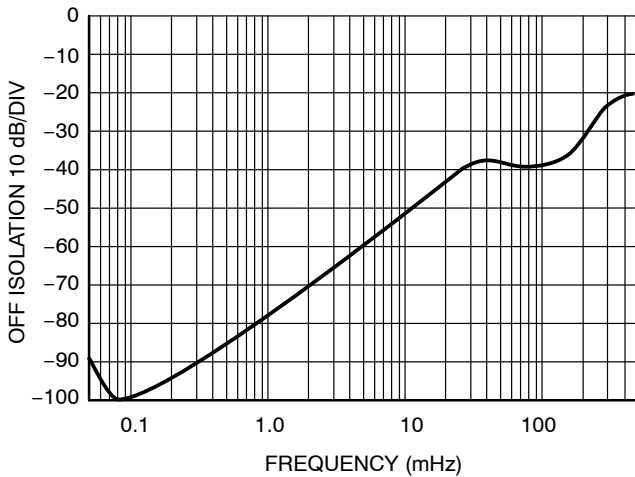
**Figure 9. Typical On Resistance**  
 $V_{CC} = 3.3\text{ V}, V_{EE} = -3.3\text{ V}$



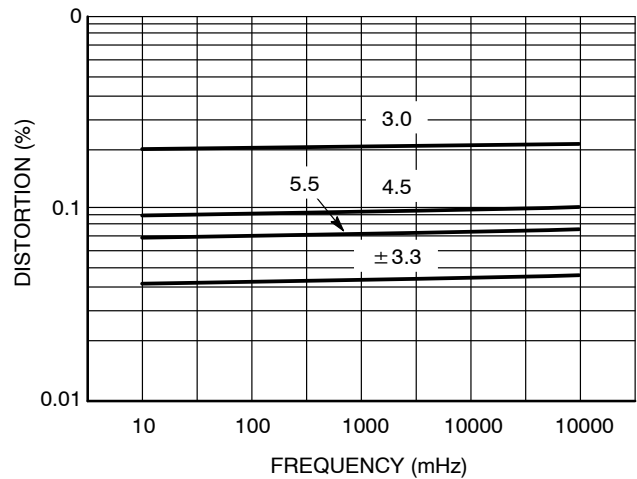
**Figure 10. Bandwidth,  $V_{CC} = 5.0\text{ V}$**



**Figure 11. Phase Shift,  $V_{CC} = 5.0\text{ V}$**



**Figure 12. Off Isolation,  $V_{CC} = 5.0\text{ V}$**



**Figure 13. Total Harmonic Distortion**

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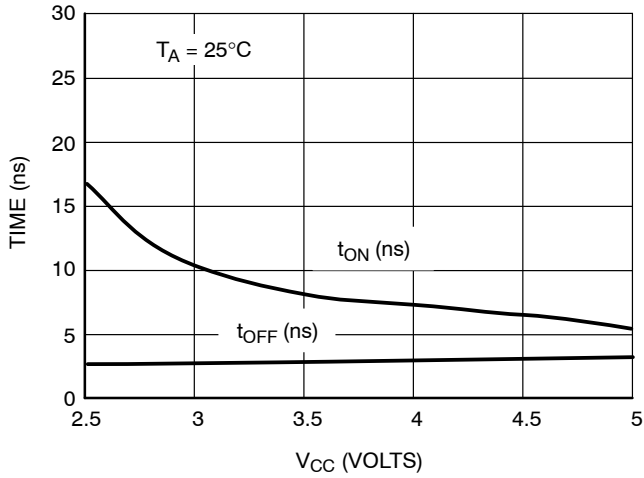


Figure 14.  $t_{ON}$  and  $t_{OFF}$  versus  $V_{CC}$

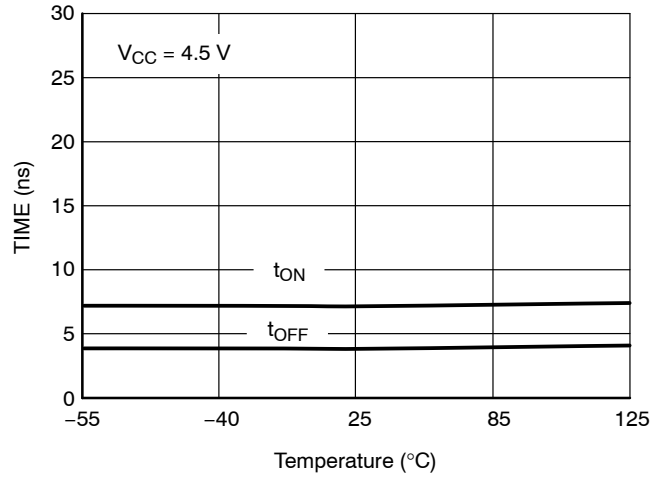


Figure 15.  $t_{ON}$  and  $t_{OFF}$  versus Temp

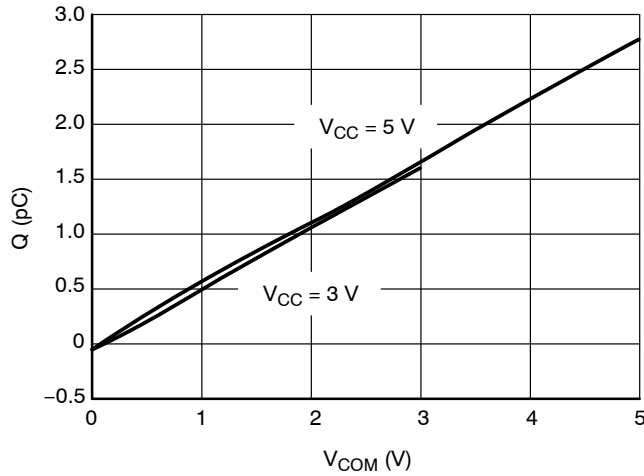


Figure 16. Charge Injection versus COM Voltage

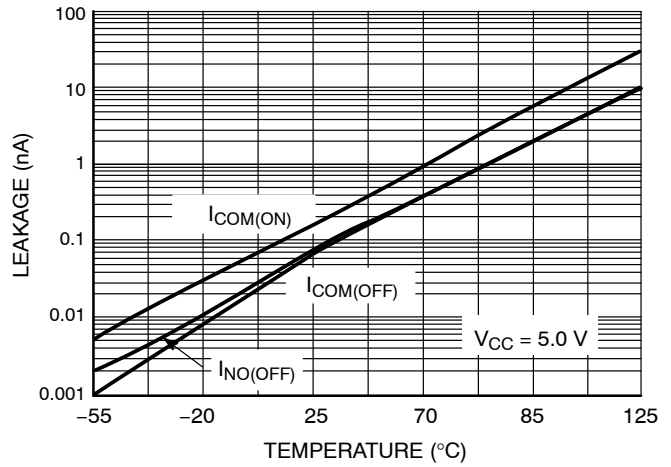


Figure 17. Switch Leakage versus Temperature

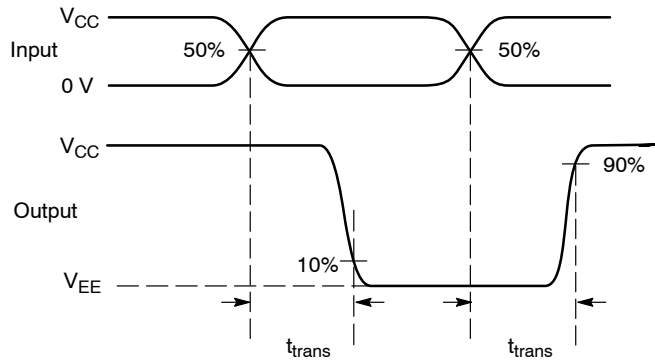
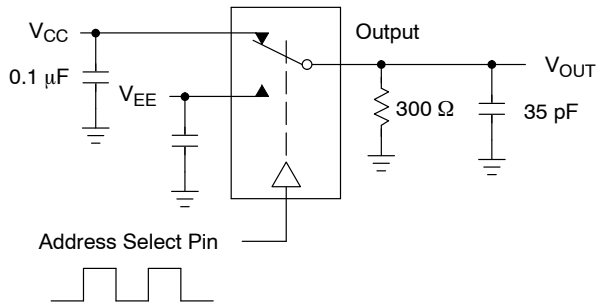


Figure 18. Channel Selection Propagation Delay

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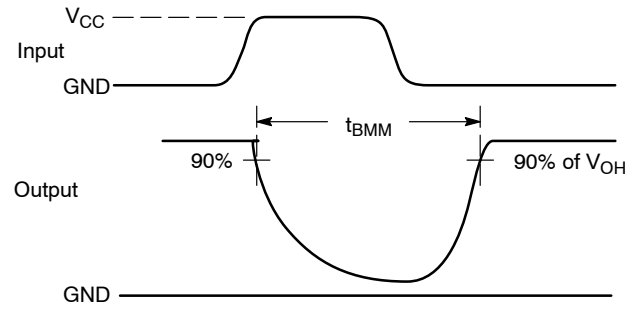
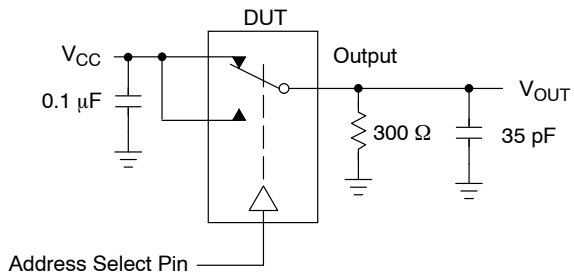


Figure 19.  $t_{BMM}$  (Time Break-Before-Make)

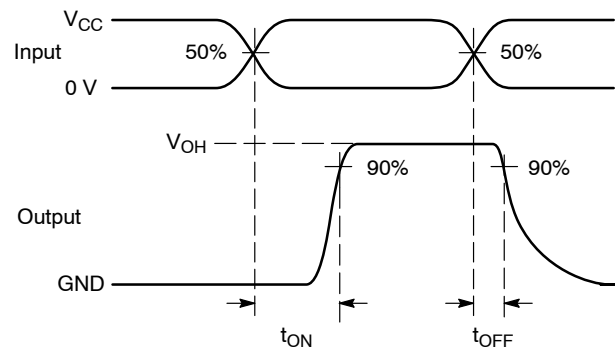
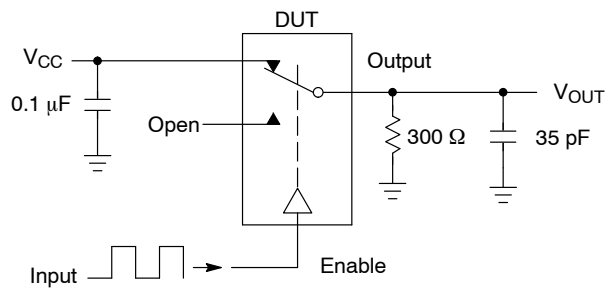


Figure 20.  $t_{ON}/t_{OFF}$

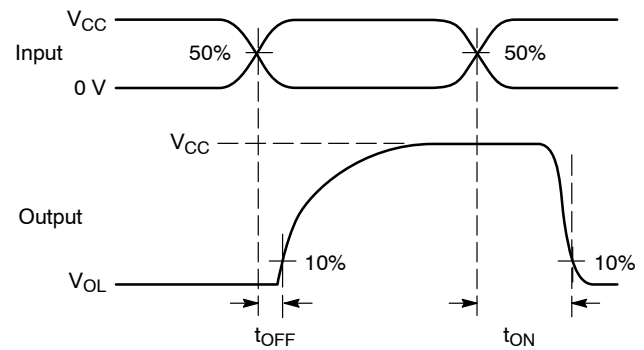
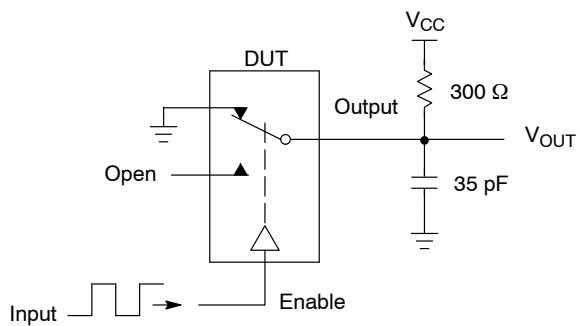
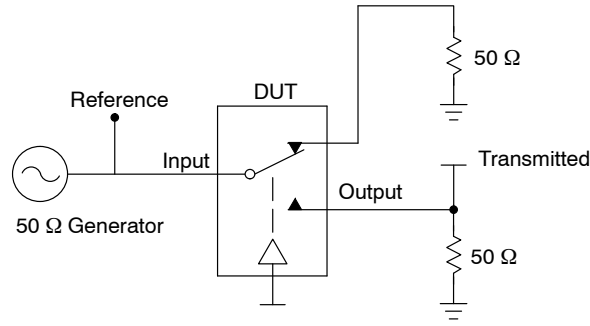


Figure 21.  $t_{ON}/t_{OFF}$



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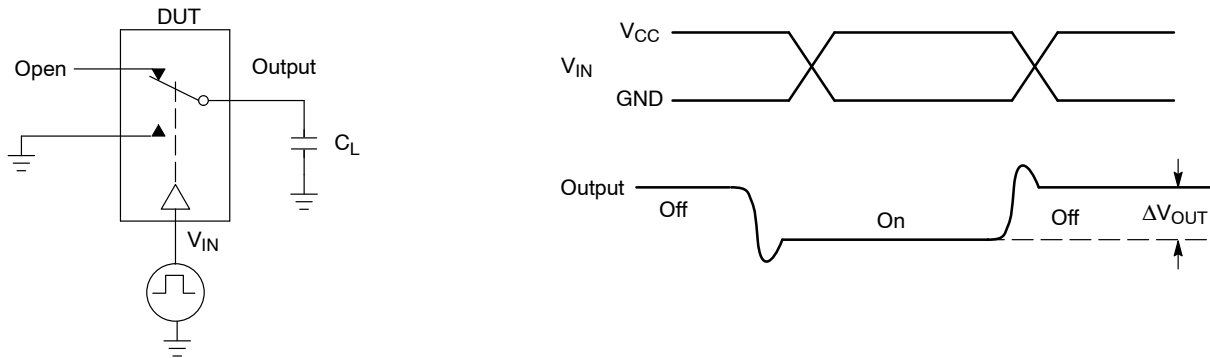
Channel switch Address and Inhibit/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch.  $V_{ISO}$ , Bandwidth and  $V_{ONL}$  are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left( \frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left( \frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

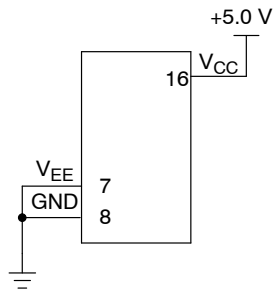
Bandwidth (BW) = the frequency 3 dB below  $V_{ONL}$

**Figure 22. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ $V_{ONL}$**

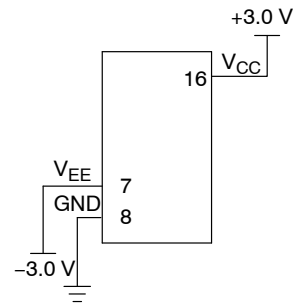


**Figure 23. Charge Injection: (Q)**

## TYPICAL OPERATION



**Figure 24. 5.0 Volts Single Supply**  
 $V_{CC} = 5.0 \text{ V}, V_{EE} = 0$

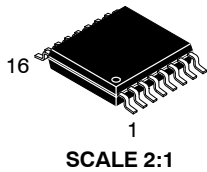


**Figure 25. Dual Supply**  
 $V_{CC} = 3.0 \text{ V}, V_{EE} = -3.0 \text{ V}$

# MECHANICAL CASE OUTLINE

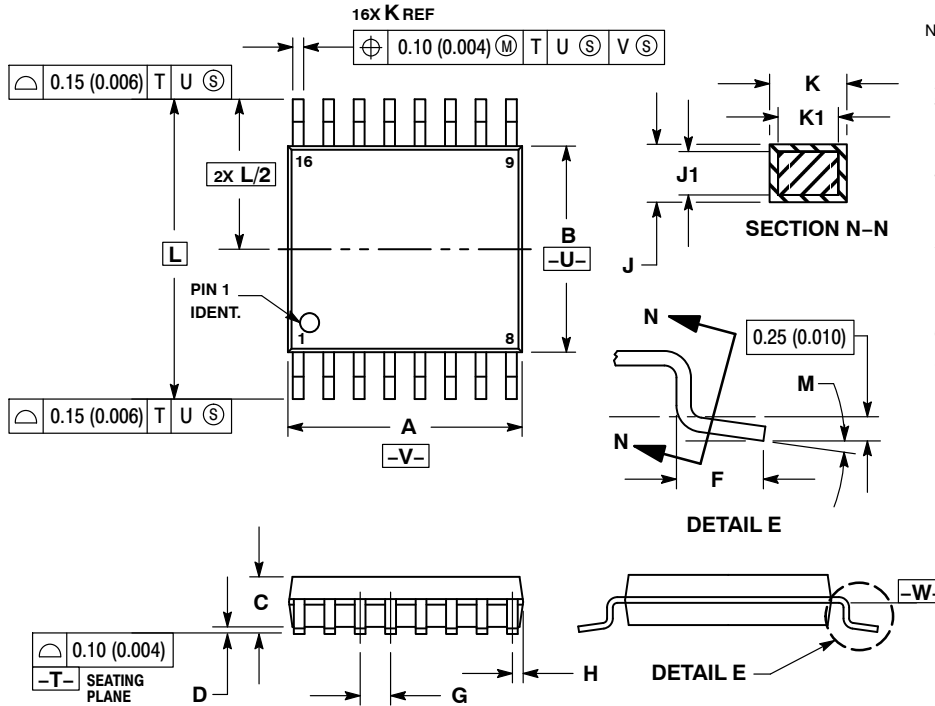
## PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-16  
CASE 948F-01  
ISSUE B

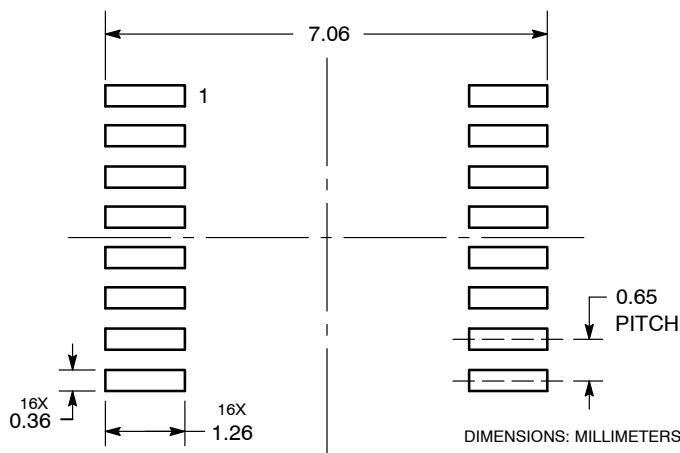
DATE 19 OCT 2006



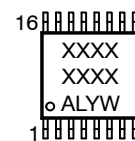
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

### SOLDERING FOOTPRINT



### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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