NLAS54404

Ultra-Low THD Stereo SPDT Switch with Independent Channel Selects

The NLAS54404 is a single supply, bidirectional, dual single−pole/double−throw (SPDT) ultra-low distortion, high OFF−Isolation analog switch that can pass analog signals that are positive and negative with respect to ground. It is primarily targeted at consumer and professional audio switching applications such as computer sound cards and home theater products. The inputs can accommodate ground referenced signals up to 2.0 V_{RMS} while operating from a single 3.3 V DC supply. The digital logic inputs are 1.8 V logic−compatible. It is used in DC−coupled ground-referenced applications.

With −118 dB THD+N performance with a 2.0 V_{RMS} signal into 20 kΩ load, superior signal muting, high PSRR and very flat frequency response, the NLAS54404 meets the exacting requirements of consumer and professional audio engineers.

Features

- Dual SPDT Switch or 2-to-1 MUX
- Independent Channel Selects
- 2.0 V_{RMS} Signal Switching from 3.3 V Supply
- −118 dB THD+N into 20 kΩ Load at 2.0 V_{RMS}
- −108 dB THD+N into 32 Ω Load at 3.9 mW
- Signal to Noise Ratio: > 119 dBV
- ±0.003 dB Insertion Loss at 1 kHz, 20 kΩ Load
- ±0.01 dB Gain Variation 20 Hz to 20 kHz
- 113 dB Signal Muting into 32 Ω Load
- 126 dB PSRR 20 Hz to 20 kHz
- Single Supply Operation: 3.3 V
- 12−Ball WLCSP, 1.6 mm x 1.2 mm
- This Device is Pb−Free, Halogen Free/BFR Free and is RoHS Compliant

Applications

- Computer Sound Cards
- Home Theater Audio Products
- SACD / DVD Audio
- DVD Player Audio Output Switching
- Headsets for MP3 / Cellphone Switching
- Hi−Fi Audio Switching Application

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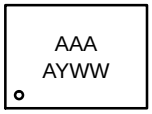
WLCSP12
FC SUFFIX
CASE 567LG

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NLAS54404FCTAG	WLCSP12 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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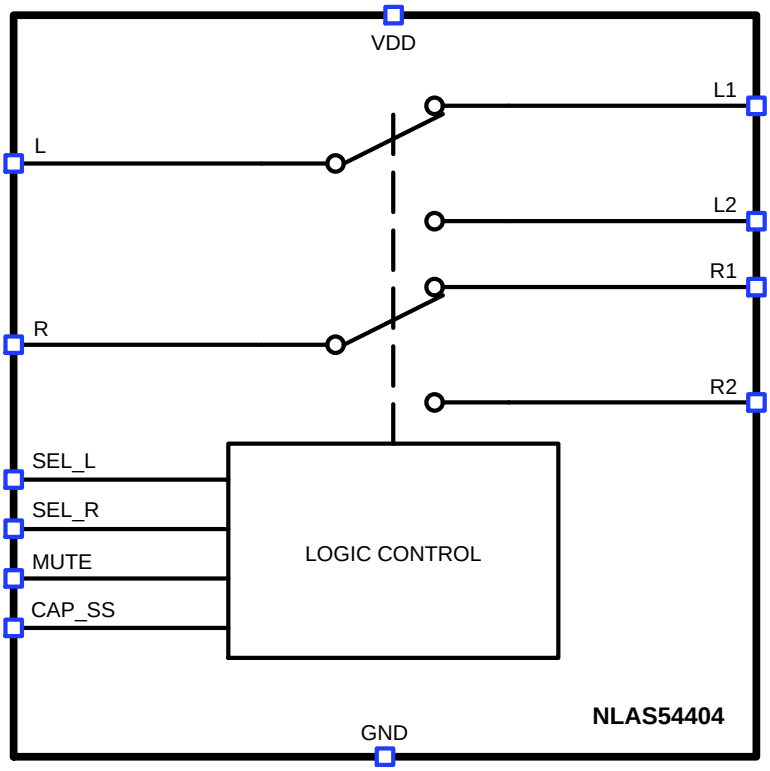


Figure 1. Block Diagram

Table 1. FUNCTION TABLE

Inputs			Outputs			
MUTE	**SEL_L**	**SEL_R**	**L1**	**L2**	**R1**	**R2**
0	0	0	ON	OFF	ON	OFF
0	0	1	ON	OFF	OFF	ON
0	1	0	OFF	ON	ON	OFF
0	1	1	OFF	ON	OFF	ON
1	X	X	OFF	OFF	OFF	OFF

NOTE: MUTE: Logic “0” ≤ 0.5 V, Logic “1” ≥ 1.4 V or float.
SEL_L, SEL_R: Logic “0” ≤ 0.5 V, Logic “1” ≥ 1.4 V.
X = Don’t Care

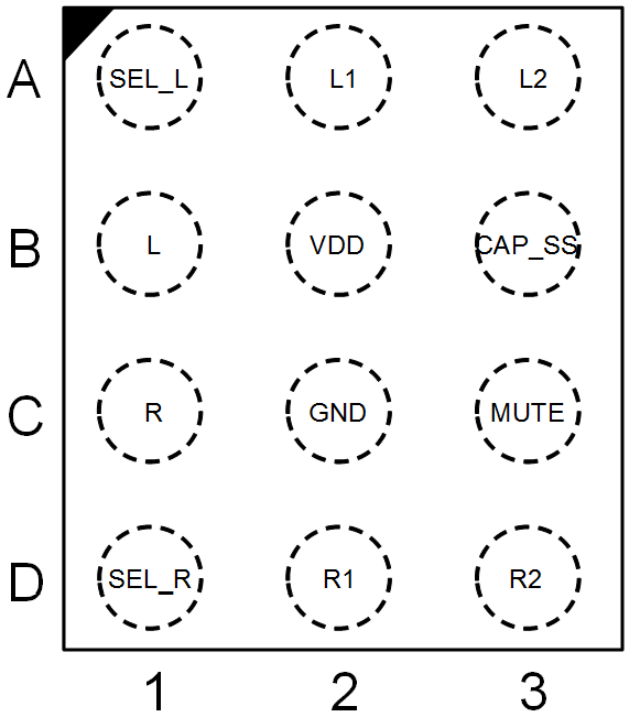


Figure 2. WLCSP−12 – Top Through View

Table 2. PIN DESCRIPTIONS

Pin Name	Ball	Description
VDD	B2	System power supply pin (+3 V to +3.6 V)
GND	C2	Ground connection
CAP_SS	B3	Turn−on delay capacitor pin
MUTE	C3	Signal mute control pin
SEL_R	D1	Input select control pin for Right
SEL_L	A1	Input select control pin for Left
R	C1	Analog switch common pin for Right
L	B1	Analog switch common pin for Left
R1	D2	Analog switch normally closed pin for Right
L1	A2	Analog switch normally closed pin for Left
R2	D3	Analog switch normally open pin for Right
L2	A3	Analog switch normally open pin for Right

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{DD}	Positive DC Supply Voltage	−0.5 to +4.1	V
V_{IS}	Analog Input/Output Voltage (L_1, L_2, R_1, R_2, L, R)	−3.1 to V_{DD} + 0.5	V
V_{IN}	Digital Select Input Voltage (SEL, MUTE, AC/DC, DIR_SEL)	−0.5 to V_{DD} + 0.5	V
I_{IO}	Switch Continuous Current (L_1, L_2, R_1, R_2, L, R)	±300	mA
I_{IO_PK}	Switch Peak Current (L_1, L_2, R_1, R_2, L, R) (Pulsed 1ms, 10% Duty Cycle, Max).	±500	mA
P_D	Power Dissipation in Still Air	800	mW
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C
T_J	Junction Bias Under Bias	150	°C
θ_{JA}	Thermal Resistance	80	°C/W
T_S	Storage Temperature	−65 to +150	°C
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 30% − 35%	UL94−V0 (0.125 in)	
ESD	ESD Protection Human Body Model Machine Model	> 4000 > 100	V
I_L	Latch−up Current, Above V_{CC} and below GND at 125°C (Note 1)	±300	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Positive 3V DC Supply Voltage	3.0	3.6	V
V_S	Switch Input / Output Voltage (L_1, L_2, R_1, R_2, L, R)	−2.9	V_{DD}	V
V_{IN}	Digital Select Input Voltage	GND	V_{DD}	V
T_A	Operating Temperature Range	−40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Voltages referenced to GND)
3.3 V Supply: V_{DD} = +3.0 V to +3.6 V, GND = 0 V, V_{SIGNAL} = 2.0 VRMS, R_{LOAD} = 20 kΩ , f = 1 kHz, V_{SELH} = V_{MUTEH} = 1.4 V, V_{SELL} = V_{MUTEL} = 0.5 V, CAP_SS = 0.1 μF, (Note 2), Unless otherwise specified.

Parameter	Test Conditions	Supply (V)	Temp (°C)	Min (Notes 3, 4)	Typ	Max (Notes 3, 4)	Units
ANALOG SWITCH CHARACTERISTICS							
Analog Signal Range, V_{ANALOG}		3.3	Full	−	2.0	−	V_{RMS}
ON−Resistance, r_{ON}	V_{DD} = 3.3 V, I_R or I_L = 80 mA, V_{Lx} or V_{Rx}	3.3	25	−	2.1	−	Ω
	= −2.828 V to +2.828 V (See Figure 6)		Full	−	2.3	−	
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 3.3 V, I_R or I_L = 80 mA, V_{Lx} or V_{Rx} = Voltage at max r_{ON} over −2.828 V to +2.828 V (Note 7)	3.3	25	−	0.0042	−	Ω
			Full	−	0.043	−	
r_{ON} Flatness, $r_{FLAT(ON)}$	V_{DD} = 3.3 V, I_R or I_L = 80 mA, V_{Lx} or V_{Rx}	3.3	25	−	0.021	0.055	Ω
	= −2.828 V, 0 V, +2.828 V (Note 5)		Full	−	0.051	−	
L, R, Lx, Rx Pull−down Resistance	V_{DD} = 3.6 V, V_{Lx} or V_{Rx} = −2.83 V, 2.83 V, V_L or V_R = −2.82 V, 2.83 V, $V_{AC/DC}$ = 0 V, V_{MUTE} = 3.6 V, measure current, calculate resistance.	3.6	25	225	300	375	kΩ
			Full	−	345	−	
DYNAMIC CHARACTERISTICS							
THD+N	V_{SIGNAL} = 2 V_{RMS}, f = 1 kHz, A−weighted filter, R_{LOAD} = 20 kΩ	3.3	25	−	< −118	−	dB
	V_{SIGNAL} = 1.9 V_{RMS}, f = 1 kHz, A−weighted filter, R_{LOAD} = 20 kΩ		25	−	< −117	−	
	V_{SIGNAL} = 1.8 V_{RMS}, f = 1 kHz, A−weighted filter, R_{LOAD} = 20 kΩ		25	−	< −116	−	
	V_{SIGNAL} = 0.707 V_{RMS}, f = 1 kHz, A−weighted filter, R_{LOAD} = 32 Ω		25	−	< −108	−	
SNR	f = 20 Hz to 20 kHz, A−weighted filter, inputs grounded, R_{LOAD} = 20 kΩ or 32 Ω	3.3	25	−	> 119	−	dBV
Insertion Loss, G_{ON}	f = 1 kHz, R_{LOAD} = 20 kΩ	3.3	25	−	±0.003	−	dB
Gain vs Frequency, G_f	f = 20 Hz to 20 kHz, R_{LOAD} = 20 kΩ, reference to G_{ON} at 1 kHz	3.3	25	−	±0.01	−	dB
Stereo Channel Imbalance L_1 and R_1, L_2 and R_2	f = 20 Hz to 20 kHz, R_{LOAD} = 20 kΩ	3.3	25	−	±0.006	−	dB
OFF−Isolation (Muting)	f = 20 Hz to 22 kHz, L = R = 2 V_{RMS}, R_{LOAD} = 20 kΩ, MUTE = 3.3 V, SEL_L/SEL_R = "X"	3.3	25	−	105	−	dB
	f = 20 Hz to 22 kHz, V_L or V_R = 0.7 V_{RMS}, R_{LOAD} = 32 Ω		25	−	112	−	
Crosstalk (Channel−to− Channel)	R_L = 20 kΩ, f = 20 Hz to 20 kHz, V_{SIGNAL} = 2 V_{RMS}, signal source impedance = 20 Ω, (Note 8)	3.3	25	−	90	−	dB
	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_{SIGNAL} = 0.7 V_{RMS}, signal source impedance = 20 Ω, (Note 8)		25	−	112	−	
PSRR	f = 1 kHz, V_{SIGNAL}= 100 mV_{RMS}, inputs grounded	3.3	25	−	131	−	dB

2. V_{IN} = input voltage to perform proper function.
3. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
4. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
5. Flatness is defined as the difference between maximum and minimum value of ON−resistance at the specified analog signal voltage points.
6. Limits established by characterization and are not production tested.
7. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value.
8. Crosstalk is inversely proportional to source impedance.

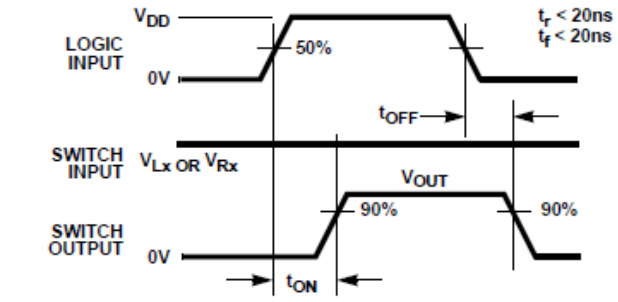
DC ELECTRICAL CHARACTERISTICS (Voltages referenced to GND)
3.3 V Supply: V_{DD} = +3.0 V to +3.6 V, GND = 0 V, V_{SIGNAL} = 2.0 VRMS, R_{LOAD} = 20 kΩ , f = 1 kHz, V_{SELH} = V_{MUTEH} = 1.4 V, V_{SELL} = V_{MUTEL} = 0.5 V, CAP_SS = 0.1 μF, (Note 2), Unless otherwise specified.

Parameter	Test Conditions	Supply (V)	Temp (°C)	Min (Notes 3, 4)	Typ	Max (Notes 3, 4)	Units
DYNAMIC CHARACTERISTICS							
PSRR	f = 20 kHz, V_{SIGNAL}= 100 mV_{RMS}, inputs grounded	3.3	25	−	131	−	dB
Bandwidth, −3 dB	R_{LOAD} = 50 Ω	3.3	25	−	250	−	MHz
ON to Mute Time, $T_{TRANS-OM}$	CAP_SS = 0.1 μF	3.3	25	−	245	−	ns
Mute to ON Time, $T_{TRANS-MO}$	CAP_SS = 0.1 μF, R_L = 32 Ω, V_{IS} = 1.5V	3.3	25	−	1810	−	μs
Turn−ON Time, t_{ON}	V_{DD} = 3.3 V, V_{Lx} or V_{Rx} = 1.5 V, V_{MUTE} = 0 V, R_L = 32 Ω to 20 kΩ (See Figure 3)	3.3	25	−	20.7	−	μs
Turn−OFF Time, t_{OFF}	V_{DD} = 3.3 V, V_{Lx} or V_{Rx} = 1.5 V, V_{MUTE} = 0 V, R_L = 32 Ω to 20 kΩ (See Figure 3)	3.3	25	−	100	−	ns
Break−Before−Make Time Delay, t_D	V_{DD} = 3.6 V, V_{Lx} or V_{Rx} = 1.5 V, V_{MUTE} = 0 V, R_L = 32 Ω to 20 kΩ (See Figure 4)	3.6	25	−	17.6	−	μs
OFF−Isolation	R_L = 50 Ω, f = 1 MHz, V_L or V_R = 1 V_{RMS} (See Figure 5)	3.3	25	−	64	−	dB
Crosstalk (Channel−to−Channel)	R_L = 50 Ω, f = 1 MHz, V_L or V_R = 1 V_{RMS} (See Figure 7)	3.3	25	−	75	−	dB
Lx, Rx OFF Capacitance, C_{OFF}	f = 1 MHz, V_{Lx} or V_{Rx} = V_L or V_R = 0 V (See Figure 8)	3.3	25	−	6.8	−	pF
L, R ON Capacitance, $C_{COM(ON)}$	f = 1 MHz, V_{Lx} or V_{Rx} = V_{COM} = 0 V (See Figure 8)	3.3	25	−	11.5	−	pF
POWER SUPPLY CHARACTERISTICS							
Power Supply Range, V_{DD}		3.3	Full	3	−	3.6	V
Positive Supply Current, I+	V_{DD} = +3.6 V, V_{MUTE} = 0 V,	3.6	25	−	54	65	μA
	V_{SEL} = 0 V or V_{DD}	3.6	Full	−	59	−	
	V_{DD} = +3.6 V, V_{MUTE} = V_{DD},	3.6	25	−	14	18	
	V_{SEL} = 0 V or V_{DD}	3.6	Full	−	15	−	
	V_{DD} = +3.6 V, V_{MUTE} = 0 V,	3.6	25	−	55	65	
	V_{SEL} = 1.8 V	3.6	Full	−	58	−	
DIGITAL INPUT CHARACTERISTICS							
Input Voltage Low, V_{SELL}, V_{MUTEL}		3.3	Full	−	−	0.5	V
Input Voltage High, V_{SELH}, V_{MUTEH}		3.3	Full	1.4	−	−	V
Input Current, I_{SELH}, I_{SELL}	V_{DD} = 3.6 V, V_{MUTE} = 0 V, V_{SEL} = 0 V or V_{DD}	3.6	Full	−0.5	0.01	0.5	μA
Input Current, I_{MUTEL}	V_{DD} = 3.6 V, V_{SEL} = V_{DD}, V_{MUTE} = 0 V	3.6	Full	−1.3	−0.7	0.3	μA
Input Current, I_{MUTEH}	V_{DD} = 3.6 V, V_{SEL} = 0 V, V_{MUTE} = V_{DD}	3.6	Full	−0.5	0.01	0.5	μA

2. V_{IN} = input voltage to perform proper function.
3. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
4. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
5. Flatness is defined as the difference between maximum and minimum value of ON−resistance at the specified analog signal voltage points.
6. Limits established by characterization and are not production tested.
7. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value.
8. Crosstalk is inversely proportional to source impedance.

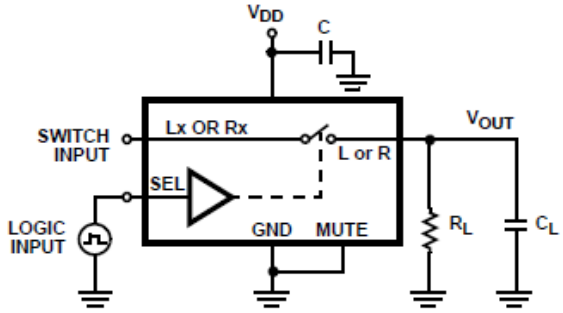
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TEST CIRCUITS AND WAVEFORMS



Logic input waveform is inverted for switches that have the opposite logic sense.

MEASUREMENT POINTS

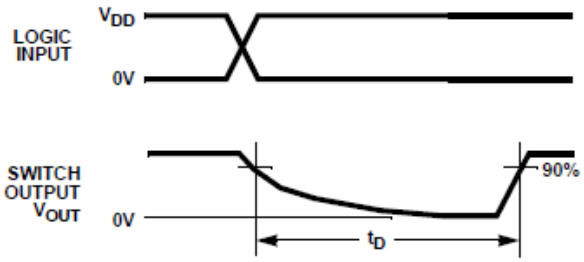


Repeat test for all switches. C_L includes fixture and stray capacitance.

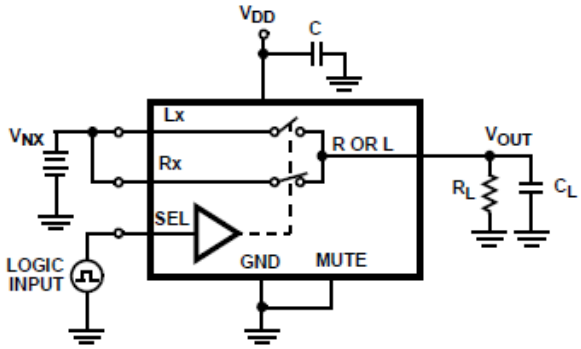
$$V_{OUT} = V_{(Lx \text{ or } Rx)} \frac{R_L}{R_L + r_{ON}}$$

TEST CIRCUIT

Figure 3. Switching Times



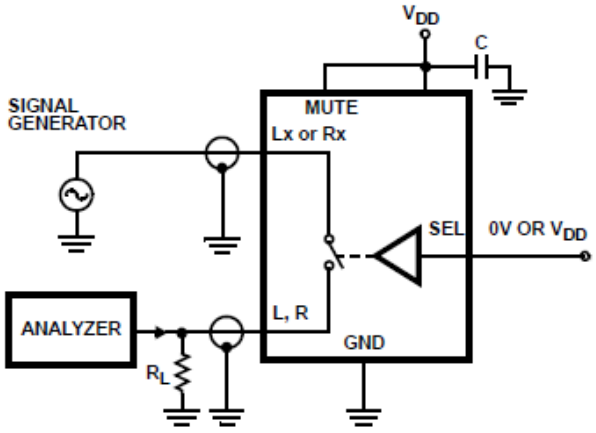
MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

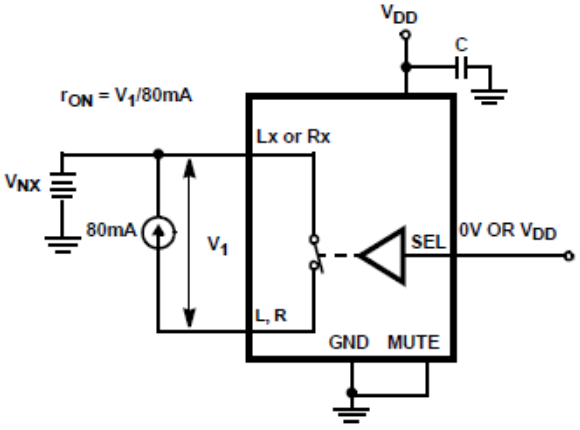
TEST CIRCUIT

Figure 4. Break−Before−Make Time



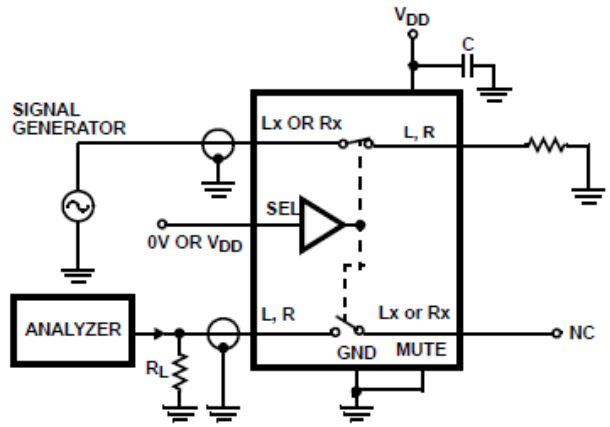
Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

Figure 5. Off−Isolation Test Circuit



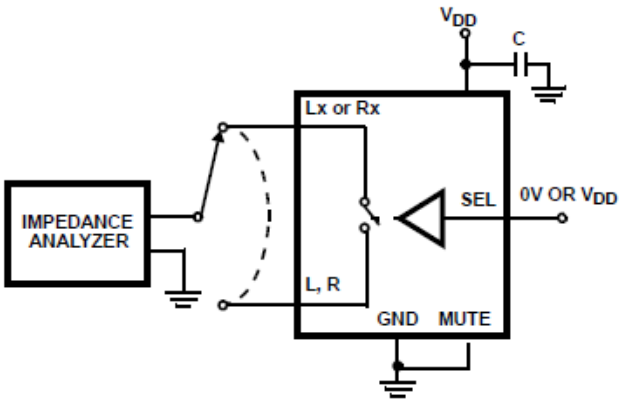
Repeat test for all switches.

Figure 6. r_{ON} Test Circuit



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

Figure 7. Crosstalk Test Circuit



Repeat test for all switches.

Figure 8. Capacitance Test Circuit

Sound Card Application Block Diagrams

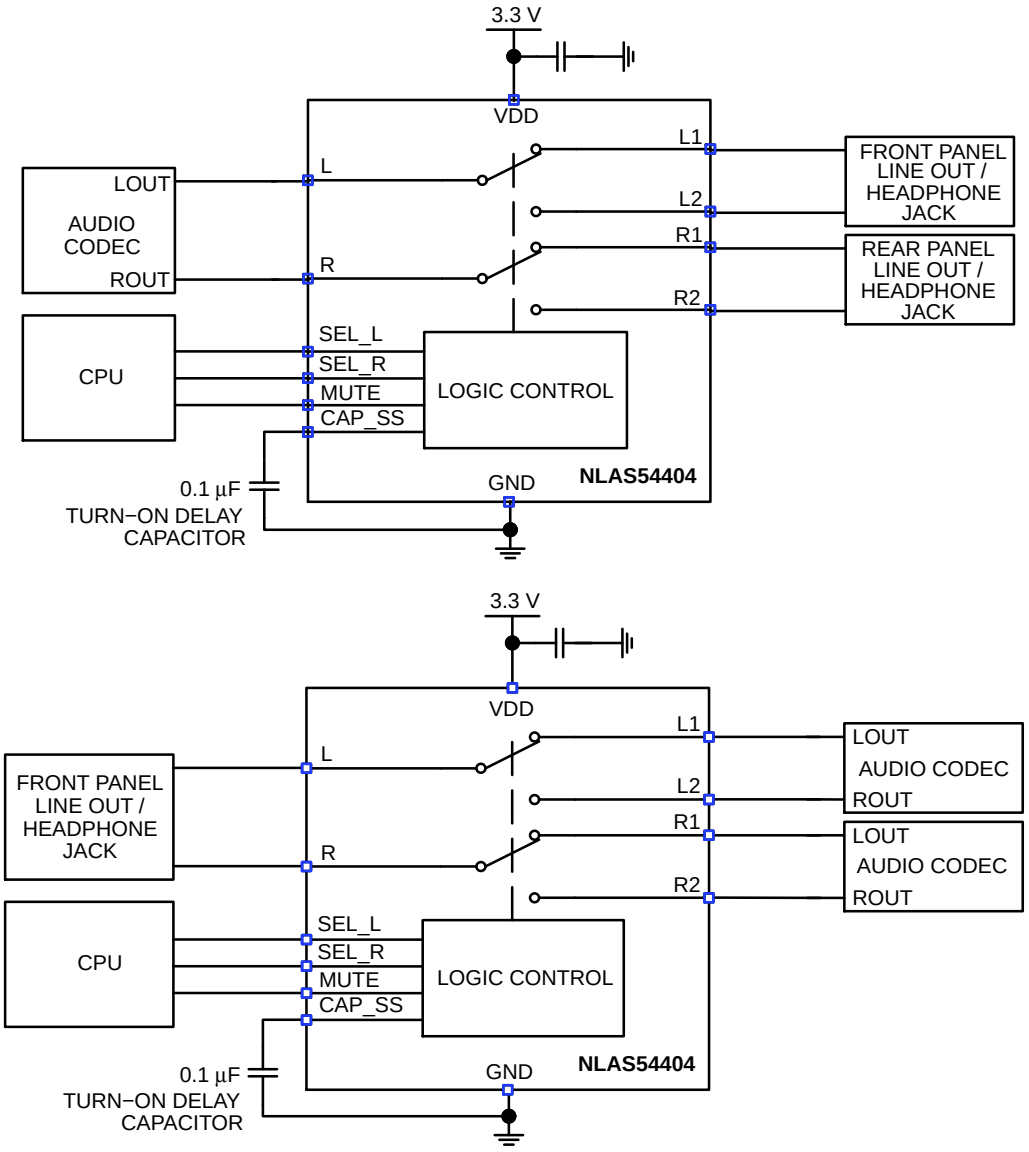


Figure 9. Typical Application

Detailed Description

The NLAS54404 is a single supply, bidirectional, dual single pole/double throw (SPDT) ultra−low distortion, high OFF−Isolation analog switch. It was designed to operate from a 3.3 V single supply. The switches can accommodate ±2.828 V_{PEAK} (2 V_{RMS}) ground−referenced analog signals. The switch r_{ON} flatness across this range is extremely small resulting in excellent THD+N performance (0.00013% with 20 kΩ load and 0.00039% with 32 Ω load at 707 mV_{RMS}).

The NLAS54404 was designed primarily for consumer and professional audio switching applications such as computer sound cards and home theater products. The “Sound Card Application Block Diagrams” show two typical sound card applications. In the upper block diagram, the NLAS54404 is being used to route a single stereo source to either the front or back panel line outs of the computer sound card. In the lower block diagram, the NLAS54404 is being used to multiplex two stereo sources to a single line out of the computer sound card.

SPDT Switch Cell Architecture and Performance Characteristics

The normally open (L_2, R_2) and normally closed (L_1, R_1) of the SPDT switches have a typical r_{ON} of 2.1 Ω and an OFF−isolation of > 113 dB. The low on−resistance (2.1 Ω and r_{ON} flatness (0.021 Ω) provide very low insertion loss and minimal distortion to applications that require hi−fidelity signal reproduction.

The SPDT switch cells have internal charge pumps that allow for signals to swing below ground. They were specifically designed to pass audio signals that are ground referenced and have a swing of ±2.828 V_{PEAK} while driving either 10 k / 20 kΩ (receiver) or 32 Ω (headphone) loads.

Each switch cell incorporates special circuitry to delay the switch transition from the OFF−state (high impedance) to the ON−state (2.1 Ω). This turn−on delay may help reduce clicks and pops in the speaker by matching turn−on time to transient switching events. The turn−on delay time is determined by the capacitor value of the delayed turn−on capacitor connected at the CAP_SS pin, the speaker load and the DC level of the audio signal. With a 0.1 μF ceramic chip capacitor, a 32 Ω load and 1.5 V DC level, the turn−on delay is approximately 1810 μs. The turn−on delay may be disabled by floating the CAP_SS pin.

Supply Voltage, Signal Amplitude, and Grounding

The power supply connected at VDD pin provides power to the NLAS54404 part. The NLAS54404 is a single supply device that was designed to be operated with a 3.0 V to 3.6 V DC supply connected at the VDD pin. It was specifically designed to accept ground referenced 2 V_{RMS} (±2.828 V_{PEAK}) audio signals at its signal pins while driving either 10 k / 20 kΩ receiver loads or 32 Ω headphone loads.

When using the part in an application, a 0.1 μF decoupling capacitor should be connected from the VDD pin to ground to minimize power supply noise and transients. This capacitor should be located as close to the pin as possible.

Mute Operation

When the MUTE logic pin is driven HIGH, the part will go into the mute state. In the mute state, all switches of the SPDTs are open. See “Logic Control” below for more details.

Mute to On

When the MUTE pin is driven LOW, the resistance of the switches selected by the SEL_x pin will go from high OFF resistance to their ON resistance of 2.1 Ω after a certain time delay.

The turn−on delay time is determined by the capacitor value of the delayed turn−on capacitor connected at the CAP_SS pin, the speaker load and the DC level of the audio signal. See Figures 26 and 27.

Table 3 indicates how mute to ON delay is affected by the CAP_SS capacitor value and the switch input DC voltage level.

Table 3. SIGNAL TURN−ON DELAY FOR A 32 Ω LOAD

Capacitor Value	V_{IS} DC Level	Turn−On Delay
No Capacitor	1.5 V	30.2 μs
0.05 μF	1.5 V	564 μs
0.1 μF	1.5 V	1810 μs
No Capacitor	60 mV	27.6 μs
0.05 μF	60 mV	40 μs
0.1 μF	60 mV	56.4 μs

On to Mute

When the MUTE pin is driven HIGH, the switches will turn off quickly (245 ns).

Logic Control

The NLAS54404 has three logic control pins; MUTE, SEL_L and SEL_R. The MUTE, SEL_L and SEL_R control pins determine the state of the switches.

The NLAS54404 logic is 1.8 V CMOS compatible (Low ≤ 0.5 V and High ≥ 1.4 V) over a supply range of 3.0 V to 3.6 V at the VDD pin. This allows control via 1.8 V or 3 V μ−controller.

SEL_L, SEL_R, Mute Control Pins

The state of the SPDT switches of the NLAS54404 device is determined by the voltage at the MUTE, SEL_L SEL_R pins. The SEL_L and SEL_R control pins are only active when MUTE is logic “0”. The MUTE has an internal pull−up resistor to the internal 3.3 V supply rail and can be driven HIGH or tri−stated (floated) by the μ−processor.

These pins are 1.8 V logic compatible. When powering the part by the VDD pin, the logic voltage can be as high as the VDD voltage which is typically 3.3 V.

Logic Levels:

MUTE = Logic “0” (Low) when ≤ 0.5 V

MUTE = Logic “1” (High) when ≥ 1.4 V or floating

SEL = Logic “0” (Low) when ≤ 0.5 V

SEL = Logic “1” (High) when ≥ 1.4 V

DC Coupled Operation

The Audio CODEC drivers can be directly coupled to the NLAS54404 when the audio signals from the drivers are ground referenced or do not have a significant DC offset voltage, < 50 mV.

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes or diode stacks from the pin to VDD and to GND (see Figure 10). To prevent forward biasing these diodes, VDD must be applied before any input signals, and the signal voltages must remain between VDD and −3 V and the logic voltage must remain between VDD and ground.

If these conditions cannot be guaranteed, then precautions must be implemented to prohibit the current and voltage at the logic pin and signal pins from exceeding the maximum ratings of the switch. The following two methods can be used to provide additional protection to limit the current in the event that the voltage at a signal pin goes below ground by more than −3 V or above the VDD rail and the logic pin goes below ground or above the VDD rail.

Logic inputs can be protected by adding a 1 kΩ resistor in series with the logic input (see Figure 10). The resistor limits the input current below the threshold that produces permanent damage, and the sub−microamp input current produces an insignificant voltage drop during normal operation.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low r_{ON} switch. Connecting Schottky diodes to the signal pins, as shown in Figure 10 will shunt the fault current to the supply or to ground thereby protecting the switch. These Schottky diodes must be sized to handle the expected fault current and to clamp when the voltage reaches the overvoltage limit.

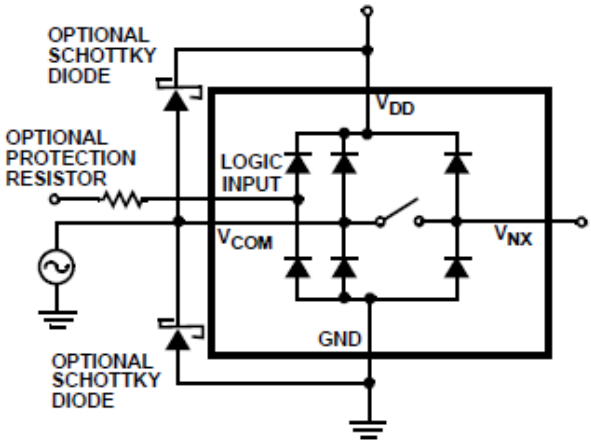


Figure 10. OVERVOLTAGE PROTECTION

High−Frequency Performance

In 50 Ω systems, the NLAS54404 has a −3 dB bandwidth of 250 MHz (see Figure 28). The frequency response is very consistent over varying analog signal levels.

An OFF−switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feed−through from a switch’s input to its output. OFF−Isolation is the resistance to this feed−through, while crosstalk indicates the amount of feed−through from one switch to another. Figure 29 details the high OFF−Isolation and crosstalk rejection provided by this part. At 1 MHz, Off−Isolation is about 64 dB in 50 Ω systems, decreasing approximately 20 dB per decade as frequency increases. Higher load impedances decrease OFF−Isolation and crosstalk rejection due to the voltage divider action of the switch off impedance and the load impedance.

TYPICAL CHARACTERISTICS

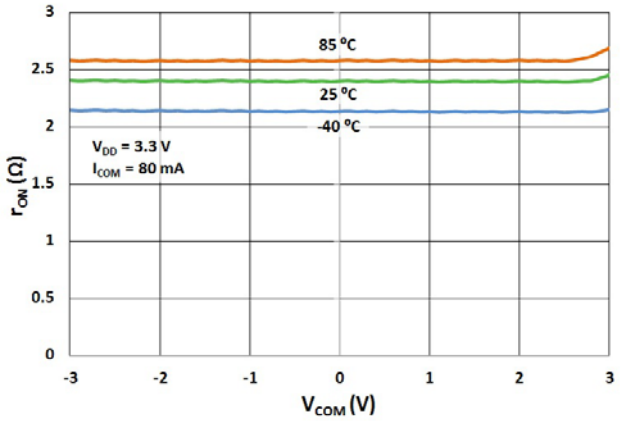


Figure 11. On−Resistance vs. Switch Voltage

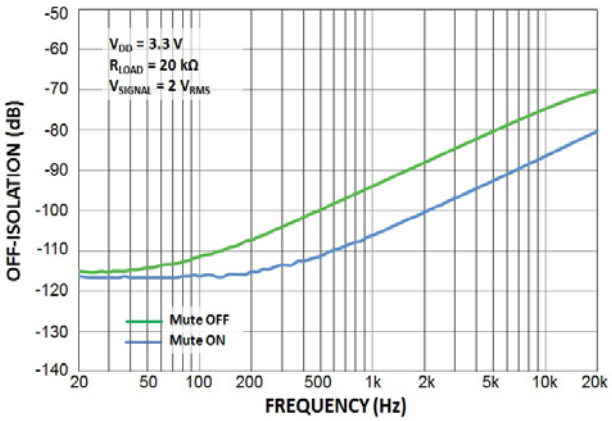


Figure 12. Off−Isolation, 2 V_{RMS} Signal, 20 kΩ Load

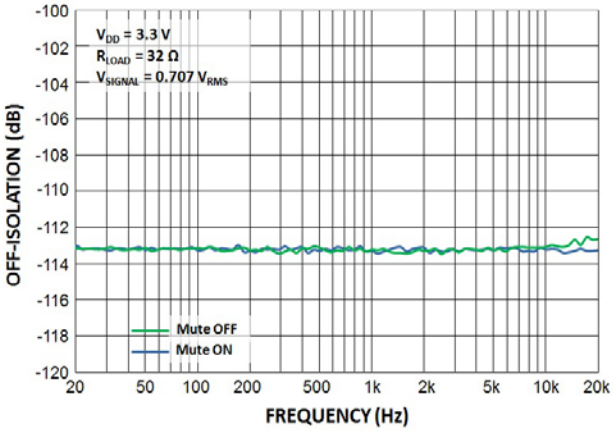


Figure 13. Off−Isolation, 0.707 V_{RMS} Signal, 32 Ω Load

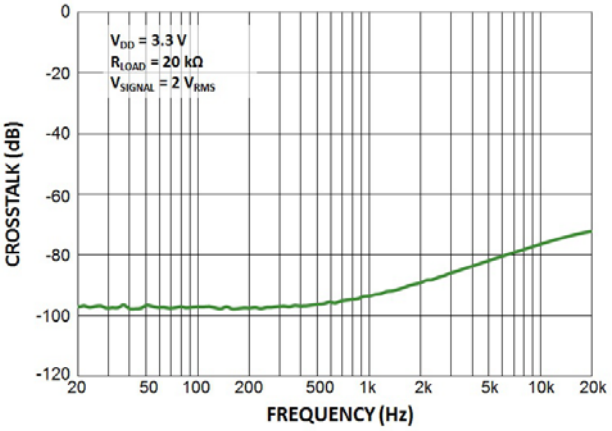


Figure 14. Channel−to−Channel Crosstalk

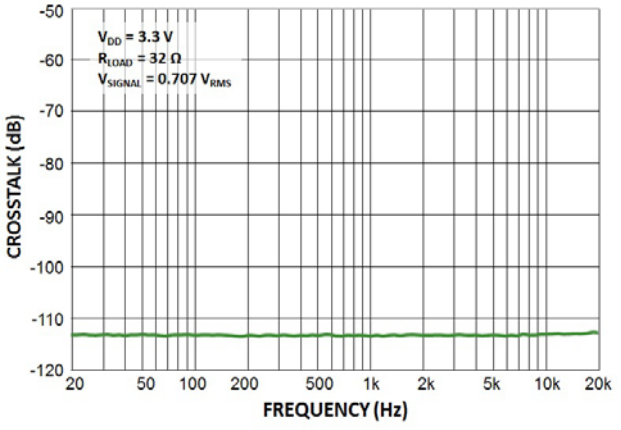


Figure 15. Channel−to−Channel Crosstalk

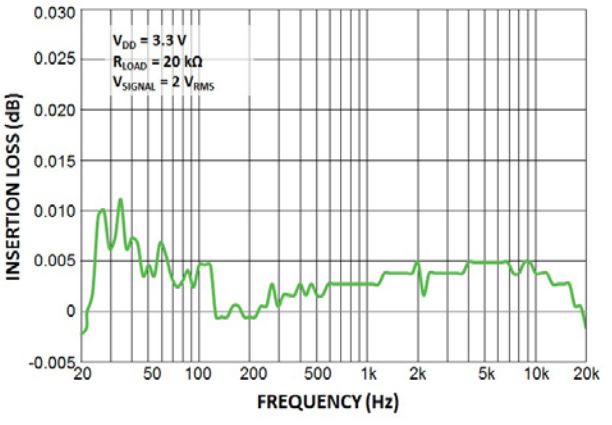


Figure 16. Insertion Loss vs. Frequency

TYPICAL CHARACTERISTICS

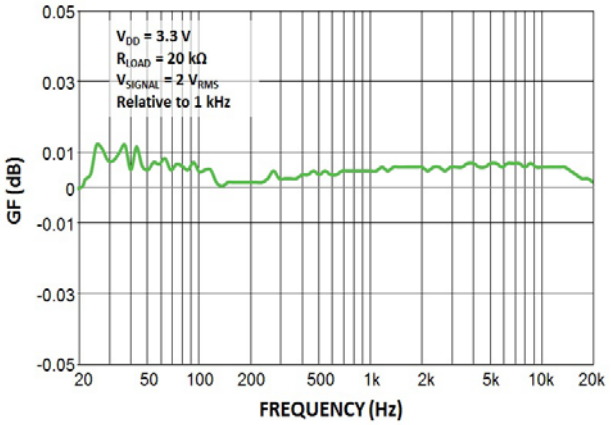


Figure 17. Gain vs. Frequency

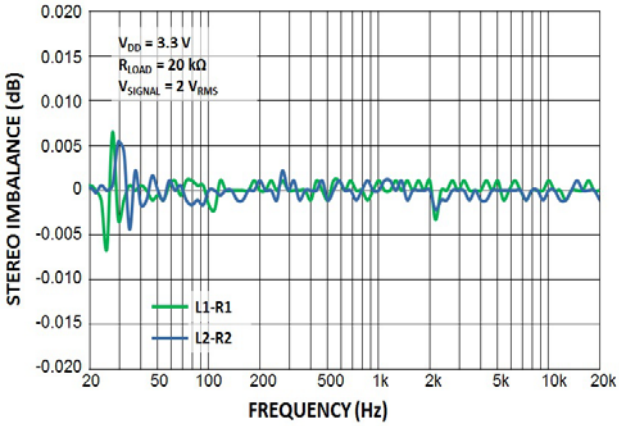


Figure 18. Stereo Imbalance vs. Frequency

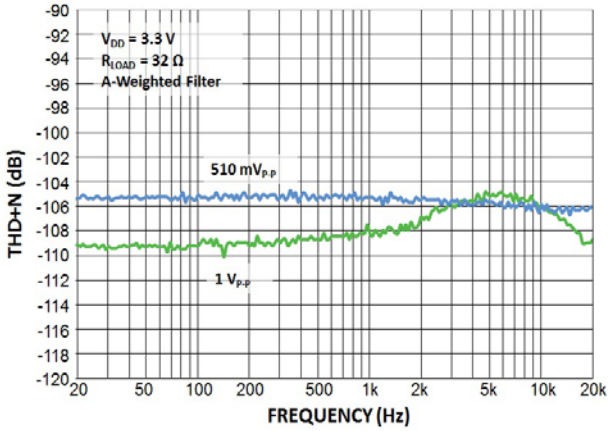


Figure 19. THD+N vs. Signal Levels vs. Frequency

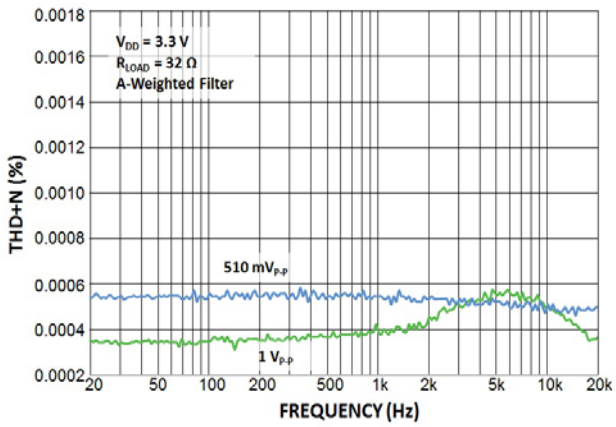


Figure 20. THD+N vs. Signal Levels vs. Frequency

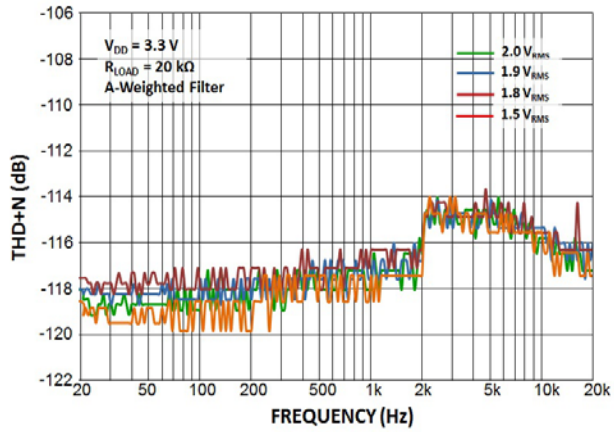


Figure 21. THD+N vs. Signal Levels vs. Frequency

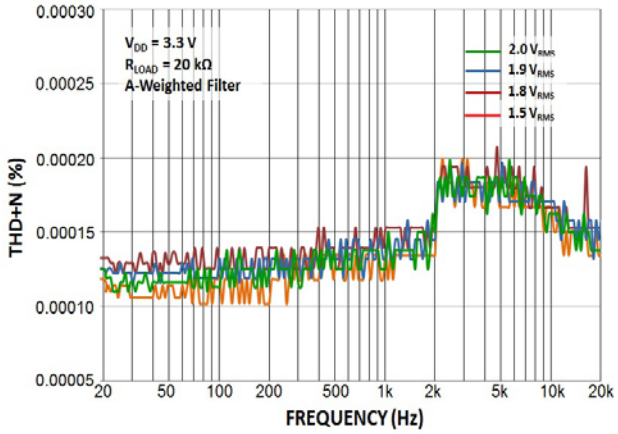


Figure 22. THD+N vs. Signal Levels vs. Frequency

TYPICAL CHARACTERISTICS

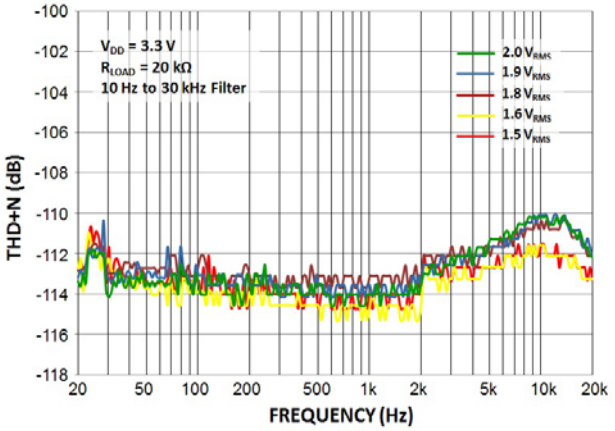


Figure 23. THD+N vs. Signal Levels vs. Frequency

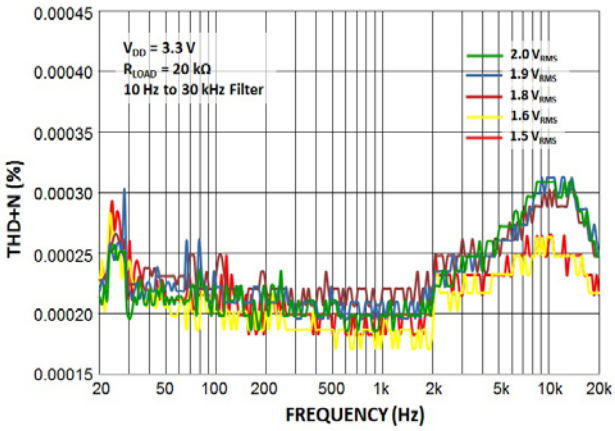


Figure 24. THD+N vs. Signal Levels vs. Frequency

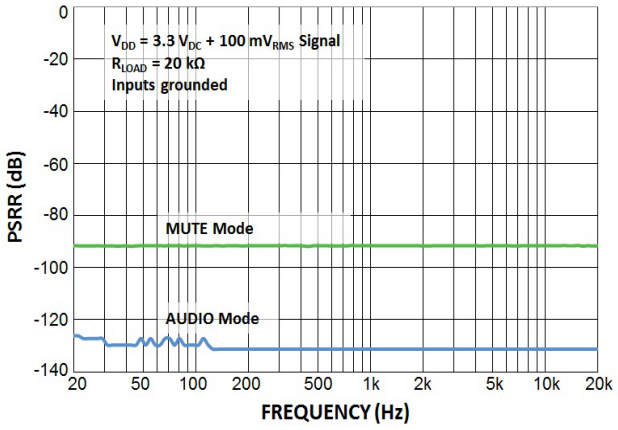


Figure 25. PSRR vs. Frequency

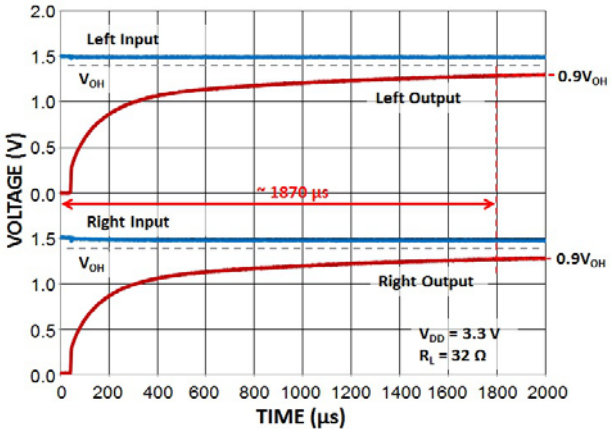


Figure 26. Switch Turn−On Dealy Time (0.1 µF)

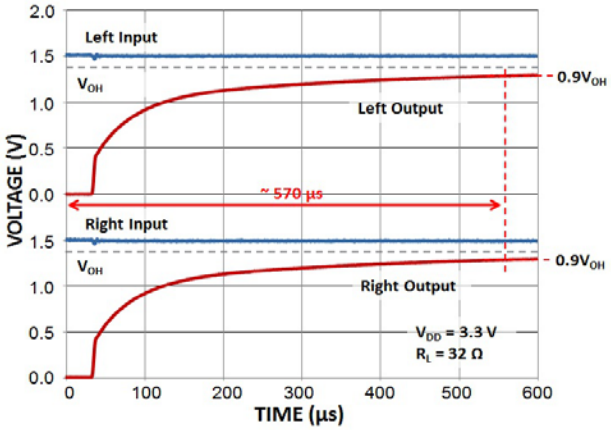


Figure 27. Switch Turn−On Dealy Time (0.05 µF)

TYPICAL CHARACTERISTICS

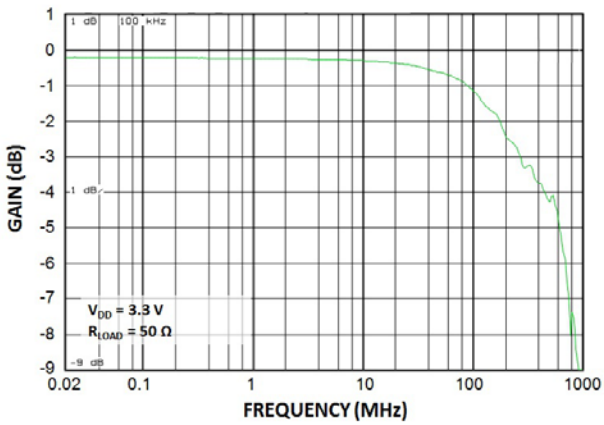


Figure 28. Frequency Response

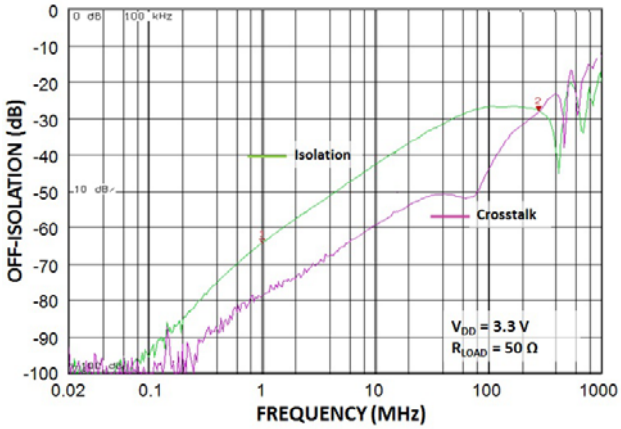


Figure 29. Crosstalk and Off−Isolation

PACKAGE DIMENSIONS

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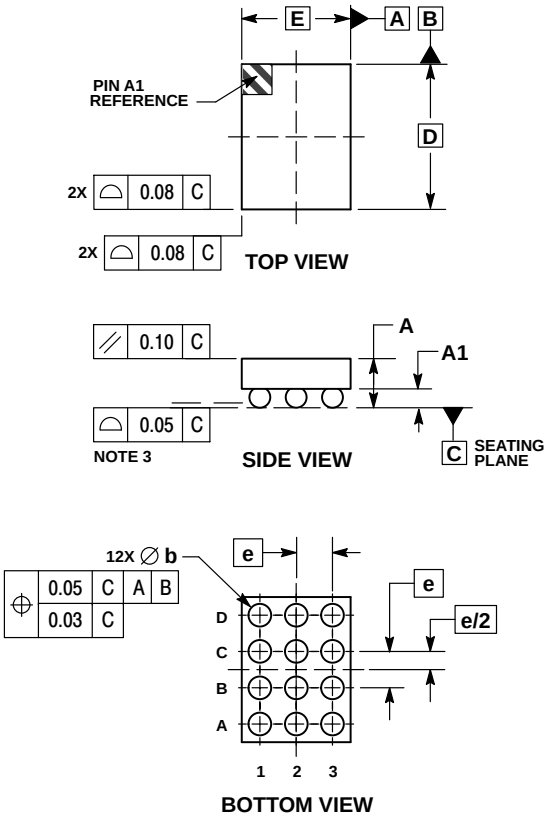
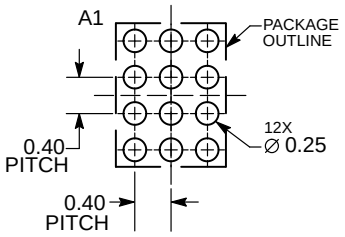
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.54
A1	0.187	0.23
b	0.23	0.27
D	1.60 BSC	
E	1.20 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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