Single 2-Input NOR Gate

NLV74HC1G02

The NLV74HC1G02 is a high speed CMOS 2−input NOR gate fabricated with silicon gate CMOS technology.

The internal circuit is composed of multiple stages, including a buffer output which provides high noise immunity and stable output.

The NLV74HC1G02 output drive current is 1/2 compared to MC74HC series.

Features

- High Speed: t_{PD} = 7 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 1 μA (Max) at T_A = 25°C
- High Noise Immunity
- Balanced Propagation Delays (t_{pLH} = t_{pHL})
- Symmetrical Output Impedance (I_{OH} = I_{OL} = 2 mA)
- Chip Complexity: < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
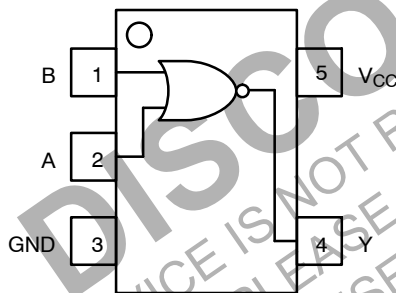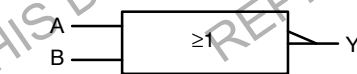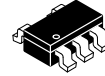- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAMS

SC−88A
DF SUFFIX
CASE 419A

TSOP−5
DT SUFFIX
CASE 483
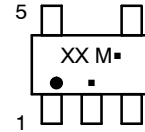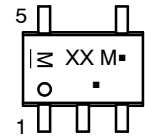
XX = Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)
*Date Code orientation and/or position may vary depending upon manufacturing location.

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	L
H	L	L
H	H	L

Figure 1. Pinout

Figure 2. Logic Symbol

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

PIN ASSIGNMENT	
1	B
2	A
3	GND
4	Y
5	V_{CC}

NLV74HC1G02

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V$_{CC}$	DC Supply Voltage		−0.5 to +7.0	V
V$_{IN}$	DC Input Voltage		−0.5 to V$_{CC}$ +0.5	V
V$_{OUT}$	DC Output Voltage		−0.5 to V$_{CC}$ +0.5	V
I$_{IK}$	DC Input Diode Current		±20	mA
I$_{OK}$	DC Output Diode Current		±20	mA
I$_{OUT}$	DC Output Source/Sink Current		±12.5	mA
I$_{CC}$ or I$_{GND}$	DC Supply Current per Supply Pin or Ground Pin		±25	mA
T$_{STG}$	Storage Temperature Range		−65 to +150	°C
T$_L$	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T$_J$	Junction Temperature Under Bias		+150	°C
θ$_{JA}$	Thermal Resistance (Note 1)	SC−88A	377	°C/W
P$_D$	Power Dissipation in Still Air at 85°C	SC−88A	332	mW
MSL	Moisture Sensitivity		Level 1	
F$_R$	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V$_{ESD}$	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	2000 1000	V
I$_{LATCHUP}$	Latchup Performance (Note 3)		±500	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 20 ounce copper trace with no air flow per JESD51−7.
2. HBM tested to ANSI/ESDA/JEDEC JS−001−2017. CDM tested to JESD22−C101−F. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued per JEDEC/JEP172A.
3. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V$_{CC}$	DC Supply Voltage		2.0	6.0	V
V$_{IN}$	DC Input Voltage		0.0	V$_{CC}$	V
V$_{OUT}$	DC Output Voltage		0.0	V$_{CC}$	V
T$_A$	Operating Temperature Range		−55	+125	°C
t$_r$, t$_f$	Input Rise and Fall Time	V$_{CC}$ = 2.0 V V$_{CC}$ = 3.0 V V$_{CC}$ = 4.5 V V$_{CC}$ = 6.0 V	0 0 0 0	1000 600 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# NLV74HC1G02

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V$_{CC}$ (V)	T$_A$ = 25°C Min	T$_A$ = 25°C Typ	T$_A$ = 25°C Max	−40°C ≤ T$_A$ ≤ 85°C Min	−40°C ≤ T$_A$ ≤ 85°C Max	−55°C ≤ T$_A$ ≤ 125°C Min	−55°C ≤ T$_A$ ≤ 125°C Max	Unit
V$_{IH}$	High−Level Input Voltage		2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.20	– – – –	– – – –	1.5 2.1 3.15 4.20	– – – –	1.5 2.1 3.15 4.20	– – – –	V
V$_{IL}$	Low−Level Input Voltage		2.0 3.0 4.5 6.0	– – – –	– – – –	0.5 0.9 1.35 1.80	– – – –	0.5 0.9 1.35 1.80	– – – –	0.5 0.9 1.35 1.80	V
V$_{OH}$	High−Level Output Voltage	V$_{IN}$ = V$_{IH}$ or V$_{IL}$ I$_{OH}$ = −20 μA	2.0 3.0 4.5 6.0	1.9 2.9 4.4 5.9	2.0 3.0 4.5 6.0	– – – –	1.9 2.9 4.4 5.9	– – – –	1.9 2.9 4.4 5.9	– – – –	V
		V$_{IN}$ = V$_{IH}$ or V$_{IL}$ I$_{OH}$ = −2 mA I$_{OH}$ = −2.6 mA	4.5 6.0	4.18 5.68	4.31 5.80	– –	4.13 5.63	– –	4.08 5.58	– –	
V$_{OL}$	Low−Level Output Voltage	V$_{IN}$ = V$_{IH}$ or V$_{IL}$ I$_{OL}$ = 20 μA	2.0 3.0 4.5 6.0	– – – –	0.0 0.0 0.0 0.0	0.1 0.1 0.1 0.1	– – – –	0.1 0.1 0.1 0.1	– – – –	0.1 0.1 0.1 0.1	V
		V$_{IN}$ = V$_{IH}$ or V$_{IL}$ I$_{OL}$ = 2 mA I$_{OL}$ = 2.6 mA	4.5 6.0	– –	0.17 0.18	0.26 0.26	– –	0.33 0.33	– –	0.40 0.40	
I$_{IN}$	Input Leakage Current	V$_{IN}$ = 6.0 V or GND	6.0	–	–	± 0.1	–	± 1.0	–	± 1.0	μA
I$_{CC}$	Quiescent Supply Current	V$_{IN}$ = V$_{CC}$ or GND	6.0	–	–	1.0	–	10	–	40	μA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	T$_A$ = 25°C Min	T$_A$ = 25°C Typ	T$_A$ = 25°C Max	−40°C ≤ T$_A$ ≤ 85°C Min	−40°C ≤ T$_A$ ≤ 85°C Max	−55°C ≤ T$_A$ ≤ 125°C Min	−55°C ≤ T$_A$ ≤ 125°C Max	Unit
t$_{PLH}$, t$_{PHL}$	Propagation Delay, (A or B) to Y	V$_{CC}$ = 5.0 V C$_L$ = 15 pF	–	3.5	15	–	20	–	25	ns
		V$_{CC}$ = 2.0 V C$_L$ = 50 pF V$_{CC}$ = 3.0 V V$_{CC}$ = 4.5 V V$_{CC}$ = 6.0 V	– – – –	20 11 8 7	100 27 20 17	– – – –	125 35 25 21	– – – –	155 90 35 26	
t$_{TLH}$, t$_{THL}$	Output Transition Time	V$_{CC}$ = 5.0 V C$_L$ = 15 pF	–	3	10	–	15	–	20	ns
		V$_{CC}$ = 2.0 V C$_L$ = 50 pF V$_{CC}$ = 3.0 V V$_{CC}$ = 4.5 V V$_{CC}$ = 6.0 V	– – – –	25 16 11 9	125 35 25 21	– – – –	155 45 31 26	– – – –	200 60 38 32	
C$_{IN}$	Input Capacitance		–	5	10	–	10	–	10	pF

		Typical @ 25°C, V$_{CC}$ = 5.0 V	
C$_{PD}$	Power Dissipation Capacitance (Note 4)	10	pF

4. C$_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I$_{CC(OPR)}$ = C$_{PD}$ • V$_{CC}$ • f$_{in}$ + I$_{CC}$. C$_{PD}$ is used to determine the no−load dynamic power consumption; P$_D$ = C$_{PD}$ • V$_{CC}^2$ • f$_{in}$ + I$_{CC}$ • V$_{CC}$.
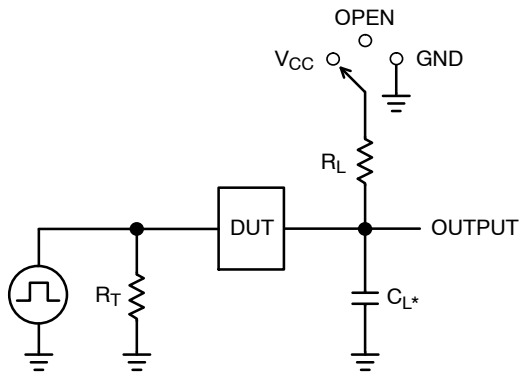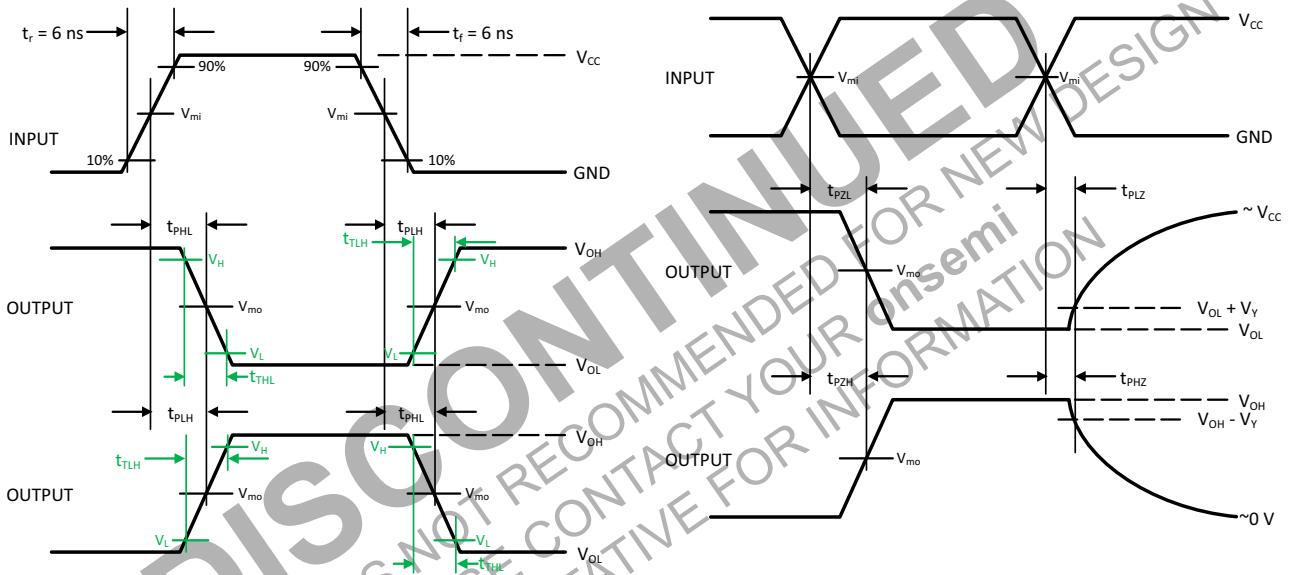
*C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 W)
f = 1 MHz

Figure 3. Test Circuit

Test	Switch Position	C_L, pF	R_L, Ω
t_{PLH} / t_{PHL}	Open		X
t_{TLH} / t_{THL} (Note 5)	Open	See AC Characteristics Table	X
t_{PLZ} / t_{PZL}	V_{CC}		1 k
t_{PHZ} / t_{PZH}	GND		1 k

X – Don't Care

Figure 4. Switching Waveforms

V_{CC}, V	V_{mi}, V	V_{mo}, V		V_L, V	V_H, V	V_Y, V
		t_{PLH}, t_{PHL}	t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}			
3.0 to 3.6	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	V_{OL} + 0.1 (V_{OH} − V_{OL})	V_{OL} + 0.9 (V_{OH} − V_{OL})	0.3
4.5 to 5.5	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	V_{OL} + 0.1 (V_{OH} − V_{OL})	V_{OL} + 0.9 (V_{OH} − V_{OL})	0.3

5. t_{TLH} and t_{THL} are measured from 10% to 90% of (V_{OH} − V_{OL}), and 90% to 10% of (V_{OH} − V_{OL}), respectively.

NLV74HC1G02

ORDERING INFORMATION

Device	Packages	Specific Device Code	Pin 1 Orientation (See below)	Shipping†
NLVHC1G02DFT2G*	SC−88A	H3	Q4	3000 / Tape & Reel
MC74HC1G02DTT1G	TSOP−5	H3	Q4	3000 / Tape & Reel

†For complete information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel
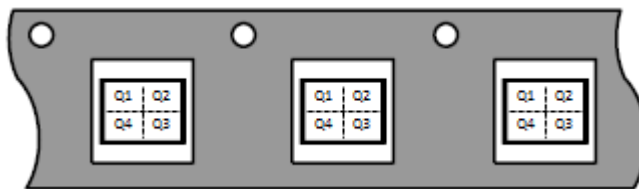
SCALE 2:1

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE M

DATE 11 APR 2023
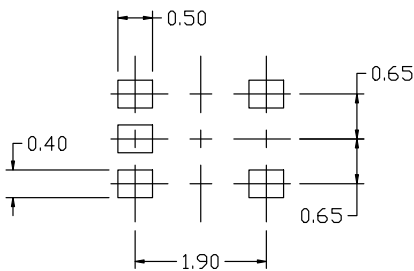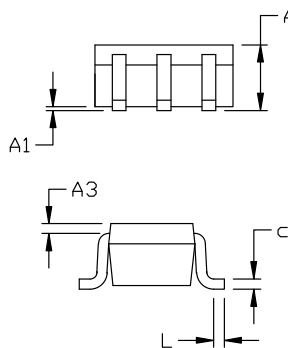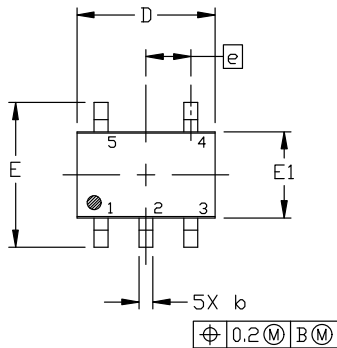
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30
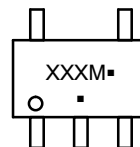
5X b

⊕ 0.2 Ⓜ B Ⓜ

RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXM▪

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

**TSOP−5 3.00x1.50x0.95, 0.95P**
CASE 483
ISSUE P

DATE 01 APR 2024
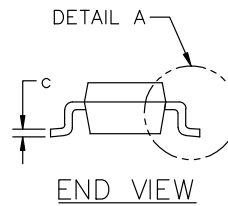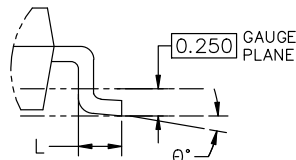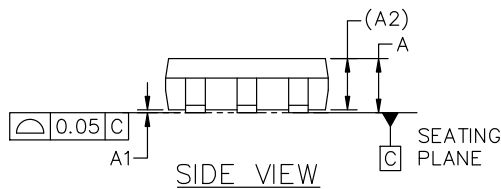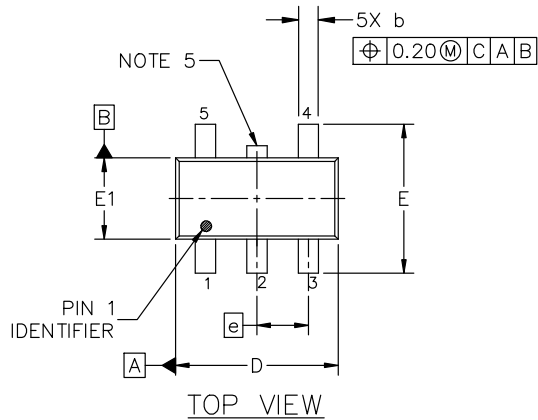
NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

5X b

⊕ | 0.20 Ⓜ | C | A | B

NOTE 5

B

5   4

E1   E

PIN 1
IDENTIFIER

1   2   3

e

A   D

TOP VIEW

(A2)
A

□ | 0.05 | C

A1

SIDE VIEW

SEATING
PLANE
C

DETAIL A

c

END VIEW

0.250 GAUGE PLANE

L   θ°

DETAIL "A"
SCALE 2:1

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2	0.950 REF.		
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e	0.950 BSC		
L	0.200	0.400	0.600
θ	0°	5°	10°

**GENERIC
MARKING DIAGRAM***

5

XXXAYW▪

1

Analog

5

XXX M▪

1

Discrete/Logic
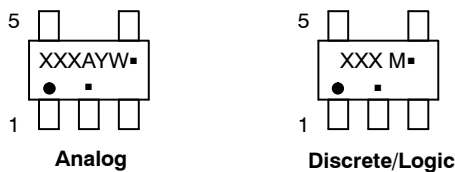
XXX = Specific Device Code
A   = Assembly Location
Y   = Year
W   = Work Week
▪   = Pb−Free Package

XXX = Specific Device Code
M   = Date Code
▪   = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

1.900

0.950

2.400

1.000

0.700

RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	98ARB18753C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	TSOP−5 3.00x1.50x0.95, 0.95P		PAGE 1 OF 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

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