Single 2-Input NAND Gate

NLV74VHC1G00, NLV74VHC1GT00

The NLV74VHC1G00 / NLV74VHC1GT00 is a 2−input NAND gate in tiny footprint packages. The NLV74VHC1G00 has CMOS−level input thresholds while the NLV74VHC1GT00 has TTL−level input thresholds.

The input structures provide protection when voltages up to 5.5 V are applied, regardless of the supply voltage. This allows the device to be used to interface 5 V circuits to 3 V circuits. Some output structures also provide protection when V_{CC} = 0 V and when the output voltage exceeds V_{CC}. These input and output structures help prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- Designed for 2.0 V to 5.5 V V_{CC} Operation
- 3.5 ns t_{PD} at 5 V (typ)
- Inputs/Outputs Over−Voltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Source/Sink 8 mA at 3.0 V
- Available in SC−88A, TSOP−5, and SOT−953 Packages
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant
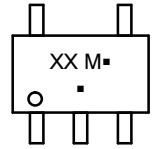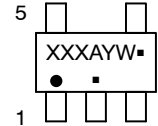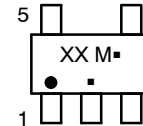

Figure 1. Logic Symbol

MARKING DIAGRAMS
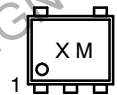

SC−88A
DF SUFFIX
CASE 419A

TSOP−5
DT SUFFIX
CASE 483

SOT−953
P5 SUFFIX
CASE 527AE

XX = Specific Device Code
M = Date Code*
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 7 of this data sheet.
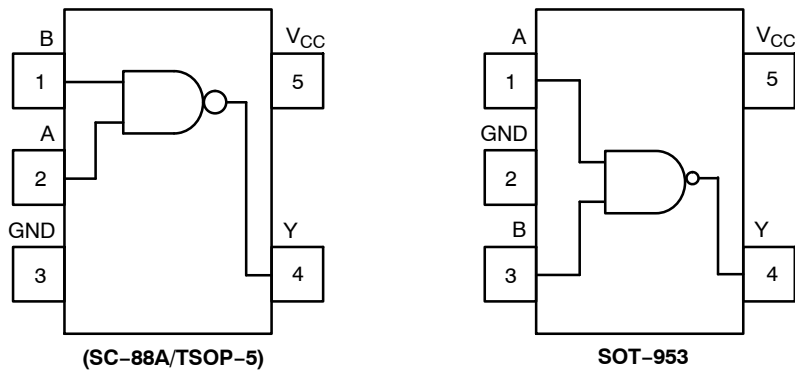
NLV74VHC1G00, NLV74VHC1GT00

Figure 2. Pinout (Top View)

PIN ASSIGNMENT
(SC−88A/TSOP−5)

Pin	Function
1	B
2	A
3	GND
4	Y
5	V$_{CC}$

PIN ASSIGNMENT (SOT−953)

Pin	Function
1	A
2	GND
3	B
4	Y
5	V$_{CC}$

FUNCTION TABLE

Input		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

NLV74VHC1G00, NLV74VHC1GT00

MAXIMUM RATINGS

Symbol	Characteristics		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	DC Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage	1Gxx	−0.5 to V_{CC} + 0.5	V
		1GTxx Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +7.0 −0.5 to +7.0	
I_{IK}	DC Input Diode Current	V_{IN} < GND	−20	mA
I_{OK}	DC Output Diode Current	1Gxx V_{OUT} > V_{CC}, V_{OUT} < GND	±20	mA
		1GTxx V_{OUT} < GND	−20	
I_{OUT}	DC Output Source/Sink Current		±25	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SC−88A TSOP−5 SOT−953	377 320 254	°C/W
P_D	Power Dissipation in Still Air	SC−88A TSOP−5 SOT−953	332 390 491	mW
MSL	Moisture Sensitivity		Level 1	−
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	−
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 1000	V
$I_{Latchup}$	Latchup Performance (Note 4)		± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 10mm−by−1inch, 2 ounce copper trace no air flow per JESD51−7.
3. HBM tested to ANSI/ESDA/JEDEC JS−001−2017. CDM tested to EIA/JESD22−C101−F. JEDEC recommends that ESD qualification to EIA/JESD22−A115−A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage	1Gxx	0	V_{CC}	V
		1GTxx Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	0 0 0	V_{CC} 5.5 5.5	
T_A	Operating Temperature Range		−55	+125	°C
t_r , t_f	Input Rise and Fall Time	V_{CC} = 3.0 V to 3.6 V V_{CC} = 4.5 V to 5.5 V	0 0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NLV74VHC1G00, NLV74VHC1GT00

DC ELECTRICAL CHARACTERISTICS (NLV74VHC1G00)

Symbol	Parameter	Test Conditions	V_{CC} (V)	$T_A = 25°C$ Min	Typ	Max	$-40°C \leq T_A \leq 85°C$ Min	Max	$-55°C \leq T_A \leq 125°C$ Min	Max	Unit
V_{IH}	High−Level Input Voltage		2.0	1.5	–	–	1.5	–	1.5	–	V
			3.0	2.1	–	–	2.1	–	2.1	–	
			4.5	3.15	–	–	3.15	–	3.15	–	
			5.5	3.85	–	–	3.85	–	3.85	–	
V_{IL}	Low−Level Input Voltage		2.0	–	–	0.5	–	0.5	–	0.5	V
			3.0	–	–	0.9	–	0.9	–	0.9	
			4.5	–	–	1.35	–	1.35	–	1.35	
			5.5	–	–	1.65	–	1.65	–	1.65	
V_{OH}	High−Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50$ μA $I_{OH} = -50$ μA $I_{OH} = -50$ μA $I_{OH} = -4$ mA $I_{OH} = -8$ mA	2.0 3.0 4.5 3.0 4.5	1.9 2.9 4.4 2.58 3.94	2.0 3.0 4.5 – –	– – – – –	1.9 2.9 4.4 2.48 3.80	– – – – –	1.9 2.9 4.4 2.34 3.66	– – – – –	V
V_{OL}	Low−Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50$ μA $I_{OL} = 50$ μA $I_{OL} = 50$ μA $I_{OL} = 4$ mA $I_{OL} = 8$ mA	2.0 3.0 4.5 3.0 4.5	– – – – –	0.0 0.0 0.0 – –	0.1 0.1 0.1 0.36 0.36	– – – – –	0.1 0.1 0.1 0.44 0.44	– – – – –	0.1 0.1 0.1 0.52 0.52	V
I_{IN}	Input Leakage Current	$V_{IN} = 5.5$ V or GND	2.0 to 5.5	–	–	±0.1	–	±1.0	–	± 1.0	μA
I_{OFF}	Power Off Leakage Current	$V_{IN} = 5.5$ V	0.0	–	–	1.0	–	10	–	10	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5	–	–	1.0	–	20	–	40	μA

DC ELECTRICAL CHARACTERISTICS (NLV74VHC1GT00)

Symbol	Parameter	Test Conditions	V_{CC} (V)	$T_A = 25°C$ Min	Typ	Max	$-40°C \leq T_A \leq 85°C$ Min	Max	$-55°C \leq T_A \leq 125°C$ Min	Max	Unit
V_{IH}	High–Level Input Voltage		2.0	1.0	–	–	1.0	–	1.0	–	V
			3.0	1.4	–	–	1.4	–	1.4	–	
			4.5	2.0	–	–	2.0	–	2.0	–	
			5.5	2.0	–	–	2.0	–	2.0	–	
V_{IL}	Low–Level Input Voltage		2.0	–	–	0.28	–	0.28	–	0.28	V
			3.0	–	–	0.45	–	0.45	–	0.45	
			4.5	–	–	0.8	–	0.8	–	0.8	
			5.5	–	–	0.8	–	0.8	–	0.8	
V_{OH}	High–Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 mA$ $I_{OH} = -8 mA$	2.0 3.0 4.5 3.0 4.5	1.9 2.9 4.4 2.58 3.94	2.0 3.0 4.5 – –	– – – – –	1.9 2.9 4.4 2.48 3.80	– – – – –	1.9 2.9 4.4 2.34 3.66	– – – – –	V
V_{OL}	Low–Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50 \mu A$ $I_{OL} = 50 \mu A$ $I_{OL} = 50 \mu A$ $I_{OL} = 4 mA$ $I_{OL} = 8 mA$	2.0 3.0 4.5 3.0 4.5	– – – – –	0.0 0.0 0.0 – –	0.1 0.1 0.1 0.36 0.36	– – – – –	0.1 0.1 0.1 0.44 0.44	– – – – –	0.1 0.1 0.1 0.52 0.52	V
I_{IN}	Input Leakage Current	$V_{IN} = 5.5$ V or GND	2.0 to 5.5	–	–	±0.1	–	±1.0	–	± 1.0	μA
I_{OFF}	Power Off Leakage Current	$V_{IN} = 5.5$ V or $V_{OUT} = 5.5$ V	0	–	–	1.0	–	10	–	10	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5	–	–	1.0	–	20	–	40	μA
I_{CCT}	Increase in Quiescent Supply Current per Input Pin	One Input: V_{IN} = 3.4 V; Other Input at V_{CC} or GND	5.5	–	–	1.35	–	1.5	–	1.65	mA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Min	Typ	Max	$-40°C \leq T_A \leq 85°C$ Min	Max	$-55°C \leq T_A \leq 125°C$ Min	Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay, (A or B) to Y (Figures 3 and 4)	$C_L = 15$ pF	3.0 to 3.6	–	4.5	7.9	–	9.5	–	11.0	ns
		$C_L = 50$ pF		–	5.6	11.4	–	13.0	–	15.5	
		$C_L = 15$ pF	4.5 to 5.5	–	3.0	5.5	–	6.5	–	8.0	
		$C_L = 50$ pF		–	3.8	7.5	–	8.5	–	10.0	
C_{IN}	Input Capacitance			–	4.0	10	–	10	–	10	pF
C_{OUT}	Output Capacitance	Output in High Impedance State		–	6.0	–	–	–	–	–	pF

			Typical @ 25°C, $V_{CC} = 5.0$ V	
C_{PD}	Power Dissipation Capacitance (Note 5)		8.0	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.
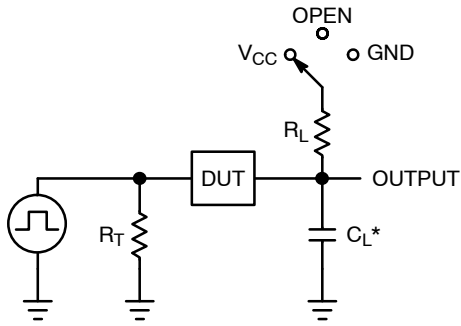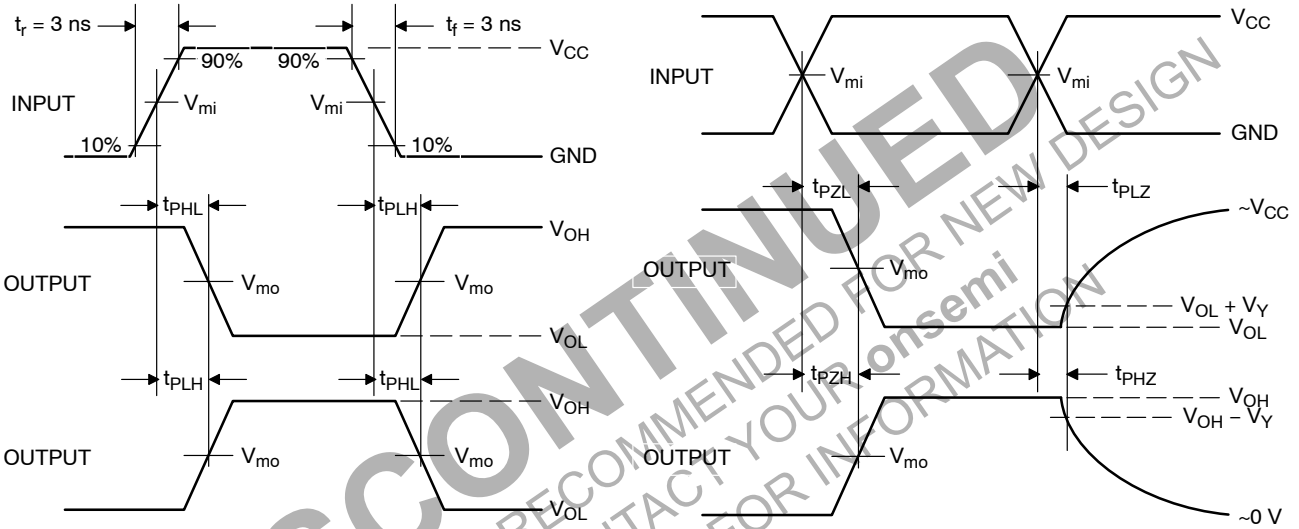
C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Figure 3. Test Circuit

Test	Switch Position	C_L, pF	R_L, Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table	X
t_{PLZ} / t_{PZL}	V_{CC}		1 k
t_{PHZ} / t_{PZH}	GND		1 k

X = Don't Care

Figure 4. Switching Waveforms

V_{CC}, V	V_{mi}, V	V_{mo}, V		V_Y, V
		t_{PLH}, t_{PHL}	t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}	
3.0 to 3.6	V_{CC}/2	V_{CC}/2	V_{CC}/2	0.3
4.5 to 5.5	V_{CC}/2	V_{CC}/2	V_{CC}/2	0.3

NLV74VHC1G00, NLV74VHC1GT00

ORDERING INFORMATION

Device	Packages	Specific Device Code	Pin 1 Orientation (See below)	Shipping†
MC74VHC1G00DFT2G−L22038	SC−88A	V1	Q4	3000 / Tape & Reel
NLVVHC1G00DFT1G*	SC−88A	V1	Q2	3000 / Tape & Reel
NLVVHC1G00DFT2G*	SC−88A	V1	Q4	3000 / Tape & Reel
M74VHC1GT00DFT1G−L22038	SC−88A	VH	Q2	3000 / Tape & Reel
M74VHC1GT00DFT2G−L22038	SC−88A	VH	Q4	3000 / Tape & Reel
NLVVHC1GT00DFT2G*	SC−88A	VH	Q4	3000 / Tape & Reel
MC74VHC1G00DTT1G	TSOP−5	V1	Q4	3000 / Tape & Reel
NLVVHC1G00DTT1G*	TSOP−5	V1	Q4	3000 / Tape & Reel
M74VHC1GT00DTT1G	TSOP−5	VH	Q4	3000 / Tape & Reel
MC74VHC1G00P5T5G−L22088	SOT−953	A	Q2	8000 / Tape & Reel
MC74VHC1GT00P5T5G−L22088	SOT−953	K	Q2	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel
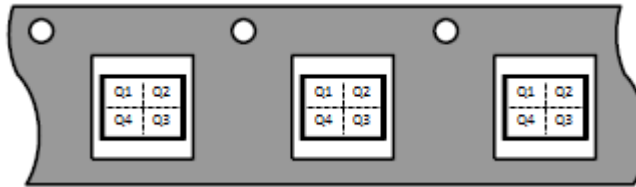
SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE M

DATE 11 APR 2023

SCALE 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

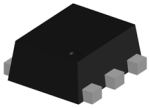| DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30
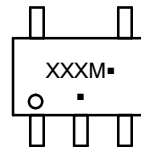
RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXM∎

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "∎", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code
M = Date Code
∎ = Pb−Free Package

(Note: Microdot may be in either location)

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

DOCUMENT NUMBER:	98ASB42984B	
DESCRIPTION:	SC−88A (SC−70−5/SOT−353)	PAGE 1 OF 1

TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

DATE 01 APR 2024
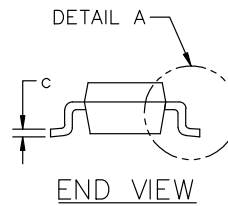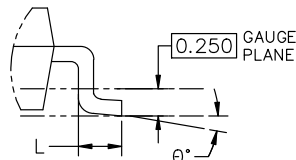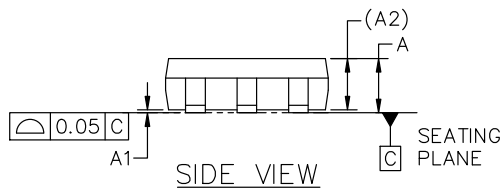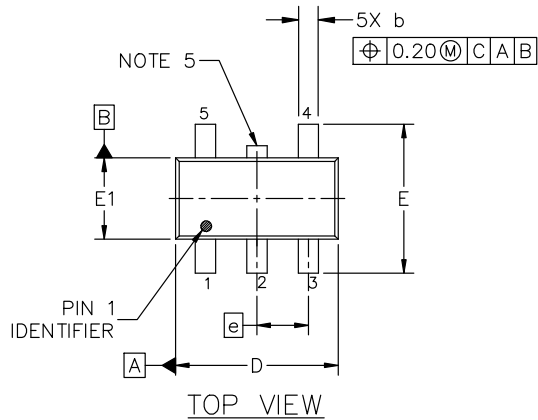
NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

TOP VIEW

SIDE VIEW

DETAIL "A"
SCALE 2:1

END VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2	0.950 REF.		
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e	0.950 BSC		
L	0.200	0.400	0.600
θ	0°	5°	10°

GENERIC MARKING DIAGRAM*

XXXAYW▪
Analog

XXX M▪
Discrete/Logic

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED MOUNTING FOOTPRINT*

1.900
0.950
2.400
1.000
0.700

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	98ARB18753C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	TSOP−5 3.00x1.50x0.95, 0.95P		PAGE 1 OF 1

SOT−953 1.00x0.80x0.37, 0.35P
CASE 527AE
ISSUE F

DATE 17 JAN 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
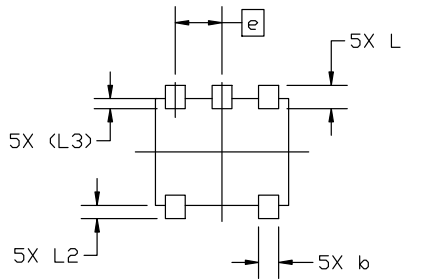4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H	0.95	1.00	1.05
L	0.125	0.175	0.225
L2	0.05	0.10	0.15
L3	0.075 (REF)		

TOP VIEW

PIN 1 INDICATOR
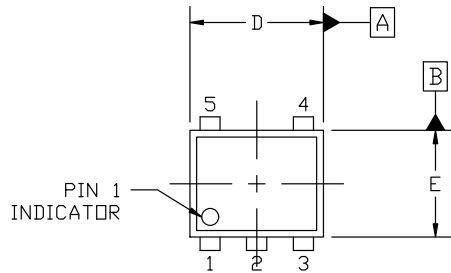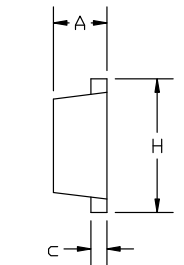
SIDE VIEW

BOTTOM VIEW
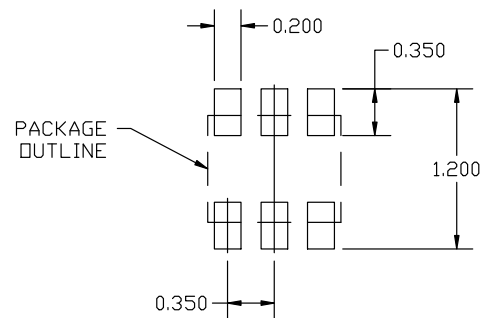
5X L
5X (L3)
5X L2
5X b

⊕ | 0.08 | A | B

RECOMMENDED MOUNTING FOOTPRINT

PACKAGE OUTLINE

0.200
0.350
1.200
0.350

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XM
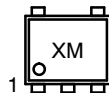
X = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON26457D	
DESCRIPTION:	SOT−953 1.00x0.80x0.37, 0.35P	PAGE 1 OF 9

ADDITIONAL INFORMATION

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