# Configurable Multifunction Gate

# NLV7SZ97

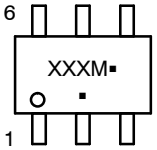
The NLV7SZ97 is an advanced high−speed CMOS multifunction gate. The device allows the user to choose logic functions MUX, AND, OR, NAND, NOR, INVERT and BUFFER. The device has Schmitt−trigger inputs, thereby enhancing noise immunity.

### Features

- Designed for 1.65 V to 5.5 V $V_{CC}$ Operation
- 3.3 ns $t_{PD}$ at $V_{CC}$ = 5 V (Typ)
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- $I_{OFF}$ Supports Partial Power Down Protection
- Sink 24 mA at 3.0 V
- Available in SC−88 Package
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### MARKING DIAGRAMS


SC−88/SC70−6/
SOT−363
CASE 419B−02



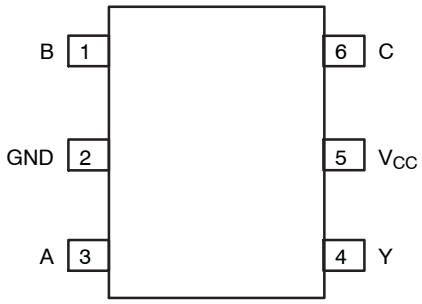

XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location or may not be present)

*Date Code orientation and/or position may vary depending upon manufacturing location.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.




(SC−88)

**Figure 1. Pinout (Top View)**

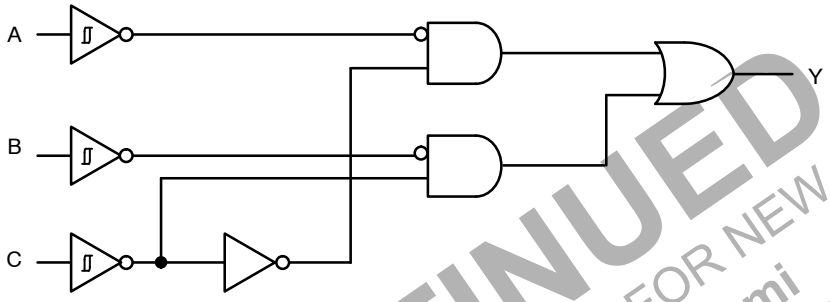



**Figure 2. Function Diagram**



**PIN ASSIGNMENT**

| Pin | Function |
|---|---|
| 1 | B |
| 2 | GND |
| 3 | A |
| 4 | Y |
| 5 | $V_{CC}$ |
| 6 | C |

**FUNCTION TABLE***

| Input | | | Output |
|---|---|---|---|
| A | B | C | Y |
| L | L | L | L |
| L | L | H | L |
| L | H | L | H |
| L | H | H | L |
| H | L | L | L |
| H | L | H | H |
| H | H | L | H |
| H | H | H | H |

*To select a logic function, please refer to “Logic Configurations section”.

## LOGIC CONFIGURATIONS

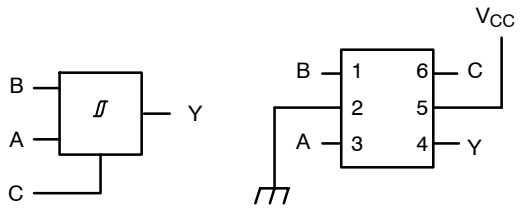



**Figure 3. 2−Input MUX**

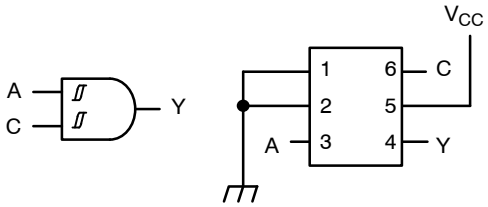



**Figure 4. 2−Input AND (When B = “L”)**

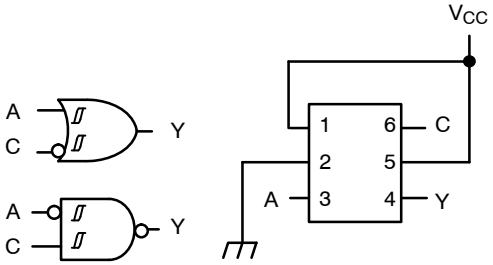



**Figure 5. 2−Input OR with Input C Inverted (When B = “H”)**

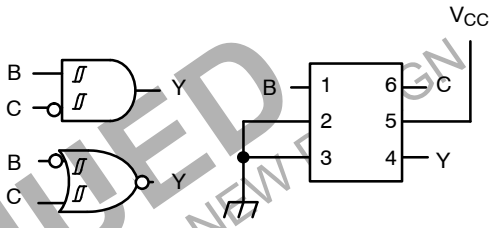



**Figure 6. 2−Input AND with Input C Inverted (When A = “L”)**

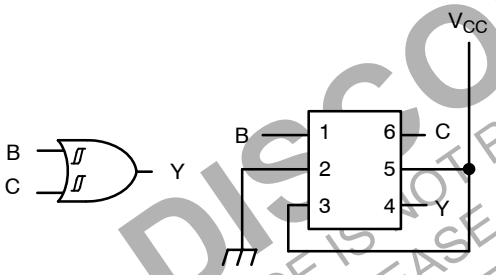



**Figure 7. 2−Input OR (When A =”H”)**

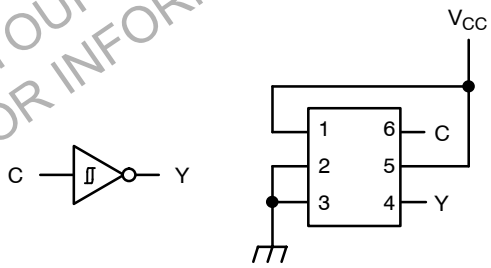



**Figure 8. Inverter (When A = “L” and B = “H”)**

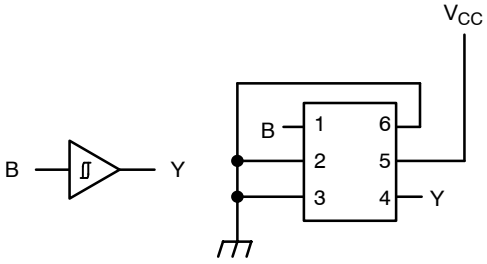



**Figure 9. Buffer (When A = C = “L”)**

## MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +7.0 | V |
| $V_{IN}$ | DC Input Voltage | | −0.5 to +7.0 | V |
| $V_{OUT}$ | DC Output Voltage | Active−Mode (High or Low State)<br>Tri−State Mode (Note 1)<br>Power−Down Mode ($V_{CC}$ = 0 V) | −0.5 to $V_{CC}$ + 0.5<br>−0.5 to +7.0<br>−0.5 to +7.0 | V |
| $I_{IK}$ | DC Input Diode Current | $V_{IN}$ < GND | −50 | mA |
| $I_{OK}$ | DC Output Diode Current | $V_{OUT}$ < GND | −50 | mA |
| $I_{OUT}$ | DC Output Source/Sink Current | | ±50 | mA |
| $I_{CC}$ or $I_{GND}$ | DC Supply Current per Supply Pin or Ground Pin | | ±100 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Secs | | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Note 2) | SC−88 | 377 | °C/W |
| $P_D$ | Power Dissipation in Still Air | SC−88 | 332 | mW |
| MSL | Moisture Sensitivity | | Level 1 | |
| $F_R$ | Flammability Rating Oxygen | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in | |
| $V_{ESD}$ | ESD Withstand Voltage (Note 3) | Human Body Mode<br>Charged Device Model | >2000<br>N/A | V |
| $I_{LATCHUP}$ | Latchup Performance (Note 4) | | ±500 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow per JESD51−7.
3. CDM tested to EIA/JESD22−C101−F. JEDEC recommends that ESD qualification to EIA/JESD22−A115−A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.



## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive DC Supply Voltage | | 1.65 | 5.5 | V |
| $V_{IN}$ | DC Input Voltage | | 0 | 5.5 | V |
| $V_{OUT}$ | DC Output Voltage | Active−Mode (High or Low State)<br>Tri−State Mode (Note 1)<br>Power−Down Mode ($V_{CC}$ = 0 V) | 0<br>0<br>0 | $V_{CC}$<br>5.5<br>5.5 | V |
| $T_A$ | Operating Free−Air Temperature | | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise or Fall Rate | $V_{CC}$ = 1.65 V to 1.95 V<br>$V_{CC}$ = 2.3 V to 2.7 V<br>$V_{CC}$ = 3.0 V to 3.6 V<br>$V_{CC}$ = 4.5 V to 5.5 V | 0<br>0<br>0<br>0 | No Limit<br>No Limit<br>No Limit<br>No Limit | nS/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Condition | $V_{CC}$ (V) | $T_A$ = 25°C | | | −40°C ≤ $T_A$ ≤ 85°C | | −55°C ≤ $T_A$ ≤ 125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| $V_{T+}$ | Positive Input Threshold Voltage | | 1.65 | 0.79 | – | 1.16 | – | 1.16 | – | 1.16 | V |
| | | | 2.3 | 1.11 | – | 1.56 | – | 1.56 | – | 1.56 | |
| | | | 3.0 | 1.5 | – | 1.87 | – | 1.87 | – | 1.87 | |
| | | | 4.5 | 2.16 | – | 2.74 | – | 2.74 | – | 2.74 | |
| | | | 5.5 | 2.61 | – | 3.33 | – | 3.33 | – | 3.33 | |
| $V_{T-}$ | Negative Input Threshold Voltage | | 1.65 | 0.35 | – | 0.62 | 0.35 | – | 0.35 | – | V |
| | | | 2.3 | 0.58 | – | 0.87 | 0.58 | – | 0.58 | – | |
| | | | 3.0 | 0.84 | – | 1.19 | 0.84 | – | 0.84 | – | |
| | | | 4.5 | 1.41 | – | 1.9 | 1.41 | – | 1.41 | – | |
| | | | 5.5 | 1.78 | – | 2.2 | 1.78 | – | 1.78 | – | |
| $V_H$ | Negative Input Threshold Voltage | | 1.65 | 0.3 | – | 0.62 | 0.3 | 0.62 | 0.3 | 0.62 | V |
| | | | 2.3 | 0.4 | – | 0.8 | 0.4 | 0.8 | 0.4 | 0.8 | |
| | | | 3.0 | 0.53 | – | 0.87 | 0.53 | 0.87 | 0.53 | 0.87 | |
| | | | 4.5 | 0.71 | – | 1.04 | 0.71 | 1.04 | 0.71 | 1.04 | |
| | | | 5.5 | 0.8 | – | 1.2 | 0.8 | 1.2 | 0.8 | 1.2 | |
| $V_{OH}$ | High−Level Output Voltage<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −50 μA | 1.65 to 5.5 | $V_{CC}$ − 0.1 | $V_{CC}$ | – | $V_{CC}$ − 0.1 | – | $V_{CC}$ − 0.1 | – | V |
| | | $I_{OH}$ = −4 mA | 1.65 | 1.20 | 1.52 | – | 1.20 | – | 1.20 | – | |
| | | $I_{OH}$ = −8 mA | 2.3 | 1.9 | 2.1 | – | 1.9 | – | 1.9 | – | |
| | | $I_{OH}$ = −16 mA | 3 | 2.4 | 2.7 | – | 2.4 | – | 2.4 | – | |
| | | $I_{OH}$ = −24 mA | 3 | 2.3 | 2.5 | – | 2.3 | – | 2.3 | – | |
| | | $I_{OH}$ = −32 mA | 4.5 | 3.8 | 4 | – | 3.8 | – | 3.8 | – | |
| $V_{OL}$ | Low−Level Output Voltage<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 100 μA | 1.65 to 5.5 | – | – | 0.1 | – | 0.1 | – | 0.1 | V |
| | | $I_{OL}$ = 4 mA | 1.65 | – | 0.08 | 0.45 | – | 0.45 | – | 0.45 | |
| | | $I_{OL}$ = 8 mA | 2.3 | – | 0.2 | 0.3 | – | 0.3 | – | 0.4 | |
| | | $I_{OL}$ = 16 mA | 3 | – | 0.28 | 0.4 | – | 0.4 | – | 0.5 | |
| | | $I_{OL}$ = 24 mA | 3 | – | 0.38 | 0.55 | – | 0.55 | – | 0.55 | |
| | | $I_{OL}$ = 32 mA | 4.5 | – | 0.42 | 0.55 | – | 0.55 | – | 0.65 | |
| $I_{IN}$ | Input Leakage Current | $V_{IN}$ = 5.5 V or GND | 1.65 to 5.5 | – | – | +0.1 | – | +1.0 | – | +1.0 | μA |
| $I_{OFF}$ | Power Off Leakage Current | $V_{IN}$ = 5.5 V or $V_{OUT}$ = 5.5 V | 0 | – | – | 1.0 | – | 10 | – | 10 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_{IN}$ = 5.5 V or GND | 5.5 | – | – | 1.0 | – | 10 | – | 10 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

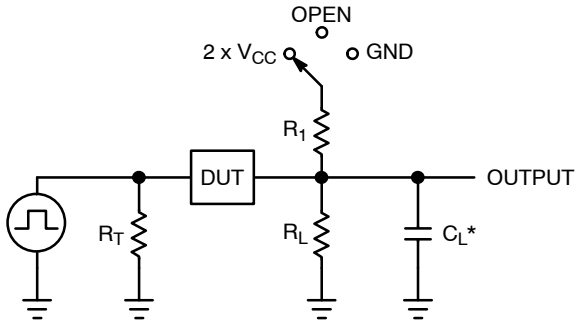
## AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Condition | $V_{CC}$ (V) | $T_A$ = 25°C | | | −40°C ≤ $T_A$ ≤ 85°C | | −55°C ≤ $T_A$ ≤ 125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay, (A or B or C) to Y (Figures 10 and 11) | $R_L$ = 1 kΩ, $C_L$ = 30 pF | 1.65 to 1.95 | – | 8.6 | 14.4 | – | 14.4 | – | 14.4 | ns |
| | | $R_L$ = 500 Ω, CL = 30 pF | 2.3 to 2.7 | – | 5.1 | 8.3 | – | 8.3 | – | 8.3 | |
| | | $R_L$ = 500 Ω, $C_L$ = 50 pF | 3.0 to 3.6 | – | 3.9 | 6.3 | – | 6.3 | – | 6.3 | |
| | | | 4.5 to 5.5 | – | 3.3 | 5.1 | – | 5.1 | – | 5.1 | |

## CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Condition | Typical | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = 5.5 V, $V_{IN}$ = 0 V or $V_{CC}$ | 2.5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{CC}$ = 5.5 V, $V_{IN}$ = 0 V or $V_{CC}$ | 4.0 | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Note 5) | 10 MHz, $V_{CC}$ = 3.3 V, $V_{IN}$ = 0 V or $V_{CC}$<br>10 MHz, $V_{CC}$ = 5.0 V, $V_{IN}$ = 0 V or $V_{CC}$ | 16<br>19.5 | pF |

5. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. $C_{PD}$ is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.




$C_L$ includes probe and jig capacitance
$R_T$ is $Z_{OUT}$ of pulse generator (typically 50 Ω)
f = 1 MHz

**Figure 10. Test Circuit**

| Test | Switch Position | $C_L$, pF | $R_L$, Ω | $R_1$, Ω |
|---|---|---|---|---|
| $t_{PLH}$ / $t_{PHL}$ | Open | See AC Characteristics Table | | |
| $t_{PLZ}$ / $t_{PZL}$ | 2 x $V_{CC}$ | 50 | 500 | 500 |
| $t_{PHZ}$ / $t_{PZH}$ | GND | 50 | 500 | 500 |

X = Don't Care

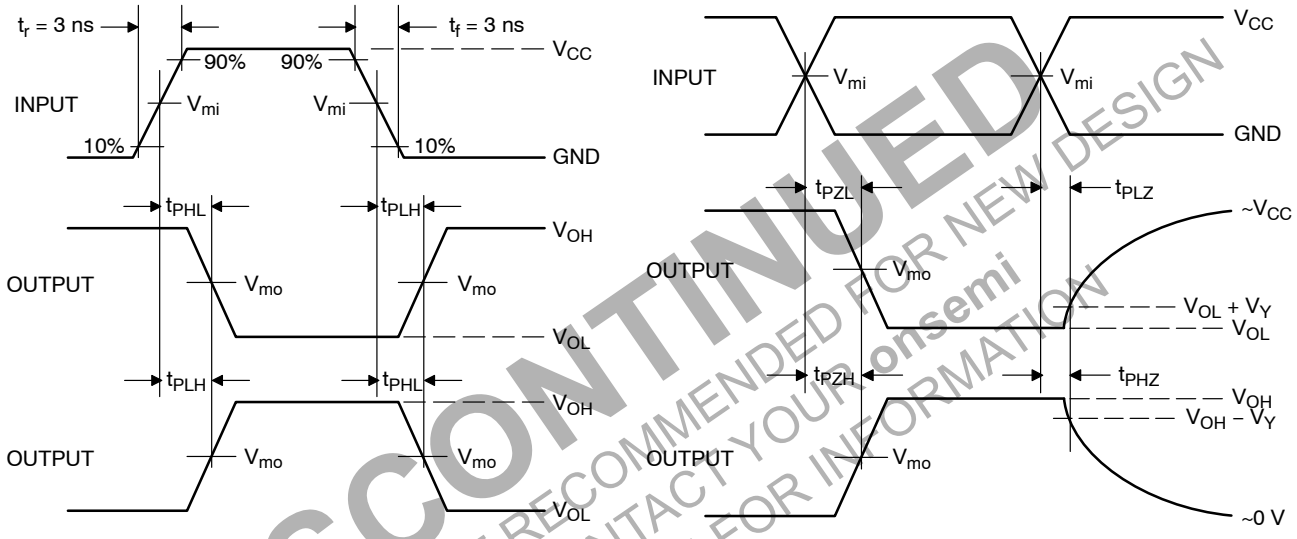



**Figure 11. Switching Waveforms**

| $V_{CC}$, V | $V_{mi}$, V | $V_{mo}$, V | | $V_Y$, V |
|---|---|---|---|---|
| | | $t_{PLH}$, $t_{PHL}$ | $t_{PZL}$, $t_{PLZ}$, $t_{PZH}$, $t_{PHZ}$ | |
| 1.65 to 1.95 | $V_{CC}$ / 2 | $V_{CC}$ / 2 | $V_{CC}$ / 2 | 0.15 |
| 2.3 to 2.7 | $V_{CC}$ / 2 | $V_{CC}$ / 2 | $V_{CC}$ / 2 | 0.15 |
| 3.0 to 3.6 | $V_{CC}$ / 2 | $V_{CC}$ / 2 | $V_{CC}$ / 2 | 0.3 |
| 4.5 to 5.5 | $V_{CC}$ / 2 | $V_{CC}$ / 2 | $V_{CC}$ / 2 | 0.3 |

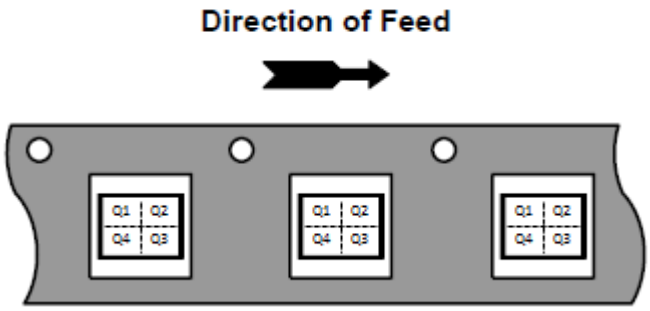
## DEVICE ORDERING INFORMATION

| Device | Package | Specific Device Code | Pin 1 Orientation (See below) | Shipping† |
|---|---|---|---|---|
| NLV7SZ97DFT2G* | SC−88 (Pb−Free) | MK | Q4 | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

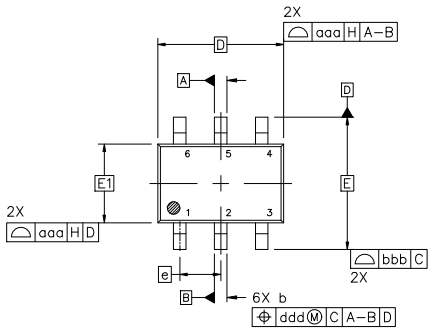
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

### Pin 1 Orientation in Tape and Reel

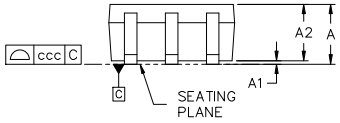


**SC−88 2.00x1.25x0.90, 0.65P**
CASE 419B−02
ISSUE Z

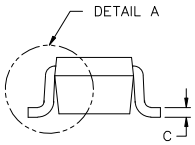
DATE 18 APR 2024



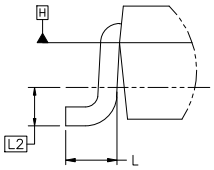

TOP VIEW




SIDE VIEW




END VIEW

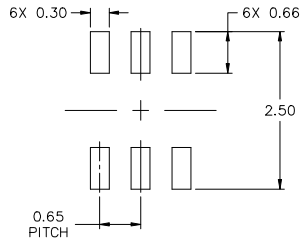



DETAIL A
SCALE 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

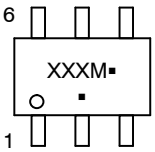
| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | −−− | −−− | 1.10 |
| A1 | 0.00 | −−− | 0.10 |
| A2 | 0.70 | 0.90 | 1.00 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.08 | 0.15 | 0.22 |
| D | 2.00 BSC | | |
| E | 2.10 BSC | | |
| E1 | 1.25 BSC | | |
| e | 0.65 BSC | | |
| L | 0.26 | 0.36 | 0.46 |
| L2 | 0.15 BSC | | |
| aaa | 0.15 | | |
| bbb | 0.30 | | |
| ccc | 0.10 | | |
| ddd | 0.10 | | |




RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***




XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

**SC−88 2.00x1.25x0.90, 0.65P**
CASE 419B−02
ISSUE Z

DATE 18 APR 2024

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales