National Semiconductor

June 1990

NM43256A
262 144-Bit CMOS Static RAM

General Description

The NM43256A is a high speed, low power, 32768 words by 8 bits CMOS static RAM fabricated with advanced silicon-gate CMOS technology. The NM43256A is a low standby power device using n-channel memory cell with polysilicon resistors. Furthermore, a novel circuit technique makes the NM43256A a high speed and low operating power device which requires no clocking or refreshing to operate.

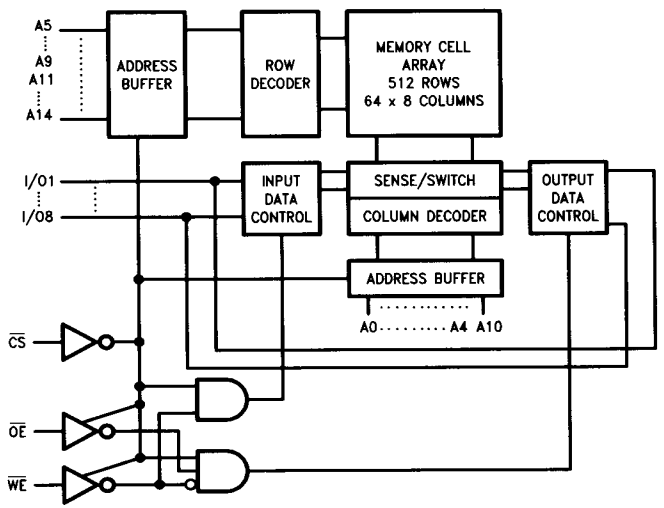
Minimum standby power is drawn by this device when $\overline{CS}$ is at a high level, independent of the other input levels.

Data retention is guaranteed at a power supply voltage as low as 2V. The NM43256AMX is packaged in TSOP (Thin Small Outline Package), supporting high density applications.

Features

- Single +5V supply
- Fully static operation: No clock or refresh required
- TTL compatible: All inputs and outputs
- Common I/O using TRI-STATE® output
- One chip select and one output enable inputs for easy application
- Fast access time:
  - — NM43256A-10 100 ns max.
  - — NM43256A-12 120 ns max.
  - — NM43256A-15 150 ns max.
- Low power dissipation:
  - — Standby supply current 2 μA typ.
  - — Data retention supply current 1 μA typ.
  - — Active 40 mA max.
  - — Standby NM43256AMX-10LL/12LL 50 μA max.
- Data retention voltage: 2 V_{min}

Block Diagram



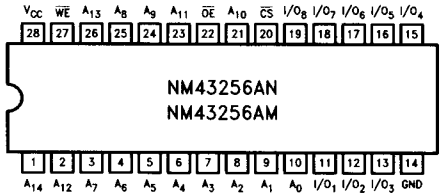
TL/D/10787–1

Truth Table

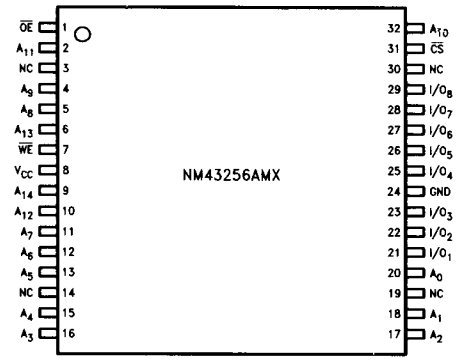
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	I_{CC}
H	X	X	Not Selected	HI-Z	Standby
L	H	H	Not Selected	HI-Z	Active
L	L	H	Read	D_{OUT}	Active
L	X	L	Write	D_{IN}	Active

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Pin Configuration



TL/D/10787-2



TL/D/10787-3

Pin Names

A_0 to A_{14}	Address Input
I/O_1 to I/O_8	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
GND	GND
NC	No Connection

Ordering Information

Part Number	Access Time Max.	Package Type	Note
NM43256AN-10	100 ns	28-Pin Plastic DIP (600 Mil)	
NM43256AN-12	120 ns		
NM43256AN-15	150 ns		
NM43256AN-10L	100 ns		L Version
NM43256AN-12L	120 ns		
NM43256AN-15L	150 ns		
NM43256AM-10L	100 ns	28-Pin Plastic SOP (450 Mil)	
NM43256AM-12L	120 ns		
NM43256AM-15L	150 ns		
NM43256AMX-10L	100 ns	32-Pin Plastic TSOP	L Version
NM43256AMX-12L	120 ns		
NM43256AMX-10LL	100 ns		LL Version
NM43256AMX-12LL	120 ns		
NM43256AMXR-10L	100 ns	32-Pin Plastic TSOP (Reverse Bent)	L Version
NM43256AMXR-12L	120 ns		
NM43256AMXR-10LL	100 ns		LL Version
NM43256AMXR-12LL	120 ns		

Absolute Maximum Ratings*

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V** to +7.0V
Input or Output Voltage	−0.5V** to V_{CC} + 0.5V
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +125°C
Power Dissipation	1.0W

***Note:** Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

****Note:** −3.0 V_{min} (Pulse width 50 ns)

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage V_{CC}	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2		V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	−0.3**		0.8	V
T_A	Ambient Temperature	0		70	°C

** −3.0 V_{min} (Pulse width 50 ns).

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{LI}	Input Leakage Current	V_{IN} = 0 to V_{CC}	−1.0		1.0	μA
I_{LO}	I/O Leakage Current	$V_{\overline{CS}} = V_{IH}$ or $V_{\overline{OE}} = V_{IH}$ or $V_{\overline{WE}} = V_{IL}$, $I_{I/O}$ = 0 to V_{CC}	−1.0		1.0	μA
I_{CCA1}	Operating Supply Current	$V_{\overline{CS}} = V_{IL}$, Min Cycle, $I_{I/O}$ = 0			(Note 1)	mA
I_{CCA2}		$V_{\overline{CS}} = V_{IL}$, $I_{I/O}$ = 0			10	mA
I_{CCA3}		$V_{\overline{CS}} \leq 0.2V$, f = 1 MHz, $I_{I/O}$ = 0, $V_{IL} \leq 0.2V$, $V_{IH} \geq V_{CC} - 0.2V$			10	mA
I_{SB}	Standby Supply Current	$V_{\overline{CS}} = V_{IH}$			3	mA
I_{SB1}		$V_{\overline{CS}} \geq V_{CC} - 0.2V$		2	(Note 2)	μA
V_{OH1}	Output High Voltage	I_{OH} = −1.0 mA	2.4			V
V_{OH2}		I_{OH} = −0.1 mA	V_{CC} − 0.5			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V

Note 1: NM43256A-10 40 mA max.
NM43256A-12 40 mA max.
NM43256A-15 35 mA max.

Note 2: NM43256AN-10/-12/-15 2 mA max.
NM43256A-10L/-12L/-15L 100 μA max.
NM43256AMX-10LL/-12LL/-15LL 50 μA max.

Capacitance (T_A = 25°C, f = 1 MHz)

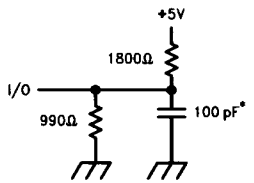
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V			5	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V			8	pF

Note: This parameter is periodically sampled and not 100% tested.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC TEST CONDITIONS

Input Pulse Levels	0.8V to 2.2V
Input Pulse Rise and Fall Time	5 ns
Timing Reference Levels	1.5V
Output Load: See *Figures 1, 2*	

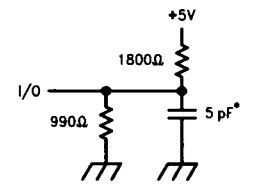


TL/D/10787–4

* . . . including scope and jig.

FIGURE 1

for t_{CHZ}, t_{OHZ}, t_{CLZ}, t_{OLZ}, t_{WHZ}, t_{OW}



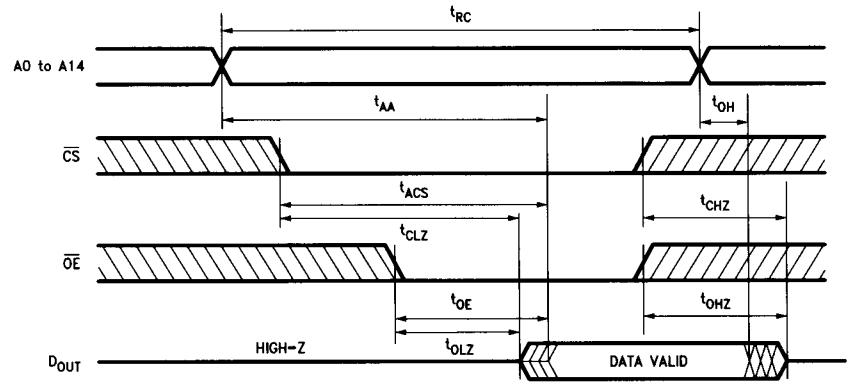
TL/D/10787–5

FIGURE 2

Read Cycle

Symbol	Parameter	NM43256AN-10/-10L NM43256AM-10L NM43256AMX-10L/-10LL		NM43256AN-12/-12L NM43256AM-12L NM43256AMX-12L/-12LL		NM43256AN-15/-15L NM43256AM-15L		Units
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	100		120		150		ns
t_{AA}	Address Access Time		100		120		150	ns
t_{ACS}	Chip Select Access Time		100		120		150	ns
t_{OE}	Output Enable to Output Valid		50		60		70	ns
t_{OH}	Output Hold from Address Change	10		10		10		ns
t_{CLZ}	Chip Select to Output in LO-Z	10		10		10		ns
t_{OLZ}	Output Enable to to Output in LO-Z	5		5		5		ns
t_{CHZ}	Chip Select to to Output in HI-Z		35		40		50	ns
t_{OHZ}	Output Enable to Output in HI-Z		35		40		50	ns

Read Cycle Timing Chart (Notes: 1, 2, 3)



TL/D/10787–6

Note 1: $\overline{WE}$ is high for read cycle.

Note 2: Device is continuously selected, $\overline{CS}$ = $\overline{OE}$ = V_{IL}.

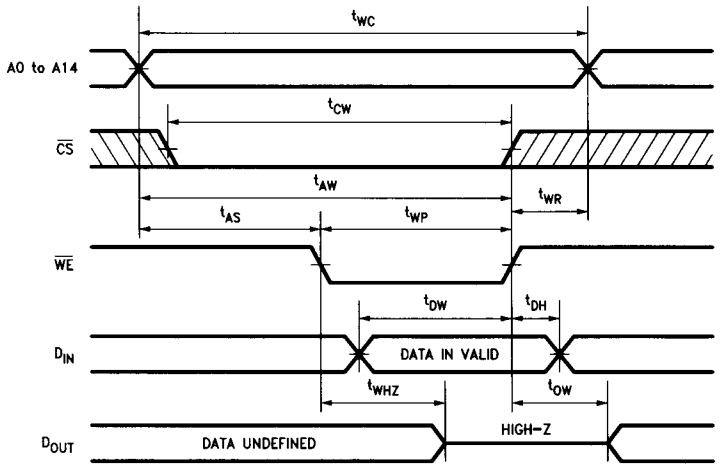
Note 3: Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

Symbol	Parameter	NM43256AN-10/-10L NM43256AM-10L NM43256AMX-10L/-10LL		NM43256AN-12/-12L NM43256AM-12L NM43256AMX-12L/-12LL		NM43256AN-15/-15L NM43256AM-15L		Units
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	100		120		150		ns
t_{CW}	Chip Select to End of Write	80		85		100		ns
t_{AW}	Address Valid to End of Write	80		85		100		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{WP}	Write Pulse Width	70		70		90		ns
t_{WR}	Write Recovery Time	5		5		5		ns
t_{DW}	Data Valid to End of Write	40		50		60		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{WHZ}	Write Enable to Output in HI-Z		35		40		50	ns
t_{OW}	Output Active from End of Write	10		10		10		ns

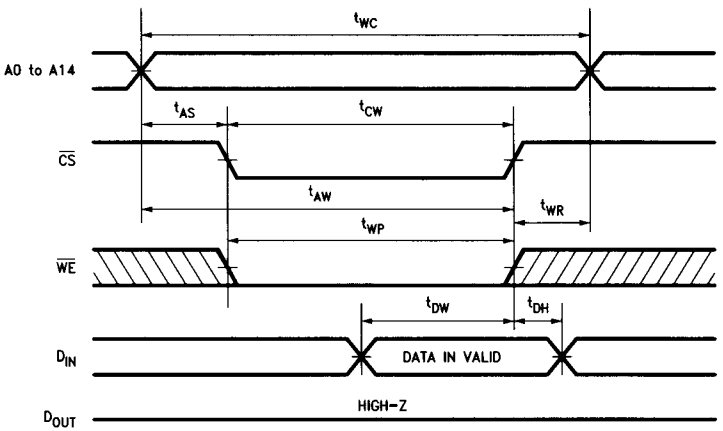
Write Cycle Timing Charts

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (Notes: 1, 2, 3, 4)



TL/D/10787–7

WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) (Notes: 1, 2)



TL/D/10787–8

Note 1: A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

Note 2: $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

Note 3: If $\overline{OE}$ is high, I/O pins remains in a high impedance state.

Note 4: During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

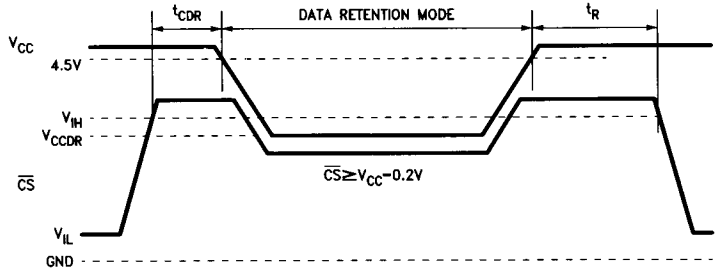
Low V_{CC} Data Retention Characteristics (T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CCDR}	Data Retention Supply Voltage	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
I_{CCDR}	Data Retention Supply Current	V_{CC} = 3.0V, $\overline{CS} \geq V_{CC} - 0.2V$		1	(Note 1)	μA
t_{CDR}	Chip Deselection to Data Retention Mode		0			ns
t_R	Operation Recovery Time		t_{RC}			ns

Note 1: NM43256A-10L/-12L/-15L 50 μA max. (T_A = 0°C ~ 70°C)
15 μA max. (T_A = 0°C ~ 40°C)

NM43256AMX-10LL/-12LL 20 μA max. (T_A = 0°C ~ 70°C)
3 μA max. (T_A = 0°C ~ 40°C)

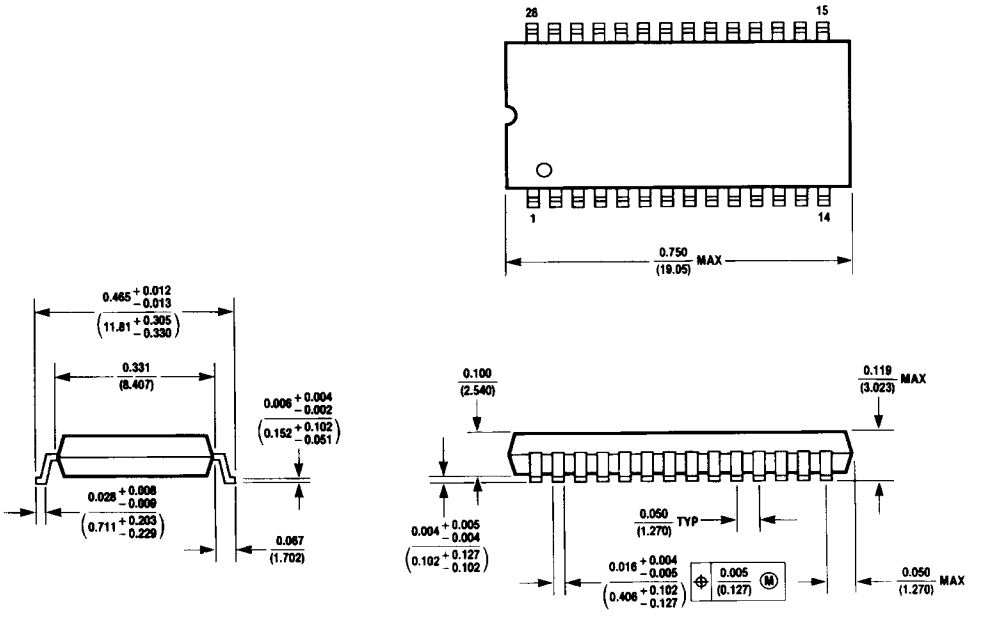
DATA RETENTION TIMING CHART (Note 1)



TL/D/10787–9

Note 1: The other inputs (Addresses, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a high impedance state.

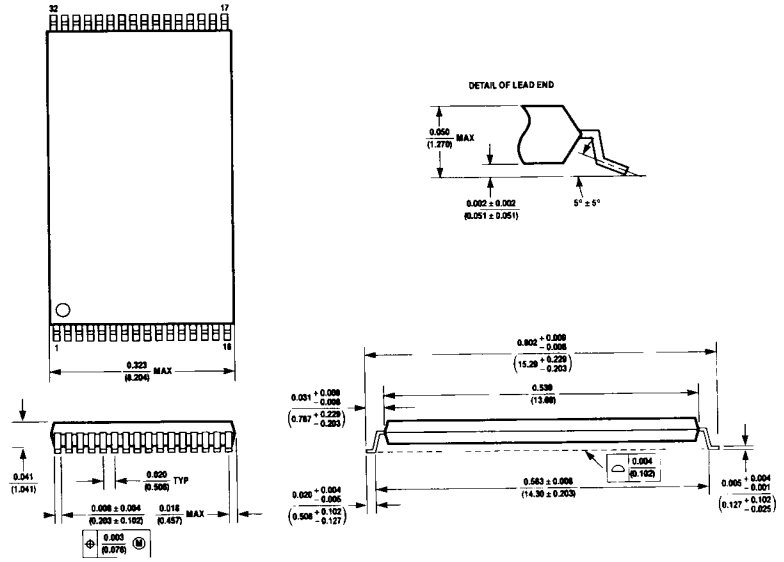
Package Information



TL/D/10787-13

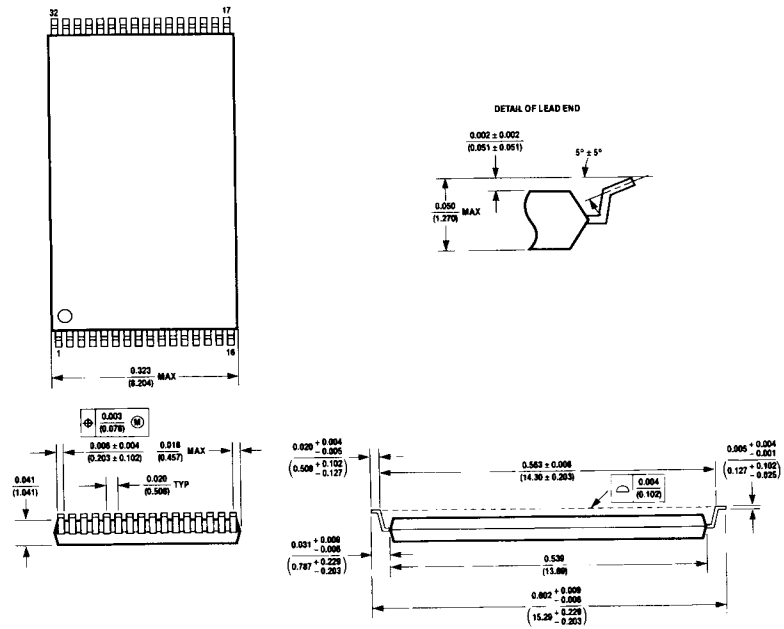
28-Pin Plastic SOP (450 mil)
Order Number NM43256AM

Package Information (Continued)



TL/D/10787–12

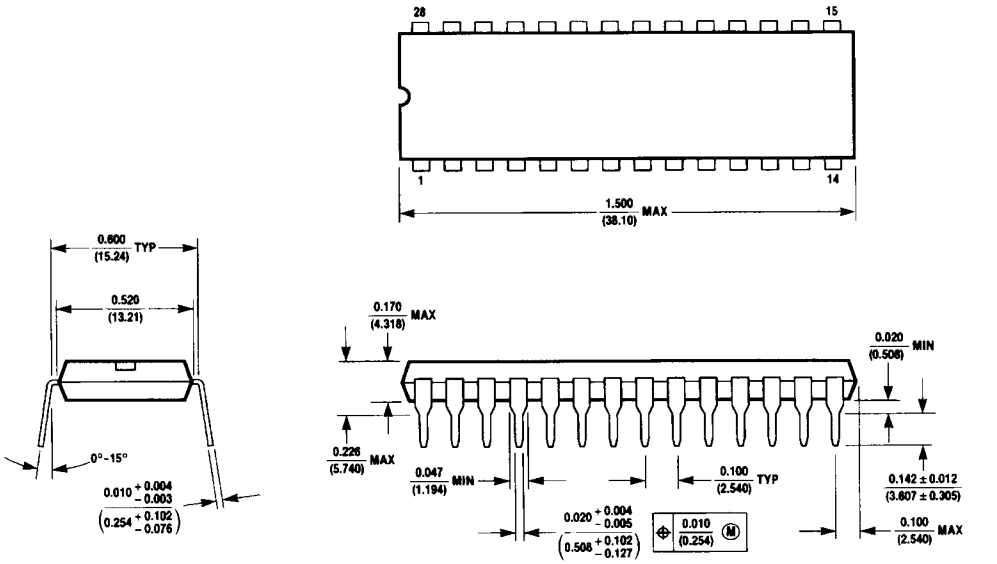
32-Pin Plastic TSOP (600 mil)
Order Number NM43256AMX



TL/D/10787–11

32-Pin Plastic TSOP (600 mil)
Order Number NM43256AMXR

Package Information (Continued)



TL/D/10787-10

28-Pin Plastic DIP (600 mil)
Order Number NM43256AN

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

OCT 17 1990 017718 ✓ 6

National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: (408) 721-5000
TWX: (910) 339-9240

National Semiconductor GmbH
Industriestrasse 10
D-8080 Furstenfeldbruck
West Germany
Tel: (0-81-41) 103-0
Telex: 527-649
Fax: (08141) 103554

National Semiconductor Japan Ltd.
Sanseido Bldg. 5F
4-15 Nishi Shinjuku
Shinjuku-Ku,
Tokyo 160, Japan
Tel: 3-299-7001
FAX: 3-299-7000

National Semiconductor Hong Kong Ltd.
Suite 513, 5th Floor
Chinachem Golden Plaza,
77 Mody Road, Tsimshatsui East,
Kowloon, Hong Kong
Tel: 3-7231290
Telex: 52996 NSSEA HX
Fax: 3-3112536

National Semiconductores Do Brasil Ltda.
Av. Brig. Faria Lima, 1383
6.0 Andor-Conj. 62
01451 Sao Paulo, SP, Brasil
Tel: (55/11) 212-5066
Fax: (55/11) 211-1181 NSBR BR

National Semiconductor (Australia) PTY, Ltd.
1st Floor, 441 St. Kilda Rd.
Melbourne, 3004
Victory, Australia
Tel: (03) 267-5000
Fax: 61-3-2677458