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National Semiconductor

August 1994

# NM93CS06/CS46/CS56/CS66 (MICROWIRE™ Bus Interface) 256-/1024-/2048-/4096-Bit Serial EEPROM with Data Protect and Sequential Read

## General Description

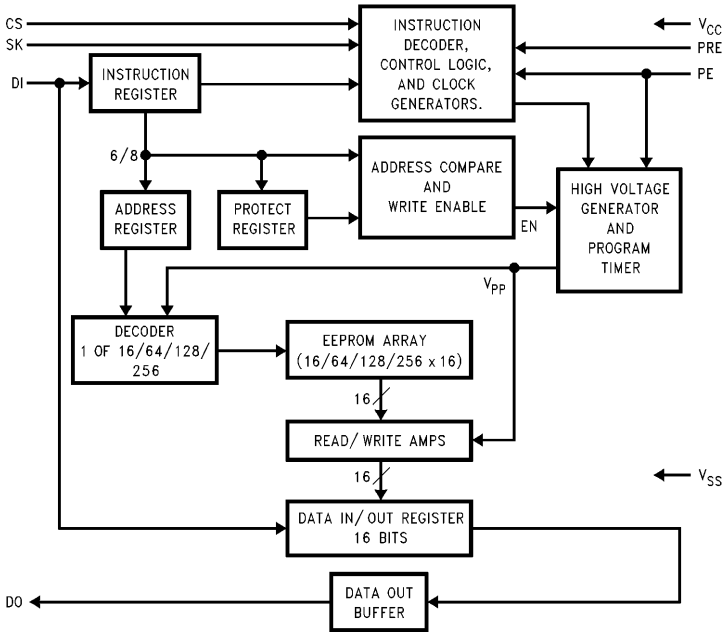
The NM93CS06/CS46/CS56/CS66 devices are 256/1024/2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory divided into 16/64/128/256 16-bit registers. Selected registers can be protected against data modification by programming the Protect Register with the address of the first register to be protected against data modification (all registers greater than, or equal to, the selected address are then protected from further change). Additionally, this address can be "locked" into the device, making all future attempts to change data impossible. These devices are fabricated using National Semiconductor floating-gate CMOS process for high reliability, high endurance and low power consumption. The NM93CSXX Family is offered in an SO package for small space considerations.

The EEPROM interfacing is MICROWIRE compatible providing simple interfacing to standard microcontrollers and microprocessors. There are a total of 10 instructions, 5 which operate on the EEPROM memory, and 5 which operate on the Protect Register. The memory instructions are READ, WRITE, WRITE ALL, WRITE ENABLE, and WRITE DISABLE. The Protect register instructions are PRREAD, PRWRITE, PRENABLE, PRCLEAR, and PRDISABLE.

## Features

- Write protection in a user defined section of memory
- Sequential register read
- Typical active current of 400 μA and standby current of 25 μA
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self timed write cycle
- Device status during programming mode
- 40 year data retention
- Endurance: $10^6$ data changes
- 4.5V to 5.5V operation in all modes of operation
- Packages available: 8-pin SO, 8-pin DIP

## Block Diagram

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NM93CS06/CS46/CS56/CS66 (MICROWIRE Bus Interface) 256-/1024-/2048-/4096-Bit Serial EEPROM with Data Protect and Sequential Read

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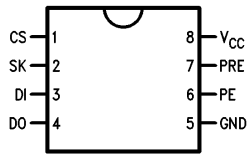
## Connection Diagram

**Dual-In-Line Package (N) and 8-Pin SO (M8)**

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**Top View**

**NS Package Number N08E and M08A**

**Pin Names**

| | |
|---|---|
| CS | Chip Select |
| SK | Serial Data Clock |
| DI | Serial Data Input |
| DO | Serial Data Output |
| GND | Ground |
| PE | Program Enable |
| PRE | Protect Register Enable |
| $V_{CC}$ | Power Supply |

## Ordering Information

**Commercial Temp. Range (0°C to +70°C)**

| Order Number* |
|---|
| NM93CS06N/NM93CS46N/NM93CS56N/NM93CS66N<br>NM93CS06M8/NM93CS46M8/NM93CS56M8/NM93CS66M8 |

**Extended Temp. Range (−40°C to +85°C)**

| Order Number* |
|---|
| NM93CS06EN/NM93CS46EN/NM93CS56EN/NM93CS66EN<br>NM93CS06EM8/NM93CS46EM8/NM93CS56EM8/NM93CS66EM8 |

**Military Temp. Range (−55°C to +125°C)**

| Order Number* |
|---|
| NM93CS06MN/NM93CS46MN/NM93CS56MN/NM93CS66MN<br>NM93CS06MM8/NM93CS46MM8/NM93CS56MM8/NM93CS66MM8 |



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## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Ambient Storage Temperature | −65°C to +150°C |
| All Input or Output Voltages with Respect to Ground | +6.5V to −0.3V |
| Lead Temperature (Soldering, 10 sec.) | +300°C |
| ESD rating | 2000V |

## Operating Conditions

| | |
|---|---|
| Ambient Operating Temperature | |
| NM93CSxx | 0°C to +70°C |
| NM93CSxxE | −40°C to +85°C |
| NM93CSxxM | −55°C to +125°C |
| Power Supply ($V_{CC}$) | 4.5V to 5.5V |

## DC and AC Electrical Characteristics $V_{CC}$ = 4.5V to 5.5V unless otherwise specified

Throughout this table, "M" refers to temperature range (−55°C to +125°C), not package.

| Symbol | Parameter | Part Number | Conditions | Min | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CCA}$ | Operating Current | NM93CS06–NM93CS66<br>NM93CS06E–NM93CS66E<br>NM93CS06M–NM93CS66M | CS = $V_{IH}$, SK = 1.0 MHz<br>SK = 1.0 MHz<br>SK = 0.5 MHz | | 1<br>1<br>1 | mA |
| $I_{CCS}$ | Standby Current | NM93CS06–NM93CS66<br>NM93CS06E–NM93CS06E<br>NM93CS06M–NM93CS06M | CS = $V_{IL}$ | | 50<br>50<br>100 | μA |
| $I_{IL}$<br>$I_{OL}$ | Input Leakage<br>Output Leakage | | $V_{IN}$ = 0V to $V_{CC}$<br>(Note 4) | | ±−1 | μA |
| $V_{IL}$<br>$V_{IH}$ | Input Low Voltage<br>Input High Voltage | | | −0.1<br>2 | 0.8<br>$V_{CC}$ + 1 | V |
| $V_{OL1}$<br>$V_{OH1}$ | Output Low Voltage<br>Output High Voltage | | $I_{OL}$ = 2.1 mA<br>$I_{OH}$ = −400 μA | <br>2.4 | 0.4 | V |
| $V_{OL2}$<br>$V_{OH2}$ | Output Low Voltage<br>Output High Voltage | | $I_{OL}$ = 10 μA<br>$I_{OH}$ = −10 μA | <br>$V_{CC}$ − 0.2 | 0.2 | V |
| $f_{SK}$ | SK Clock Frequency | NM93CS06–NM93CS66<br>NM93CS06E–NM93CS66E<br>NM93CS06M–NM93CS66M | (Note 5) | 0<br>0<br>0 | 1<br>1<br>0.5 | MHz |
| $t_{SKH}$ | SK High Time | NM93CS06–NM93CS66<br>NM93CS06E–NM93CS66E<br>NM93CS06M–NM93CS66M | | 250<br>300<br>500 | | ns |
| $t_{SKL}$ | SK Low Time | | | 250 | | ns |
| $t_{SKS}$ | SK Setup Time | | SK Must Be at $V_{IL}$<br>for $t_{SKS}$ before CS<br>goes high | 50<br>50<br>100 | | ns |
| $t_{CS}$ | Minimum CS Low Time | NM93CS06–NM93CS66<br>NM93CS06E–NM93CS66E<br>NM93CS06M–NM93CS66M | (Note 2) | 250<br>250<br>500 | | ns |
| $t_{CSS}$ | CS Setup Time | | | 100 | | ns |
| $t_{PRES}$ | PRE Setup Time | NM93CS06-NM93CS66<br>NM93CS06E-NM93CS66E<br>NM93CS06M–NM93CS66M | | 50<br>50<br>100 | | ns |
| $t_{DH}$ | DO Hold Time | | | 70 | | ns |
| $t_{PES}$ | PE Setup Time | NM93CS06–NM93CS66<br>NM93CS06E–NM93CS66E<br>NM93CS06M–NM93CS66M | | 50<br>50<br>100 | | ns |
| $t_{DIS}$ | DI Setup Time | NM93CS06–NM93CS66<br>NM93CS06E–NM93CS66E<br>NM93CS06M–NM93CS66M | | 100<br>100<br>200 | | ns |
| $t_{CSH}$ | CS Hold Time | | | 0 | | ns |



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## DC and AC Electrical Characteristics $V_{CC}$ = 4.5V to 5.5V unless otherwise specified (Continued)

| Symbol | Parameter | Part Number | Conditions | Min | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PEH}$ | PE Hold Time | NM93CS06–NM93CS66<br>NM93CS06E–NM93CS66E<br>NM93CS06M–NM93CS66M | | 250<br>250<br>500 | | ns |
| $t_{PREH}$ | PRE Hold Time | | | 50 | | ns |
| $t_{DIH}$ | DI Hold Time | | | 20 | | ns |
| $t_{PD1}$ | Output Delay to ''1'' | NM93CS06–NM93CS66<br>NM93CS06E–NM93CS66E<br>NM93CS06M–NM93CS66M | | | 500<br>500<br>1000 | ns |
| $t_{PD0}$ | Output Delay to ''0'' | NM93CS06–NM93CS66<br>NM93CS06E–NM93CS66E<br>NM93CS06M–NM93CS66M | | | 500<br>500<br>1000 | ns |
| $t_{SV}$ | CS to Status Valid | NM93CS06–NM93CS66<br>NM93CS06E–NM93CS66E<br>NM93CS06M–NM93CS66M | | | 500<br>500<br>1000 | ns |
| $t_{DF}$ | CS to DO in TRI-STATE® | NM93CS06–NM93CS66<br>NM93CS06E–NM93CS66E<br>NM93CS06M–NM93CS66M | CS = $V_{IL}$ | | 100<br>100<br>200 | ns |
| $t_{WP}$ | Write Cycle Time | | | | 10 | ms |

## Capacitance (Note 3)

$T_A$ = 25°C, f = 1 MHz

| Symbol | Test | Typ | Max | Units |
|---|---|---|---|---|
| $C_{OUT}$ | Output Capacitance | | 5 | pF |
| $C_{IN}$ | Input Capacitance | | 5 | pF |

**Note 1:** Stress ratings above those listed under ''Absolute Maximum Ratings'' may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** CS (Chip Select) must be brought low (to $V_{IL}$) for an interval of $t_{CS}$ in order to reset all internal device registers (device reset) prior to beginning another opcode cycle (this is shown in the opcode diagrams in the following pages).

**Note 3:** This parameter is periodically sampled and not 100% tested.

**Note 4:** Typical leakage values are in the 20 nA range.

**Note 5:** The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the $f_{SK}$ parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both $t_{SKH}$ and $t_{SKL}$ limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKH\ (minimum)} + t_{SKL\ (minimum)}$ for shorter SK cycle time operation.

## AC Test Conditions

| $V_{CC}$ Range | $V_{IL}/V_{IH}$ Input Levels | $V_{IL}/V_{IH}$ Timing Level | $V_{OL}/V_{OH}$ Timing Level | $I_{OL}/I_{OH}$ |
|---|---|---|---|---|
| 4.5V ≤ $V_{CC}$ ≤ 5.5V (TTL Levels) | 0.4V/2.4V | 1.0V/2.0V | 0.4V/2.4V | −2.1 mA/ 0.4 mA |
| Output Load: 1 TTL Gate ($C_L$ = 100 pF) | | | | |



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## Functional Description

The NM93CSxx EEPROM Family has 10 instructions as described below. All Data-In signals are clocked into the device on the low-to-high SK transition.

**Read and Sequential Register Read (READ):**

The READ instruction outputs serial data on the D0 pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the **sequential register read** mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

**Write Enable (WEN):**

When $V_{CC}$ is applied to the part, it ''powers up'' in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until a Write Disable (WDS) instruction is executed or $V_{CC}$ is completely removed from the part.

**Write (WRITE):**

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the WRITE instruction, however, after loading the WRITE instruction the PE pin becomes a ''don't care''. The D0 pin indicates the READY/BUSY status of the chip if CS is brought high after the $t_{CS}$ interval. D0 = logical 0 indicates that programming is still in progress. D0 = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

**Write All (WRALL):**

The WRALL instruction is valid only when the Protect Register has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held high while loading the WRALL instruction, however, after loading the instruction the PE pin becomes a ''don't care''. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the $t_{CS}$ interval. This function is DISABLED if the Protect Register is in use to lock out a section of memory.

**Write Disable (WDS):**

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

**Note:** For all Protect Register Operations: If the PRE pin is not held at $V_{IH}$, all instructions will be applied to the EEPROM array, rather than the Protect Register.

**Protect Register Read (PRREAD):**

The PRREAD instruction outputs the address stored in the Protect Register on the DO pin. The PRE pin **MUST** be held high while loading the instruction sequence. Following the PRREAD instruction the 6- or 8-bit address stored in the memory protect register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 6- or 8-bit address string.

**Protect Register Enable (PREN):**

The PREN instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held high while loading the instruction sequence.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

**Protect Register Clear (PRCLEAR):**

The PRCLEAR instruction clears the address stored in the Protect Register and, therefore, enables **all** registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held high while loading the instruction sequence, however, after loading the PRCLEAR instruction the PRE and PE pins become ''don't care''. Note that a PREN instruction must **immediately** precede a PRCLEAR instruction.

Please note that the PRCLEAR instruction and the PRWRITE instruction will both program the Protect Register with all 1s. However, the PRCLEAR instruction will allow the LAST register to be programmed, whereas the PRWRITE instruction = all 1s will PREVENT the last register from being programmed. In addition, the PRCLEAR instruction will allow the use of the WRALL command, where the PRWRITE = all 1s will lock out the Bulk programming opcode.

**Protect Register Write (PRWRITE):**

The PRWRITE instruction is used to write into the Protect Register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction the Protect Register must first be cleared by executing a PRCLEAR operation and that the PRE and PE pins **must** be held high while loading the instruction, however, after loading the PRWRITE instruction the PRE and PE pins become 'don't care'. Note that a PREN instruction must **immediately** precede a PRWRITE instruction.

**Protect Register Disable (PRDS):**

The PRDS instruction is a **ONE** TIME ONLY instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held high while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become ''don't care''.

Note that a PREN instruction must **immediately** precede a PRDS instruction.



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## Instruction Set for the NM93CS06 and NM93CS46

| Instruction | SB | Op Code | Address | Data | PRE | PE | Comments |
|---|---|---|---|---|---|---|---|
| READ | 1 | 10 | A5–A0 | | 0 | X | Reads data stored in memory, starting at specified address. |
| WEN | 1 | 00 | 11XXXX | | 0 | 1 | Enable all programming modes. |
| WRITE | 1 | 01 | A5–A0 | D15–D0 | 0 | 1 | Writes address if unprotected. |
| WRALL | 1 | 00 | 01XXXX | D15–D0 | 0 | 1 | Writes all registers. Valid only when Protect Register is cleared. |
| WDS | 1 | 00 | 00XXXX | | 0 | X | Disables all programming modes. |
| PRREAD | 1 | 10 | XXXXXX | | 1 | X | Reads address stored in Protect Register. |
| PREN | 1 | 00 | 11XXXX | | 1 | 1 | Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions. |
| PRCLEAR | 1 | 11 | 111111 | | 1 | 1 | Clears the Protect Register so that no registers are protected from WRITE. |
| PRWRITE | 1 | 01 | A5–A0 | | 1 | 1 | Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE. |
| PRDS | 1 | 00 | 000000 | | 1 | 1 | ONE TIME ONLY instruction after which the address in the Protect Register cannot be altered. |

**Note:** Address bits A5 and A4 become ''Don't Care'' for the NM93CS06.

## Instruction Set for the NM93CS56 and NM93CS66

| Instruction | SB | Op Code | Address | Data | PRE | PE | Comments |
|---|---|---|---|---|---|---|---|
| READ | 1 | 10 | A7–A0 | | 0 | X | Reads data stored in memory, starting at specified address. |
| WEN | 1 | 00 | 11XXXXXX | | 0 | 1 | Enable all programming modes. |
| WRITE | 1 | 01 | A7–A0 | D15–D0 | 0 | 1 | Writes address if unprotected. |
| WRALL | 1 | 00 | 01XXXXXX | D15–D0 | 0 | 1 | Writes all registers. Valid only when Protect Register is cleared. |
| WDS | 1 | 00 | 00XXXXXX | | 0 | X | Disables all programming modes. |
| PRREAD | 1 | 10 | XXXXXXXX | | 1 | X | Reads address stored in Protect Register. |
| PREN | 1 | 00 | 11XXXXXX | | 1 | 1 | Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions. |
| PRCLEAR | 1 | 11 | 11111111 | | 1 | 1 | Clears the ''protect register'' so that no registers are protected from WRITE. |
| PRWRITE | 1 | 01 | A7–A0 | | 1 | 1 | Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE. |
| PRDS | 1 | 00 | 00000000 | | 1 | 1 | ONE TIME ONLY instruction after which the address in the Protect Register cannot be altered. |

**Note:** Address bit A7 becomes ''Don't Care'' for the NM93CS56.



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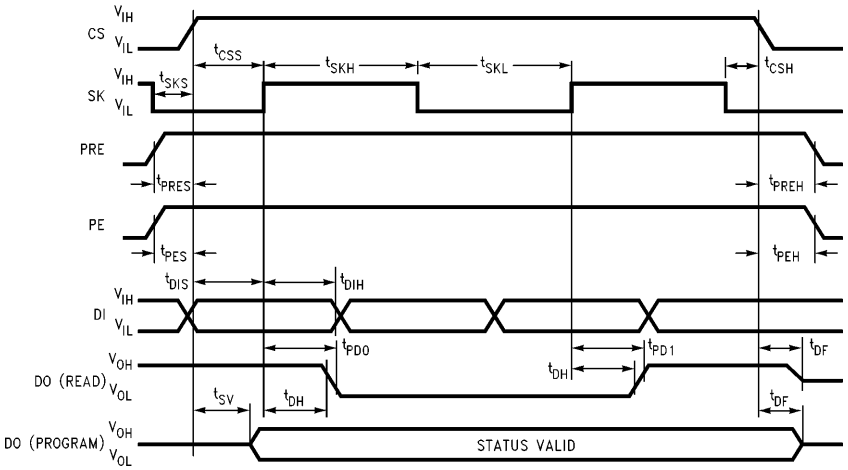
## Timing Diagrams

**Synchronous Data Timing**

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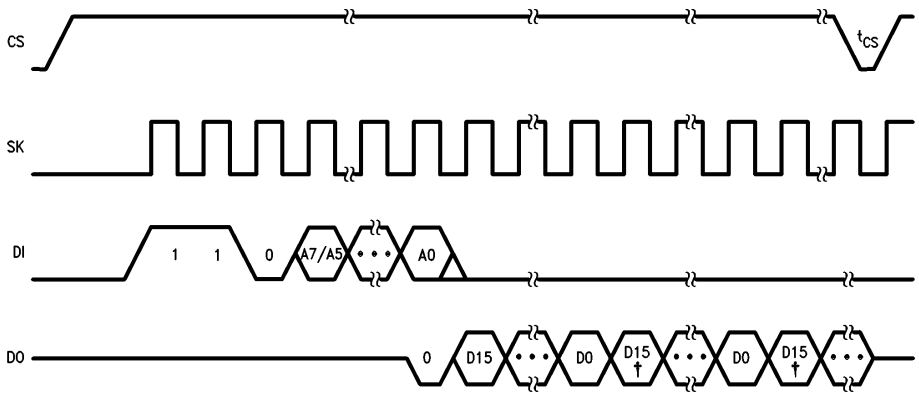
**READ:**
**PRE = 0, PE = X**




†The memory automatically cycles to the next register with continued clocking of SK.

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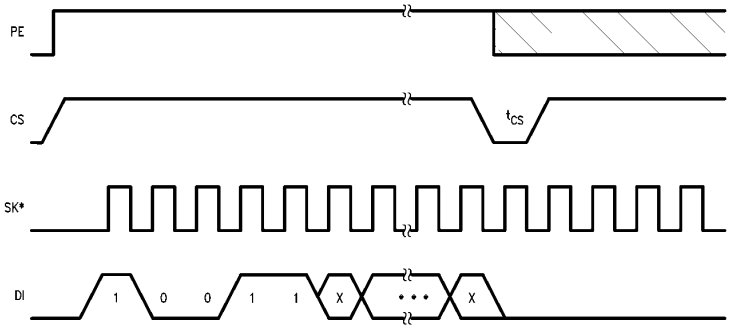
## Timing Diagrams (Continued)

**WEN:**
**PRE = 0, D0 = TRI-STATE**

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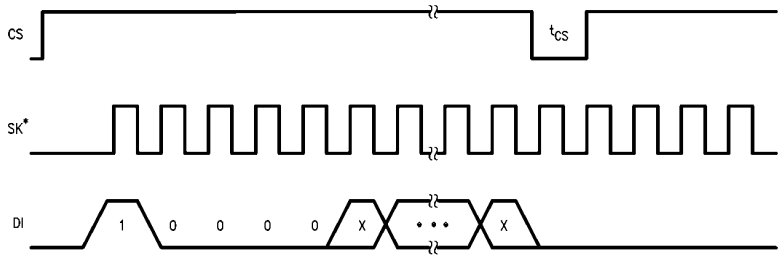
**WDS:**
**PRE = 0, PE = X, DO = TRI-STATE**

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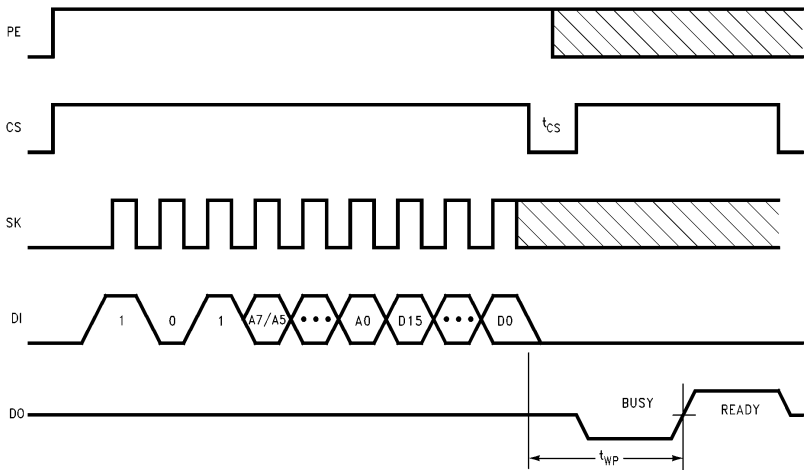
**WRITE:**
**PRE = 0**

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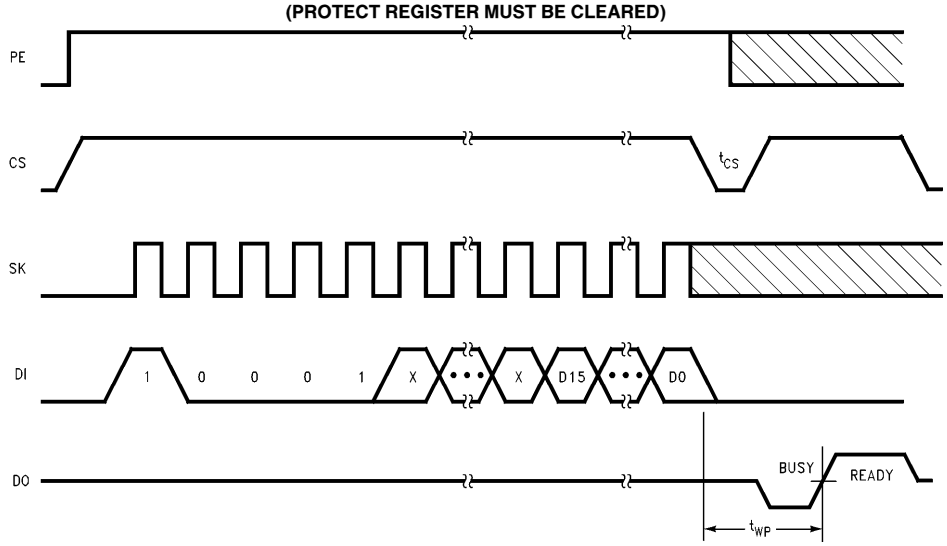
## Timing Diagrams (Continued)

**WRALL:**
**PRE = 0**
**(PROTECT REGISTER MUST BE CLEARED)**

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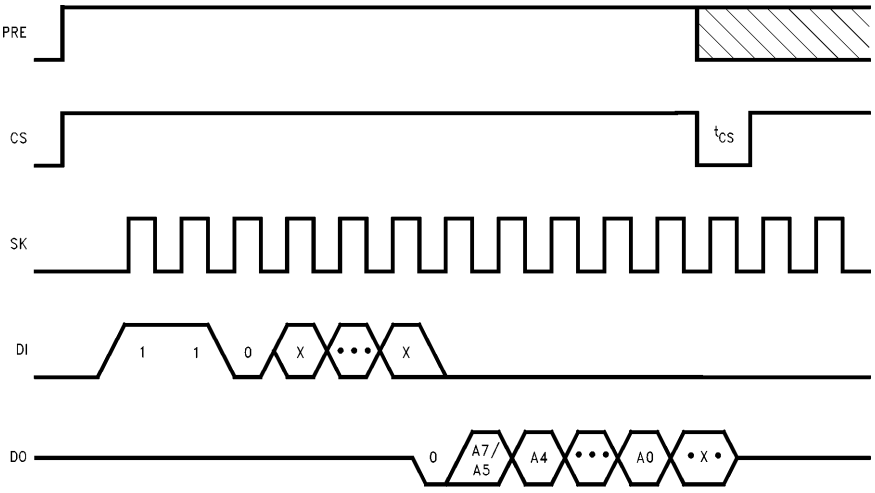
**PRREAD:**
**PE = X**

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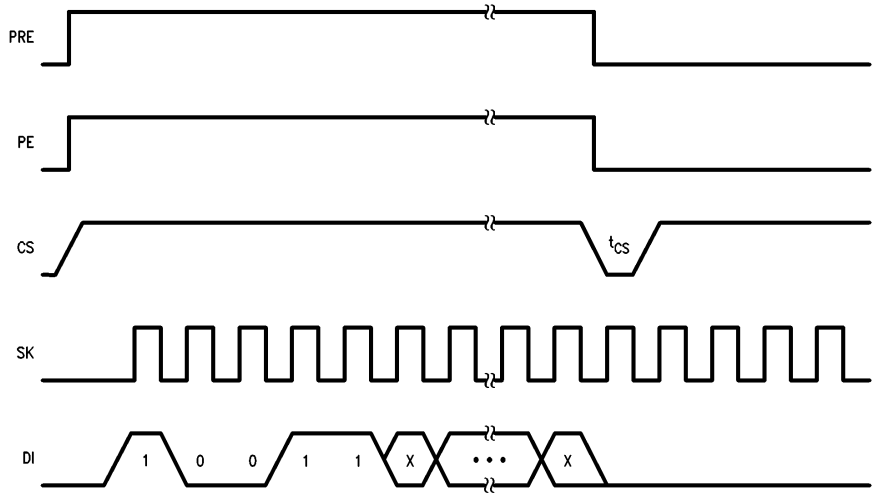
## Timing Diagrams (Continued)

**PREN:**
**D0 = TRI-STATE**
**(A WEN CYCLE MUST PRECEDE A PREN CYCLE)**

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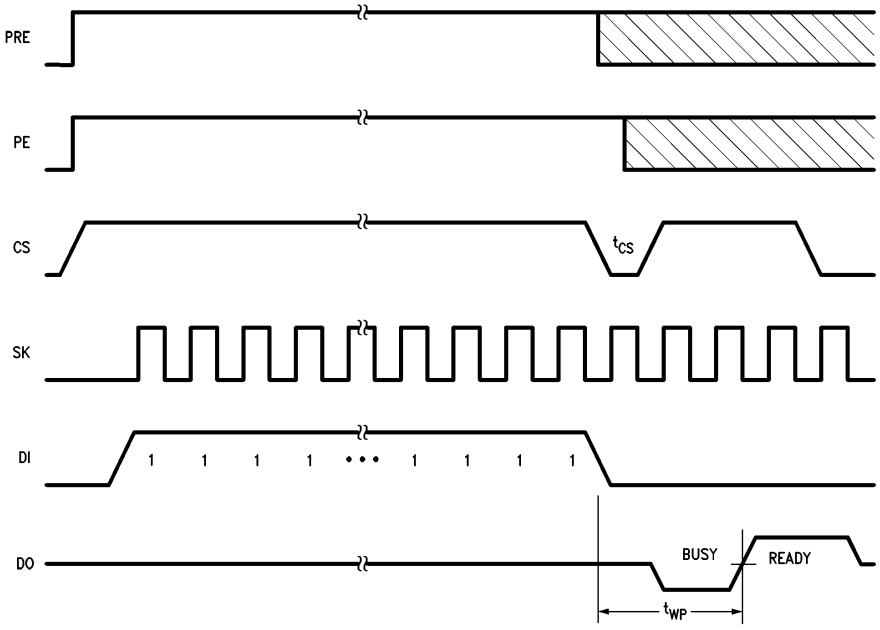
**PRCLEAR:**
**(A PREN CYCLE MUST IMMEDIATELY PRECEDE A PRCLEAR CYCLE)**

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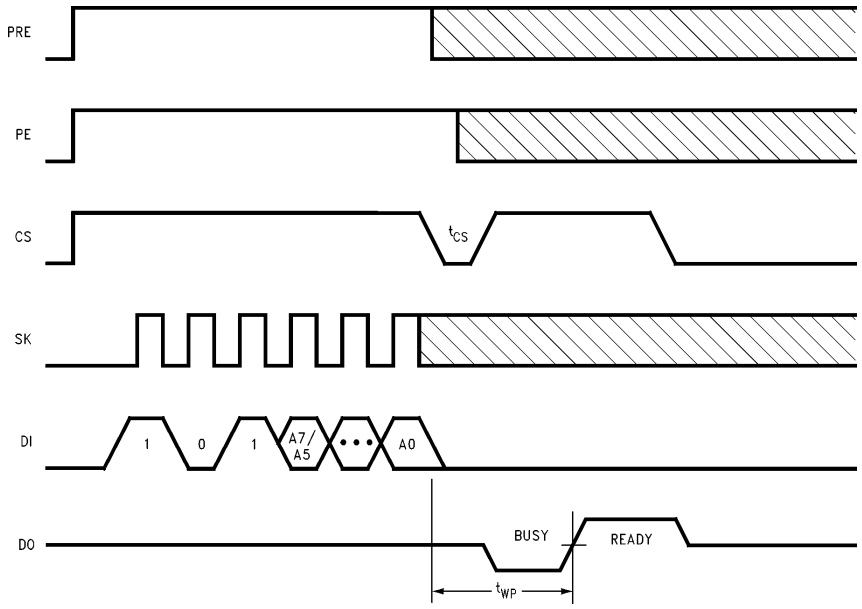
## Timing Diagrams (Continued)

**PRWRITE:**
**(PREN CYCLES MUST IMMEDIATELY PRECEDE A PRWRITE CYCLE.)**

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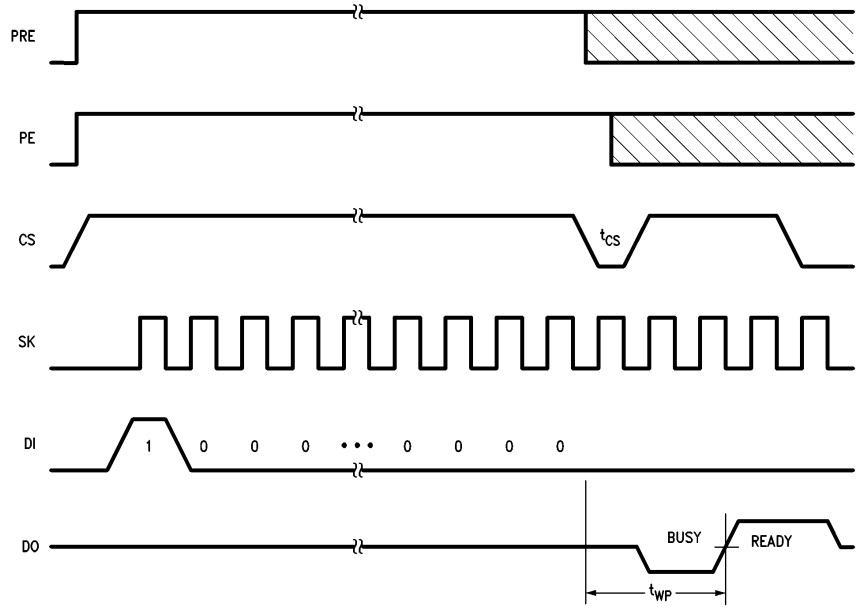
**PRDS:**
**(*ONE TIME ONLY INSTRUCTION. A PREN CYCLE MUST IMMEDIATELY PRECEDE A PRDS CYCLE.)**

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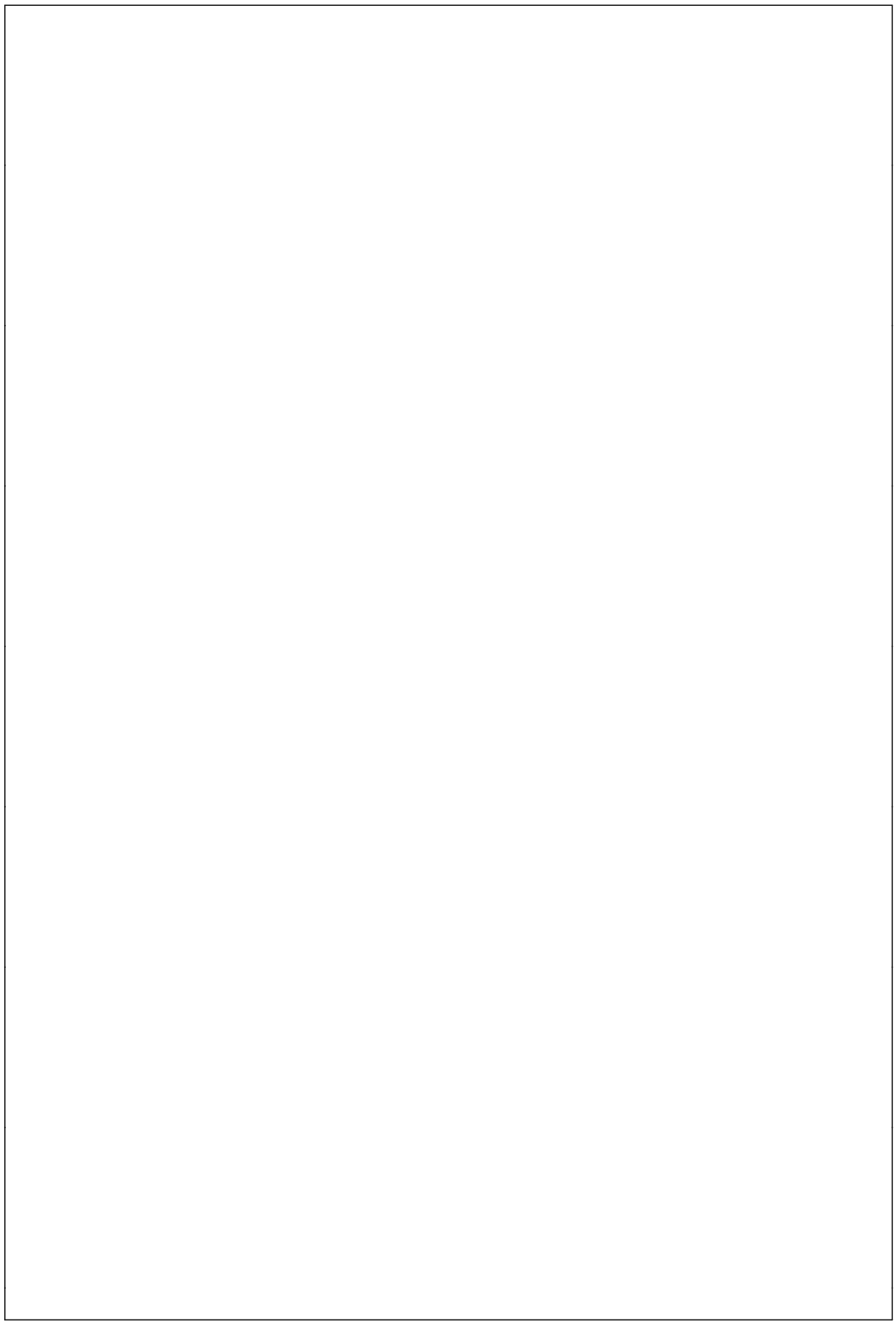



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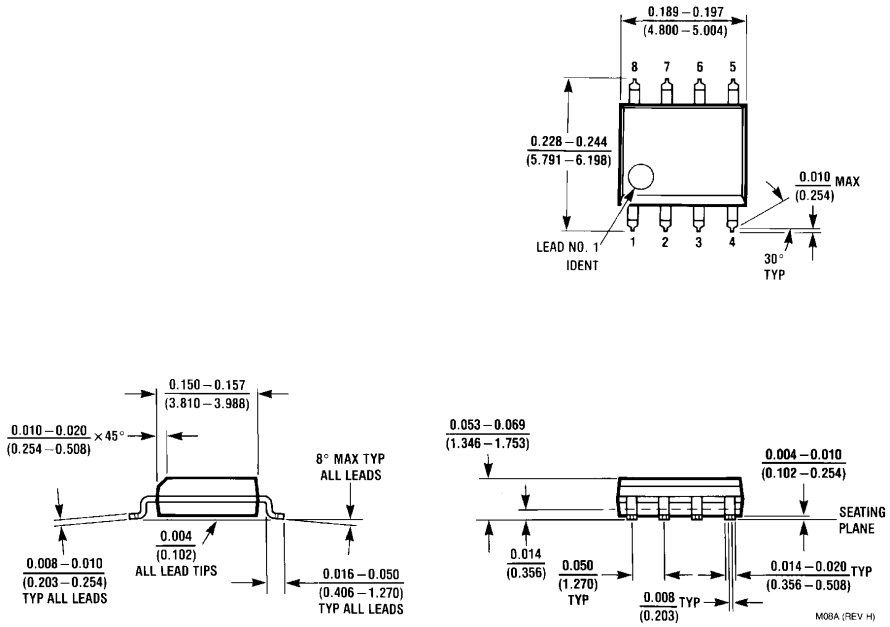
## Physical Dimensions inches (millimeters)




**Molded Package, Small Outline, 0.15 Wide, 8-Lead (M8)**
**Order Number NM93CS06M8, NM93CS46M8 or NM93CS56M8**
**NS Package Number M08A**



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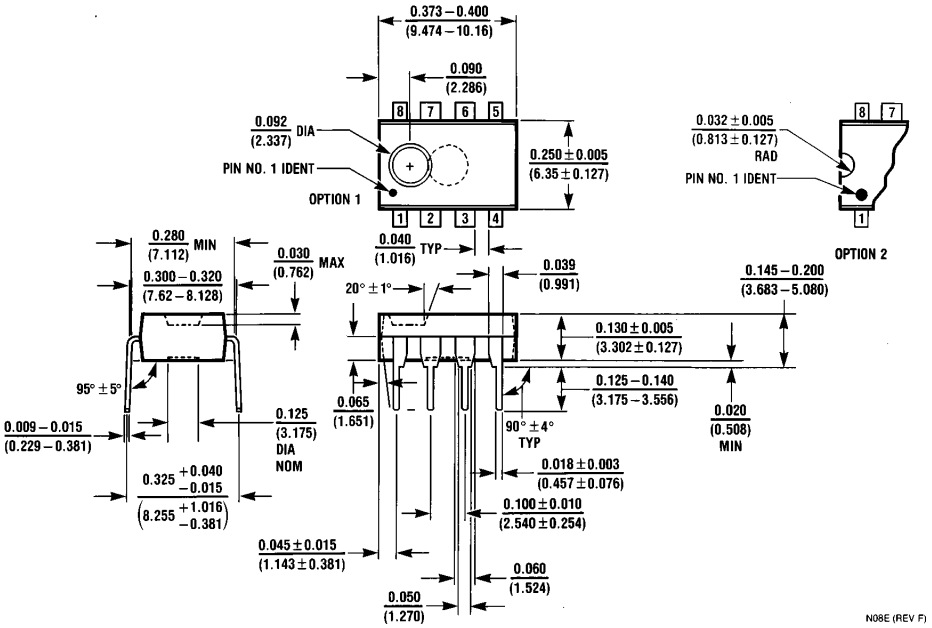
## Physical Dimensions inches (millimeters) (Continued)




**Molded Dual-In-Line Package (N)**
**Order Number NM93CS06N, NM93CS46N, NM93CS56 or NM93CS66N**
**NS Package Number N08E**

### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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