National Semiconductor

MOS EPROMs
ADVANCE INFORMATION

NMC2532 32k-Bit (4k x 8) UV Erasable PROM

General Description

The NMC2532 is a 32,768-bit EPROM operating from a single 5V power supply. This device is an ultraviolet erasable, electrically programmable, read only memory fabricated using National's high speed, low power, silicon gate technology.

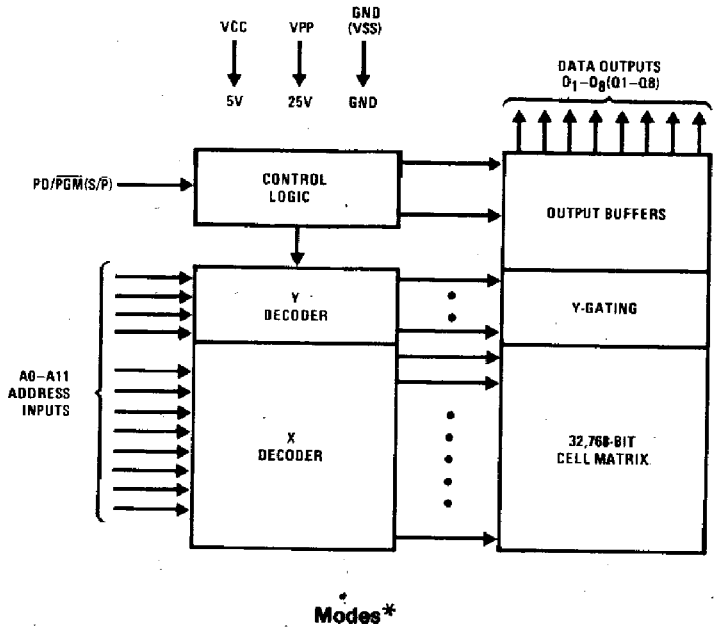
This device is deselected when pin 20 is high and automatically placed in the standby mode. This mode provides an 85% reduction in power with no increase in access time.

Bits may be programmed at random, in sequence or singly. Typical erasure time is 20 minutes using a 12 mW/cm^2 ultraviolet lamp.

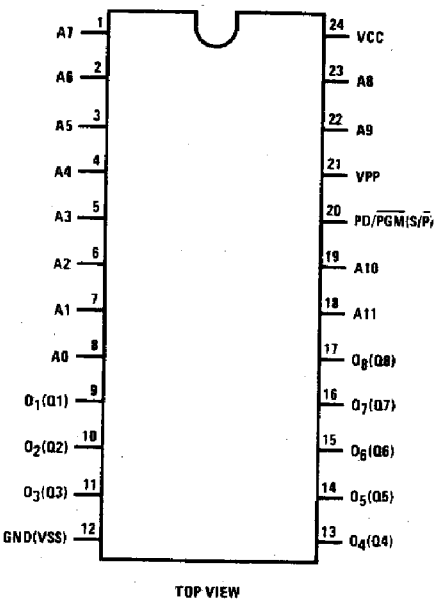
Features

- Single 5V power supply
- 450 ns max access time
- Low power:
  Active — 160 mA max
  Standby — 25 mA max
- Fully static
- TRI-STATE® output
- All I/O pins TTL compatible
- Pin compatible with existing EPROMs and ROMs
- Single location programming

Block and Connection Diagrams*



Dual-In-Line Package



TOP VIEW

Order Number NMC2532Q
See NS Package J24CQ

Modes*

Mode	Pin Name/Number			
	PD/PGM (S/P) 20	VPP 21	VCC 24	Outputs 9-11, 13-17
Read	VIL	5V	5V	DOUT
Standby	VIH	5V	5V	Hi-Z
Program	Pulsed VIH to VIL	25V	5V	DIN
Program Verify	VIL	5V	5V	DOUT
Program Inhibit	VIH	25V	5V	Hi-Z

Pin Names*

PD/PGM (S/P)	Power Down (Chip Select)
A0-A11	Address Inputs
O_1-O_8(Q1-Q8)	Data Outputs
VPP	Program Power (25V)
VCC	Power (5V)
GND (VSS)	Ground

* Symbols in parentheses are proposed industry standard.

Absolute Maximum Ratings (Note 1)

Temperature under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input and Output Voltages with Respect to VSS During Read	+6V to −0.3V
VPP Supply Voltage with Respect to VSS During Programming	+26.5V to −0.3V
Power Dissipation	1.5W
Lead Temperature (Soldering, 10 seconds)	300°C

READ OPERATION

DC Operating Characteristics (Note 2)

TA = 0°C to 70°C, VCC = 5V ± 5%, VSS = 0V, VPP = VCC ± 0.6V (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ILI	Input Load Current	VIN = 5.25V			10	μA
ILO	Output Leakage Current	VOUT = 5.25V			10	μA
ICC1	VCC Current Standby	PD/$\overline{PGM}$ (S/$\overline{P}$) = VIH		15	25	mA
ICC2	VCC Current Active	PD/$\overline{PGM}$ (S/$\overline{P}$) = VIL		85	160	mA
VIL	Input Low Voltage		−0.1		0.65	V
VIH	Input High Voltage		2.2		VCC+1	V
VOL	Output Low Voltage	IOL = 2.1 mA			0.45	V
VOH	Output High Voltage	IOH = −400 μA	2.4			V
IPP1/IPP2	VPP Standby/Active Current				300	μA

AC Characteristics

TA = 0°C to 70°C, VCC = 5V ± 5%, VSS = 0V, VPP = VCC ± 0.6V (Note 3)

Symbol		Parameter	Conditions	Min	Max	Units
Alternate	Standard					
t_{ACC}	TAVQV	Address to Output Valid	PG/$\overline{PGM}$ = VIL		450	ns
t_{APR}	TSLQV	Select to Output Valid			450	ns
t_{PXZ}	TSHQZ	Select to Output Hi-Z		0	100	ns
t_{PVX}	TAXQX	Address to Output Hold	PD/$\overline{PGM}$ = VIL	0		ns

Capacitance (Note 4) TA = 25°C, f = 1 MHz

Symbol	Parameter	Conditions	Typ	Max	Units
CIN	Input Capacitance	VIN = 0V	4	6	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

AC Test Conditions

Output Load: 1 TTL gate and CL = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Recommended DC Operating Conditions" provides conditions for actual device operation.

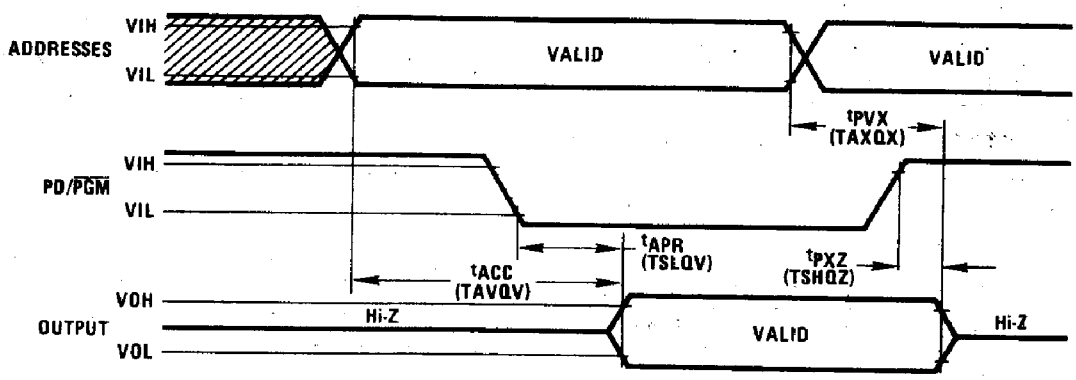
Note 2: Typical values are for TA = 25°C and nominal supply voltages.

Note 3: VPP can be tied directly to VCC (except during programming).

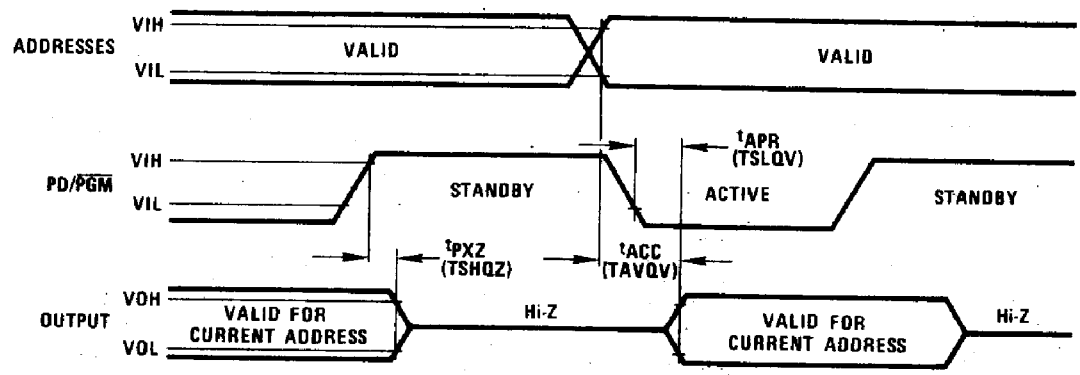
Note 4: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation C = IΔt/ΔV. Capacitance is guaranteed by periodic testing.

Switching Time Waveforms*

Read Cycle



Standby Power Down Mode



* Symbols in parentheses are proposed industry standard.

PROGRAM OPERATION

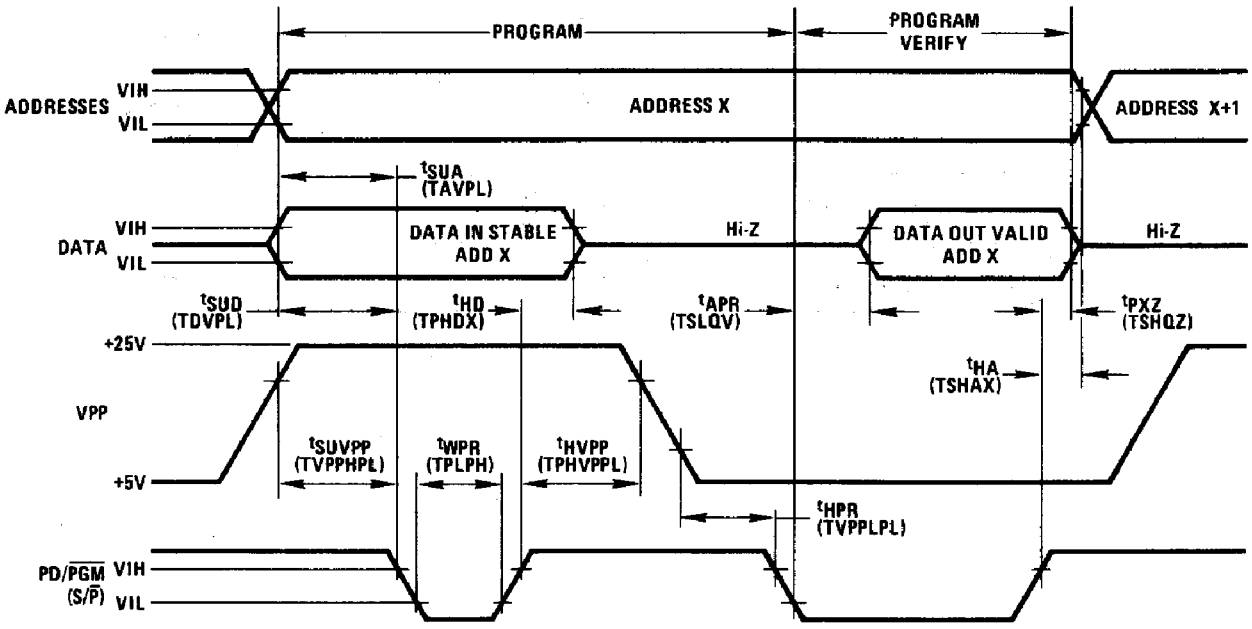
DC Characteristics $T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ILI	Input Current All Inputs	VIN = VIL or VIH			10	μA
VOL	Output Low Voltage During Verify	IOL = 2.1 mA			0.45	V
VOH	Output High Voltage During Verify	IOH = −400 μA	2.4			V
ICC	VCC Supply Current			85	160	mA
VIL	Input Low Level All Inputs		−0.1		0.65	V
VIH	Input High Level All Inputs Except VPP		2.2		VCC + 1	V
IPP	VPP Supply Current	PD/$\overline{PGM}$ (S/$\overline{P}$) = VIL			30	mA

AC Characteristics $T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$

Symbol		Parameter	Min	Typ	Max	Units
Alternate	Standard					
t_{SUA}	TAVPL	Address Set-Up Time	2			μs
t_{SUD}	TDVPL	Data Set-Up Time	2			μs
t_{SUVPP}	TVPPHPL	VPP Set-Up Time	0			ns
t_{WPR}	TPLPH	Program Pulse Width	45	50	55	ms
t_{HD}	TPHDX	Data Hold Time	2			μs
t_{HVPP}	TPHVPPL	VPP Hold Time	0			ns
t_{HPR}	TVPPLPL	VPP Recovery Time	0			ns
t_{APR}	TSLQV	Select to Output Valid			450	ns
t_{HA}	TSHAX	Address Hold Time	0			ns
t_{PXZ}	TSHQZ	Select to Output Hi-Z	0		100	ns

Programming Waveforms* (Note 5) $T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$



Note 5: The input timing reference level is 0.65V for VIL and 2.2V for VIH.
* Symbols in parentheses are proposed industry standard.

Functional Description

DEVICE OPERATION

The NMC2532 has two modes of operation in the normal system environment. These are shown in Table I.

TABLE I. OPERATING MODES (VCC = 5V)*

Mode \ Pins	PD/$\overline{PGM}$ (S/$\overline{P}$) 20	ICC Max 24	Outputs 9-11, 13-17
Read	VIL	160 mA	DOUT
Standby	VIH	25 mA	Hi-Z

Read Mode

The NMC2532 read operation requires that PD/$\overline{PGM}$ = VIL and that addresses A0-A11 have been stabilized. Valid data will apear on the output pins after t_{ACC} or t_{APR} times (see Switching Time Waveforms) depending on which is limiting.

Standby Mode

The NMC2532 is placed in the standby mode (deselected and powered down) by making PD/$\overline{PGM}$ = VIH. This automatically controls the outputs to their Hi-Z state. The power dissipation is reduced to 15% of the normal operating power. VCC must be kept at 5V. Access time at power up (chip selection) remains either t_{ACC} or t_{APR} (see Switching Time Waveforms).

PROGRAMMING

The NMC2532 is shipped from National completely erased. All bits will be at a "1" level (outputs high) in this initial state after any full erasure. Table II shows the three programming modes.

TABLE II. PROGRAMMING MODES (VCC = 5V)*

Mode \ Pins	PD/$\overline{PGM}$ (S/$\overline{P}$) 20	VPP 18	Outputs 9-11, 13-17
Program	VIL	25V	DIN
Program Verify	VIL	5V	DOUT
Program Inhibit	VIH	25V	Hi-Z

Program Mode

The NMC2532 is programmed by placing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the PD/$\overline{PGM}$ (S/$\overline{P}$) pin. All input voltage levels, including the program pulse on the PD/$\overline{PGM}$ pin are TTL compatible. The programming sequence is:

With the VPP pin at 25V and VCC = 5V, an address is selected and the desired data word is applied to the output pins (VIL = "0" and VIH = "1" for both address and data). After the address and data signals are stable the PD/$\overline{PGM}$ pin is pulsed from VIH to VIL with a pulse width between 45 ms and 55 ms.

Multiple pulses are not needed but will not cause device damage. No pins should be left open. A low level, VIL or lower *must not* be maintained steady state (DC signal) on the PD/$\overline{PGM}$ pin during programming. Several NMC2532s may be programmed in parallel (the same data in each one) in this mode.

Program Verify

The programming of the NMC2532 may be verified, either one word at a time during the programming (as shown in the timing diagram) or by reading all of the words out at the end of the programming sequence.

Program Inhibit

The program inhibit mode allows programming several NMC2532s in parallel with different data for each one by controlling which ones receive the program pulse. All similar inputs may be paralleled. Pulsing the PD/$\overline{PGM}$ pin from VIH to VIL on a selected unit or units will cause programming, while inhibiting the PD/$\overline{PGM}$ pulse will inhibit programming and keep the outputs of the inhibited devices in the Hi-Z state.

ERASURE PROCEDURE

The NMC2732 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gates to their initial state through induced photo current. It is recommended that this device be kept out of direct sunlight. The UV content of sunlight may cause the a partial erasure of some bits in a relatively short period of time. Direct sunlight (any intense light) can cause temporary functional failure due to generation of photo current. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label etc.) should be placed over the package window if this product is to be operated under these lighting conditions.

An ultraviolet source of 2537Å yielding a total integrated dosage of 15 Watt-seconds/cm^2 is required. This will erase a unit in approximately 15 to 20 minutes when a UV lamp of a 12 mW/cm^2 power rating is used. The NMC2532 to be erased should be placed one inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

* Symbols in parentheses are proposed industry standard.