National Semiconductor

NMC27C53 Very High Speed Version 262,144-Bit (32k x 8) UV Erasable CMOS PROM Pin Compatible with 256k Bipolar PROMs

General Description

The NMC27C53 is a very high-speed 256k, UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C53 is designed to operate with a single +5V power supply with ±10% tolerance.

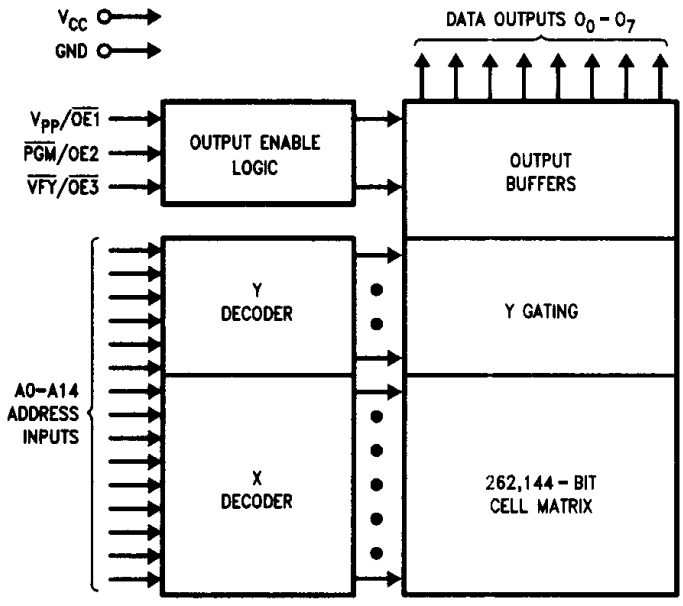
The NMC27C53 is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability. A two transistor memory cell is used for speed enhancement.

Features

- Clocked sense amps and two transistor memory cell for fast access time down to 55 ns
- Low CMOS power consumption
  — Active power: 275 mW max
- Performance compatible to current high speed microprocessors
- Pin compatible with 256k bipolar PROMs
- Single 5V power supply
- Fast and reliable programming (100 μs for most bytes)
- Static operation for NMC27C53—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming control
- High current CMOS level output driver

Block Diagram



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Pin Names

A0–A14	Address
OE1–OE3	Output Enables
O_0–O_7	Outputs
$\overline{PGM}$	Program
$\overline{VFY}$	Verify

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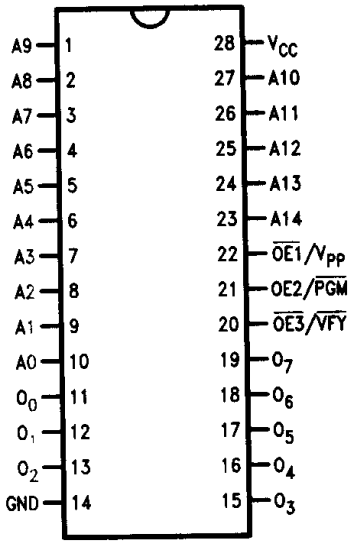
Connection Diagram

27C51	27C49
A9	
A8	
A7	A7
A6	A6
A5	A5
A4	A4
A3	A3
A2	A2
A1	A1
A0	A0
O_0	O_0
O_1	O_1
O_2	O_2
GND	GND

NMC27C53Q
Dual-In-Line Package



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27C49	27C51
	V_{CC}
	A10
V_{CC}	A11
A8	A12
A9	A13
A10	$\overline{OE1}/V_{PP}$
$\overline{OE}/V_{PP}$	OE2/$\overline{VFY}$
A11	$\overline{OE3}$
A12/$\overline{PGM}$	$\overline{OE4}/\overline{PGM}$
O_7	O_7
O_6	O_6
O_5	O_5
O_4	O_4
O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C53 pins.

Order Number NMC27C53Q
See NS Package Number J28AQ

Ordering Information

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C53Q55	55
NMC27C53Q70	70
NMC27C53Q90	90

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A13 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
$\overline{OE1}/V_{PP}$ and A13 Supply Voltage with Respect to Ground During Programming	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{OE1}$, $\overline{OE3} = V_{IH}$, or OE2 = V_{IL}			1	μA
I_{PP1}	V_{PP} Current	$V_{PP} = V_{CC}$			10	μA
I_{CC1} (Note 7)	V_{CC} Current (Active) TTL Inputs	f = 20 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		30	70	mA
I_{CC2} (Note 7)	V_{CC} Current (Active) CMOS Inputs	f = 20 MHz Inputs = V_{CC} or GND, I/O = 0 mA		25	50	mA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 16 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA (Note 8)	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA (Note 8)	V_{CC} − 0.1			V

AC Electrical Characteristics

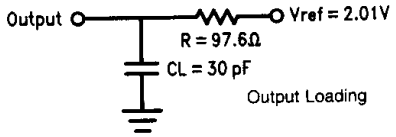
Symbol	Parameter	Conditions	NMC27C53						Units
			Q55		Q70		Q90		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{OE1}$, $\overline{OE3}$ = V_{IL}, OE2 = V_{IH}		55		70		90	ns
t_{OE}	OE to Output Delay			25		30		40	ns
t_{DF}	OE Disable to Output Float (Note 3)		0	25	0	30	0	40	ns
t_{OH}	Output Hold from Addresses, $\overline{OE1}$, OE2 or $\overline{OE3}$, Whichever Occurred First	$\overline{OE1}$ = $\overline{OE3}$ = V_{IL} OE2 = V_{IH}	0		0		0		ns

Capacitance T_A = +25°C, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

AC Test Conditions

Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.0V to 3.0V
Output Load (Note 9)	R = 97.6Ω C_L = 30 pF
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V



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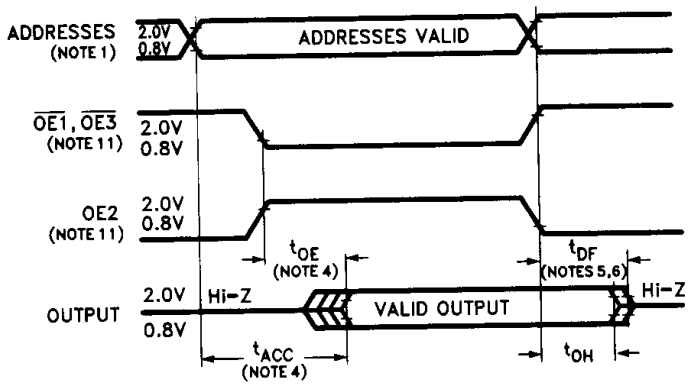
AC Waveforms (Notes 7, 8 & 11)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for T_A = 25°C and normal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: OE/$\overline{OE}$ true may be delayed up to $t_{ACC} - t_{OE}$ after address change without impacting t_{ACC}.

Note 5: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 6: TRI-STATE may be attained by any OE signal.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 9: C_L: 30 pF includes fixture capacitance.

Note 10: Inputs can undershoot −2.0V for a maximum of 20 ns.

Note 11: For the output to be in Low-Z all OE/$\overline{OE}$ inputs must be in their logical true states, i.e., $\overline{OE1}$, $\overline{OE3}$ must be at V_{IL} and OE2 must be at V_{IH}. If any or all of these inputs are not at their logical true level then the outputs will be in Hi-Z.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	OE2 Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay		0		50	ns
t_{PW}	Program Pulse Width		95	100	105	μs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$OE2 = V_{IL}$			60	mA
I_{CC}	V_{CC} Supply Current				60	mA
t_{VM1}	$\overline{OE3}$ to Data Valid (Verify Mode1)	$\overline{OE1}/V_{PP} = V_{PP}$, $OE2 = V_{IH}$			0.1	μs
t_{VM2}	OE2 to Data Valid (Verify Mode2)	$\overline{OE1}/V_{PP} = V_{PP}$, $\overline{OE3} = V_{IL}$			0.1	μs
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

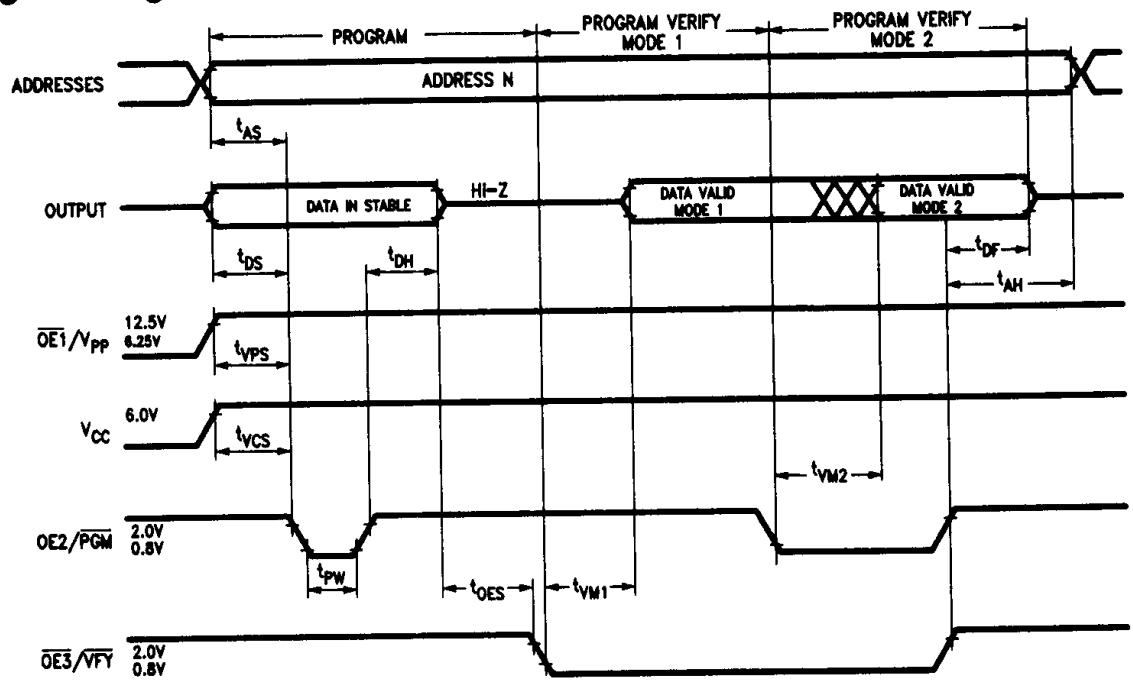
Note 1: National's standard product warranty applies only to devices programmed to the specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C53 must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not tested or guaranteed.

Programming Waveforms (Note 3)



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Fast Programming Algorithm Flow Chart

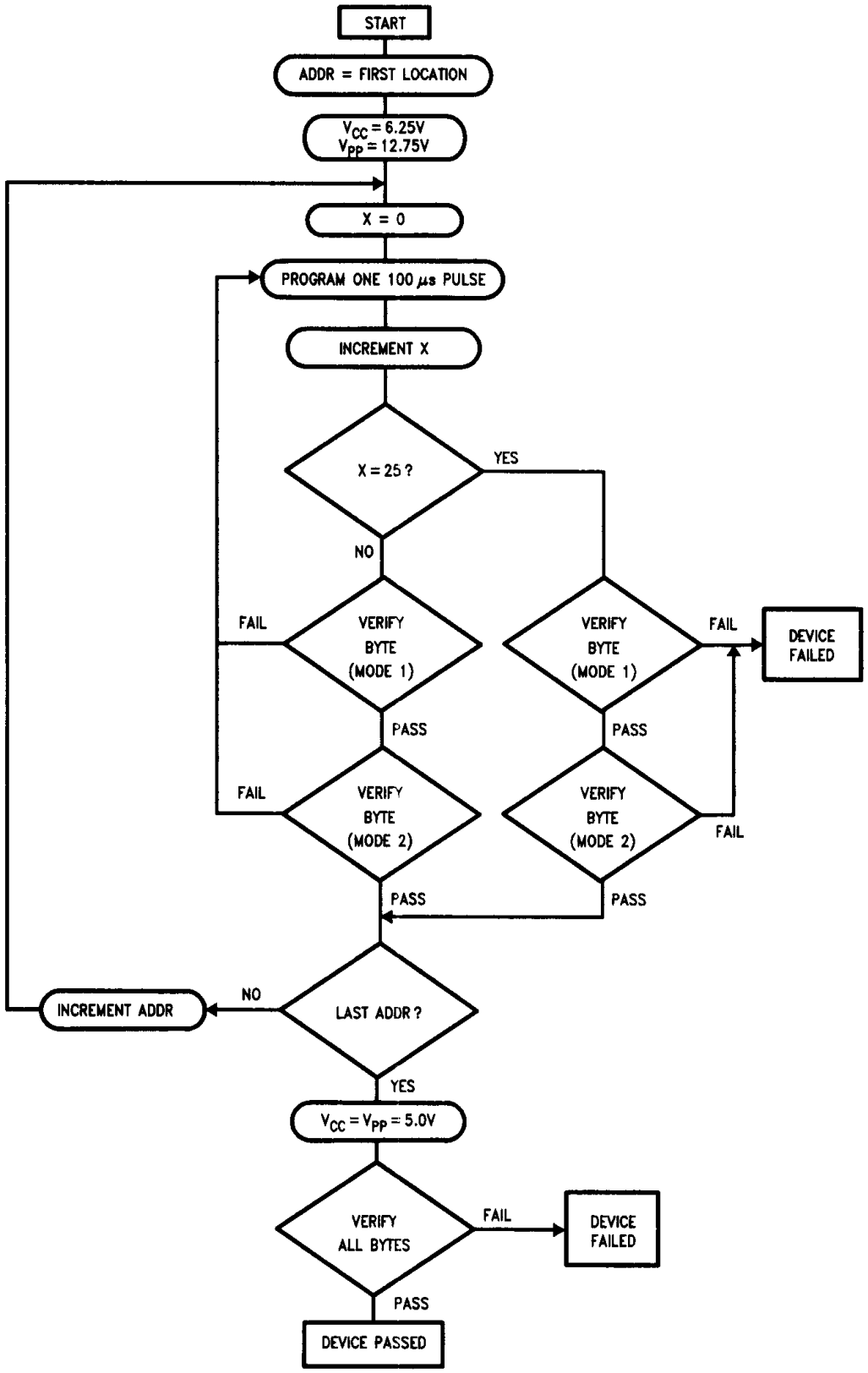

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FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C53 are listed in Table I. It should be noted that all inputs for the six modes may be at TTL levels. The power supplies required are V_{PP} and V_{CC}. The V_{CC} power supply must be at 6.25V during the four programming modes, and at 5V in the other two modes. The $\overline{OE1}/V_{PP}$ pin must be at 12.75V in the programming and verify mode, and V_{IL} in the read mode.

READ MODE

The NMC27C53 has three select functions, both of which must be logically active in order to obtain data at the outputs. Data is available at the falling edges of $\overline{OE1}$ and $\overline{OE3}$ and the rising edge of OE2, assuming that the addresses have been stable for at least $t_{ACC}-t_{OE}$. The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the specified voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

OUTPUT OR-TYING

Because NMC27C53s are usually used in larger memory arrays, National has provided a 3-line control function that accommodates this use of multiple memory connections. The 3-line control function allows for complete assurance that output bus contention will not occur. All Output Enables are functionally equivalent.

PROGRAMMING

CAUTION: Exceeding 14V on pin 22 ($\overline{OE1}/V_{PP}$) will damage the NMC27C53.

The NMC27C53 has a new memory cell which contributes greatly to its speed. The cell has two transistors which supply data to two data lines. When programmed, one or the other of the two transistors is programmed. When accessed the memory cell will discharge one of the two data lines, providing a differential voltage. This differential signal is then applied through pass devices to a true differential sense amplifier.

Initially, all memory cells are totally unprogrammed. In an unprogrammed state both transistors source the same current through the data lines and thus no differential is produced. Because of this, any attempt to read data in the read mode from an unprogrammed device will result in arbitrary outputs.

The NMC27C53 is in the program mode when $\overline{OE1}/V_{PP}$ is raised to 12.75V.

During programming the OE2 pin functions as the $\overline{PGM}$ pin which controls the programming pulse width (t_{PW}) and the $\overline{OE3}$ pin functions as the $\overline{VFY}$ pin which is to be held at V_{IL} during program verify.

To verify that a device is totally blank, the verify mode must be entered. In the verify mode each transistor of the memory cell is checked against a reference cell. By toggling OE2 both transistors in the cell are checked. For a totally unprogrammed deviced in the verify mode all outputs will be at a "1" state for OE2 = V_{IH} and at a "0" state for OE2 = V_{IL}.

It is required that at least a 0.1 μF capacitor be placed across $\overline{OE1}/V_{PP}$, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed are applied 8 bits in parallel to the data output pins. The levels required for the address, clock, and data inputs are TTL.

When the addresses, clocks, and data are stable, an active low, TTL program pulse is applied to the OE2 input. A program pulse must be applied to each address location that is to be programmed. A memory cell has been completely programmed when data from both verify modes matches the input data. The NMC27C53 is programmed with the fast programming algorithm shown in *Figure 1*. Each address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The NMC27C53 must not be programmed with a DC signal applied to the OE2 input.

Programming multiple NMC27C53s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C53s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$/OE2 input (with $\overline{OE3}$ high) programs the paralleled NMC27C53s.

PROGRAM INHIBIT

Programming multiple NMC27C53s in parallel with different data is also easily accomplished. Except for OE2 all like inputs (including $\overline{OE1}/V_{PP}$ and $\overline{OE3}$) of the paralleled NMC27C53s may be in common. A TTL low level applied to an NMC27C53s OE2/$\overline{PGM}$ input (with the other control pins at the appropriate levels) will program that NMC27C53 while keeping the same pin high on the others inhibits programming.

TABLE I. Mode Selection

Pins / Mode	$\overline{OE1}/V_{PP}$ (22)	OE2/$\overline{PGM}$ (21)	$\overline{OE3}/\overline{VFY}$ (20)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IH}	V_{IL}	5V	D_{OUT}
Program	12.75V	V_{IL}	V_{IH}	6.25V	D_{IN}
Program Verify (Mode 1)	12.75V	V_{IH}	V_{IL}	6.25V	D_{OUT} (V_{OH} if Blank)
Program Verify (Mode 2)	12.75V	V_{IL}	V_{IL}	6.25V	D_{OUT} (V_{OL} if Blank)
Program Inhibit	12.75V	V_{IH}	V_{IH}	6.25V	Hi-Z
Deselect	V_{IH}	V_{IL}	V_{IH}	5V	Hi-Z

Functional Description (Continued)

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine whether they were correctly programmed. Verifying in the read mode may not ensure that the bits have been programmed with adequate margins. To guarantee adequate margins the device should be verified in the verify mode. In this mode each transistor of the memory cell is checked against a reference cell. Verify mode is entered with $\overline{OE1}/V_{PP}$ at 12.75V and $\overline{OE3}/V_{IL}$ with OE2 at V_{IH}, the data read for verify mode 1, and at $OE2/\overline{PGM} = V_{IL}$, verify mode 2. The data read in both modes must be the same as the expected data for a completely programmed cell.

Manufacturer's Identification Code

The NMC27C53 has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is sorted in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C53 is "83C4", where "83" designates that it is made by National Semiconductor, and "C4" designates it is a 256k part.

The code is accessed by applying 12V ±0.5V to address pin A13. Addresses A1–A8, A10–A12, A14, $\overline{OE1}$, OE2 and $\overline{OE3}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

Erasure Characteristics

The erasure characteristics of the NMC27C53 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the NMC27C53's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C53 is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 W-sec/cm^2.

The NMC27C53 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C53 erasure time for various light intensities. An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.)

Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete ereaure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

System Consideration

The power switching characteristics of EPROMs require careful decoupling of devices. The supply current, I_{CC}, has two segments that are of interest to the system designer—the active current level and the transient current peaks that are produced by voltage transitions on the input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	0	0	1	1	83
Device Code	V_{IH}	1	1	0	0	0	1	0	0	C4

TABLE III. Minimum NMC27C53 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50