National Semiconductor

PRELIMINARY

NMC6514 4096-Bit (1024 × 4) Static RAM

General Description

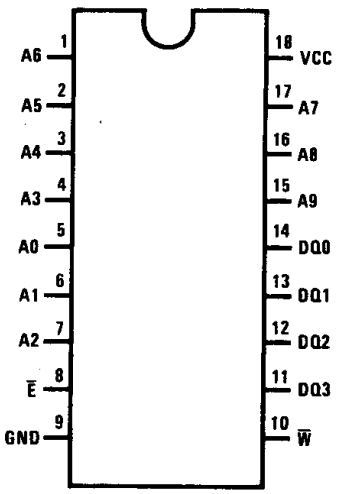
The NMC6514 is a static CMOS random access read/write memory organized as 1024 words of 4 bits each. This device is fabricated with National Semiconductor's silicon-gate CMOS technology and is fully compatible with the TTL environment. Synchronous operation is provided by on-chip address latches. The ENABLE input serves as the device strobe controlling the address latching function. The data I/O terminals, when not output data enabled, represent a high impedance for easy memory expansion.

Features

- Industry standard pinout
- Low data retention voltage — 2V
- Low speed/power product
- TTL compatible — all inputs and outputs
- TRI-STATE® outputs for bus operation
- High output drive
- High noise immunity
- Military temperature range available
- On-chip address registers (latches)
- Common I/O — high density packaging

Connection Diagram

Dual-In-Line Package



TOP VIEW

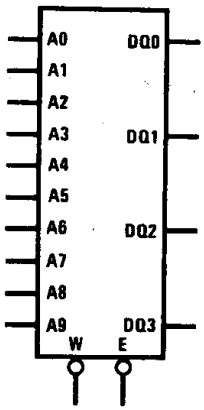
Order Number NMC6514J-2, NMC6514J-9 or NMC6514J-5
See NS Package J18A

Order Number NMC6514N-5
See NS Package N18A

Pin Names

A0–A9	Address Inputs
Ē	Chip Enable
W̄	Write Enable
DQ0–DQ3	Data In/Out

Logic Symbol



Functional Description

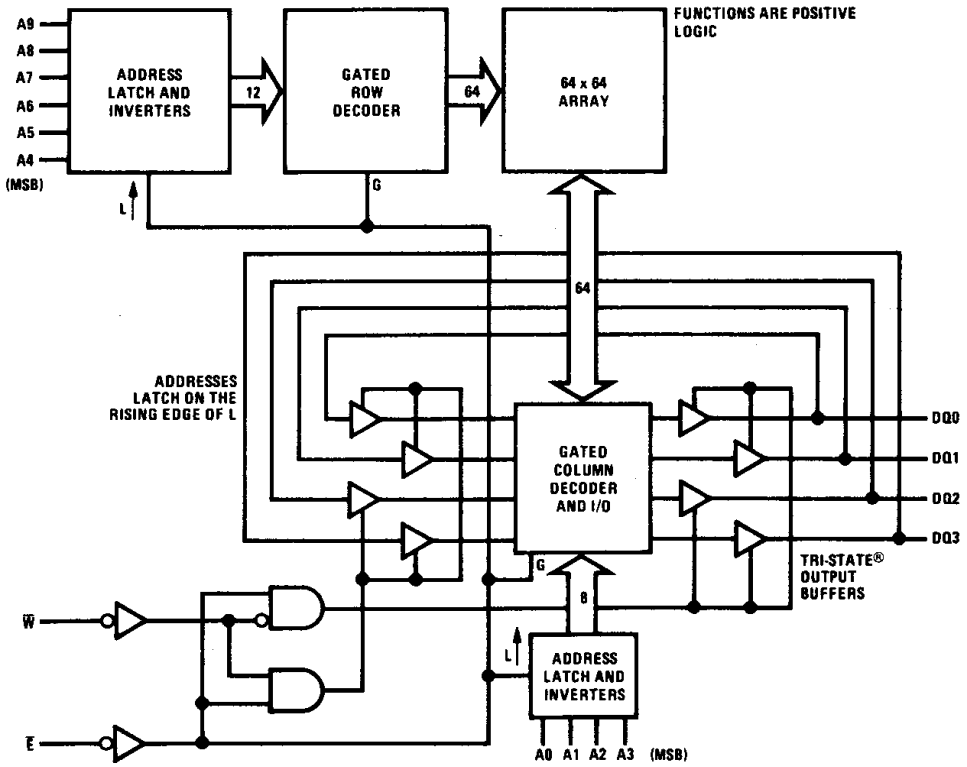
An NMC6514 memory cycle is initiated by the falling edge of the ENABLE ($\overline{E}$) input, which latches the address information into the on-chip registers. Read, write, the read-modify-write cycles are selected as a function of the ENABLE and WRITE ($\overline{W}$) input levels and timing. Data output is enabled by the falling edge of the ENABLE input and disabled by the rising edge when the WRITE input is HIGH. The output is disabled when writing.

When performing a read cycle a minimum ENABLE LOW time is required to assure valid data at the output. This minimum LOW time is defined as the device enable access time. A minimum ENABLE HIGH time is required to return the columns to the HIGH state and to precharge the sense amplifiers in preparation of the next cycle.

When performing a write cycle a minimum ENABLE LOW time is required to enter the new data. The write pulse is created by the coincident LOW of the ENABLE and WRITE inputs. The data set-up and hold time are referenced to the rising edge of either the ENABLE or WRITE inputs whichever occurs first.

A read-modify-write cycle is performed as a read cycle, for the enable access time, followed by the write pulse caused by the LOW time of the WRITE input. The output data is disabled by the falling edge of the WRITE input, and input data, meeting the set-up and hold requirements must be provided.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	7V
Voltage at Any Pin	−0.3V to VCC +0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Range

	Min	Max
Supply Voltage		
NMC6514-9	4.5V	5.5V
NMC6514-2	4.5V	5.5V
NMC6514-5	4.75V	5.25V
Temperature		
NMC6514-9	−40°C	85°C
NMC6514-2	−55°C	125°C
NMC6514-5	0°C	75°C

DC Electrical Characteristics over the operating range, unless otherwise noted

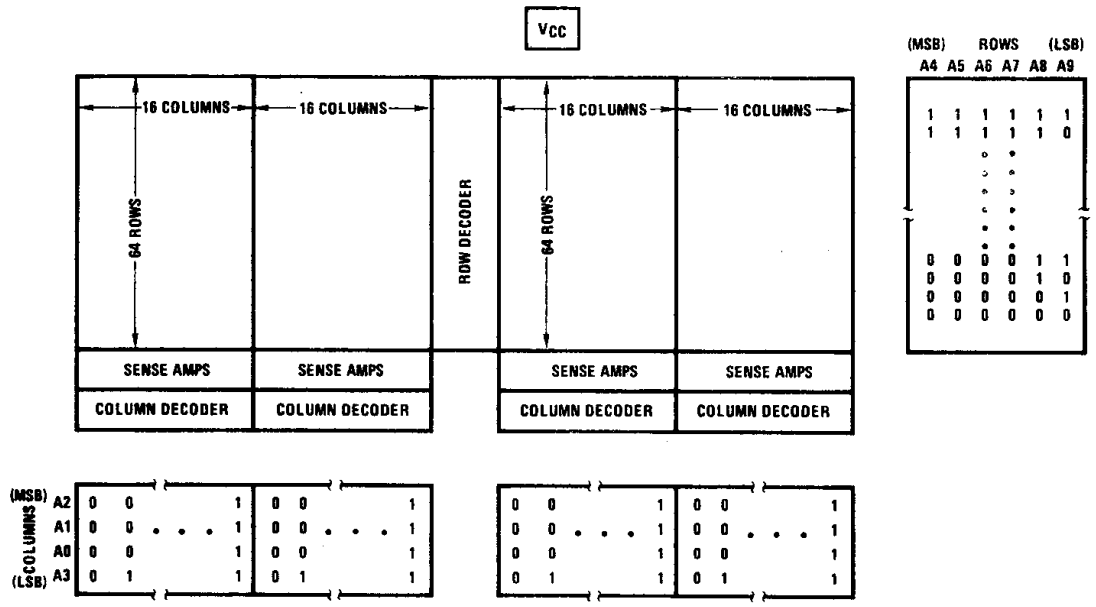
Symbol	Parameter	Conditions	NMC6514-9, NMC6514-2		NMC6514-5		Units
			Min	Max	Min	Max	
VCCDR	Data Retention Supply Voltage	VI = VCC, GND	2.0		2.0		V
ICCSB	Standby Supply Current			50		500	μA
ICCOP*	Operating Supply Current	f = 1 MHz, IO = 0, VI = VCC or GND		10		10	mA
ICCDR	Data Retention Supply Current	VCC = 3.0V, IO = 0, VI = VCC or GND		25		500	μA
II	Input Leakage Current	VI = VCC, GND	−1.0	+1.0	−10	+10	μA
VIL	Input Low Voltage		−0.3	0.8	−0.3	0.8	V
VIH	Input High Voltage		VCC − 2.0	VCC + 0.3	VCC − 2	VCC + 0.3	V
IOZ	Output Leakage Current	VI = VCC, GND	−1.0	+1.0	−10	+10	μA
VOL	Output Low Voltage	IOL = 2.0 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = −1.0 mA	2.4		2.4		V
CI	Input Capacitance	f = 1 MHz		8		8	pF
CO	Output Capacitance	f = 1 MHz		10		10	pF

* ICCOP is proportional to operating frequency.

AC Test Conditions

Input Rise and Fall Times: ≤20 ns
All Timing Reference Levels: 1/2 VCC
Output Load: 1 TTL Load, 50 pF

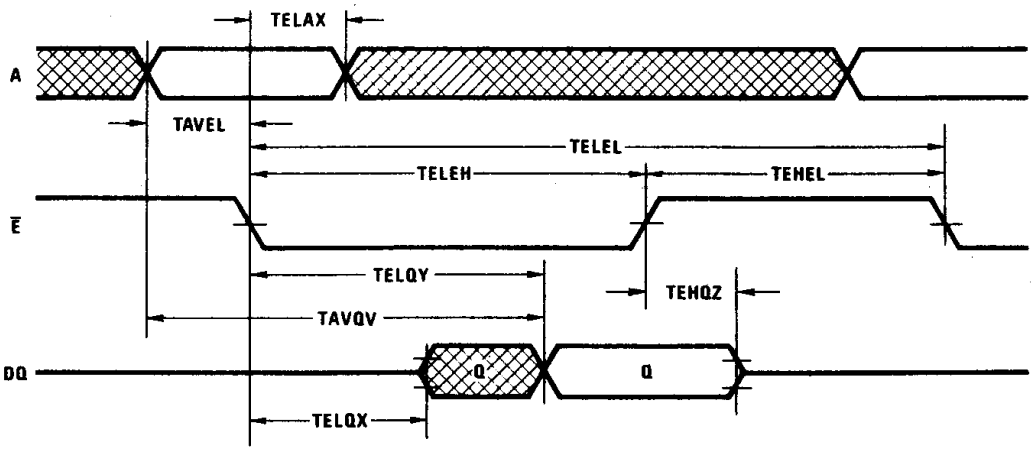
NMC6514 Bit Map and Address Decoding



Read Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6514-9, NMC6514-2		NMC6514-5		Units
		Min	Max	Min	Max	
TAVEL	Address Set-up Time	20		20		ns
TELAX	Address Hold Time	50		50		ns
TELQV	Enable Access Time		300		350	ns
TAVQV	Address Access Time		320		370	ns
TELEH	Enable ($\bar{E}$) Minimum Low Time	300		350		ns
TEHEL	Enable ($\bar{E}$) Minimum High Time	120		150		ns
TELQX	Output Enable from Enable ($\bar{E}$)		100		100	ns
TEHQZ	Output Disable from ($\bar{E}$)		100		100	ns
TELEL	Read or Write Cycle Time	420		500		ns

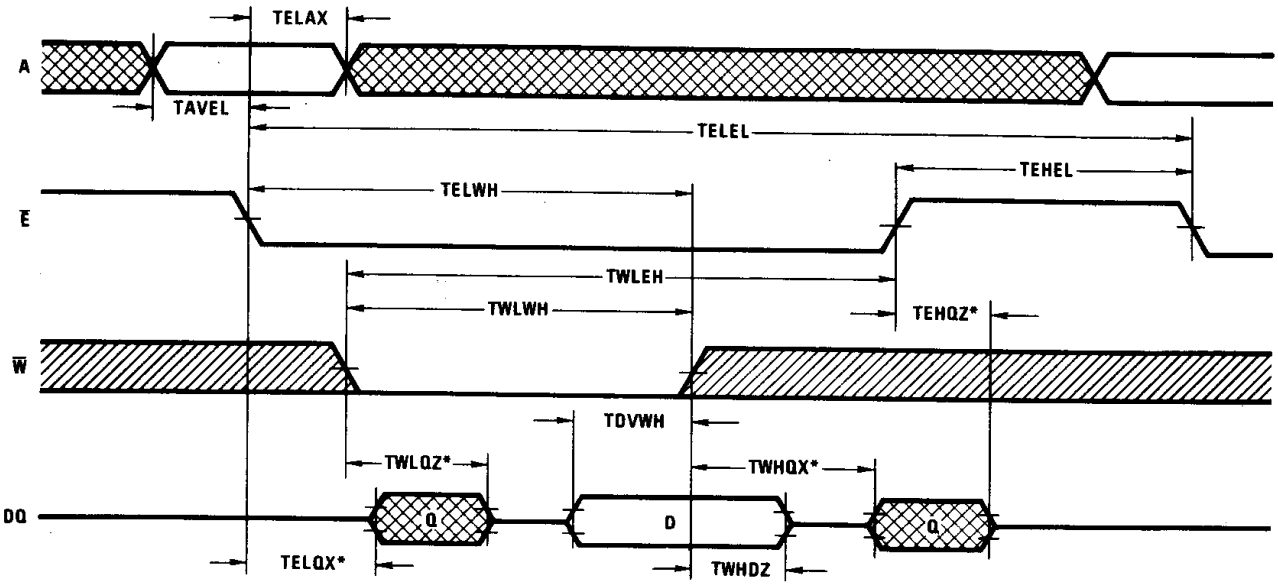
Read Cycle Waveforms



Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6514-9, NMC6514-2		NMC6514-5		Units
		Min	Max	Min	Max	
TAVEL	Address Set-up Time	20		20		ns
TELAX	Address Hold Time	50		50		ns
TWLEH	Write Pulse Width ($\bar{E}$ and $\bar{W}$ Low)	300		350		ns
TEHEL	Enable ($\bar{E}$) Minimum High Time	120		150		ns
TWLWH	Write Pulse Width ($\bar{W}$ Low)	300		350		ns
TELEL	Read or Write Cycle Time	420		500		ns
TWHQX	Output Enable from Write ($\bar{W}$)		100		100	ns
TELQX	Output Enable from Enable ($\bar{E}$)		100		100	ns
TEHQZ	Output Disable from Enable ($\bar{E}$)		100		100	ns
TWLQZ	Output Disable from Write ($\bar{W}$)		100		100	ns
TDVWH	Data Set-up Time	200		250		ns
TWHDZ	Data Hold Time	0		0		ns
TELWH	Write Pulse Width ($\bar{E}$ and $\bar{W}$ Low)	300		350		ns

Write Cycle Waveforms

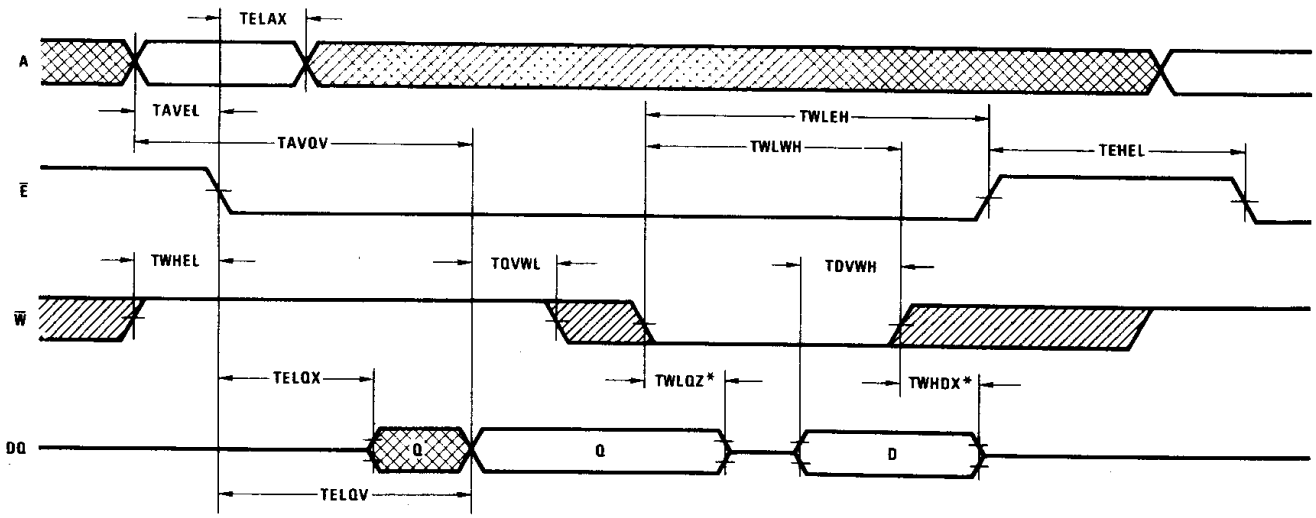


* Avoid bus contention

Read-Modify-Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6514-9, NMC6514-2		NMC6514-5		Units
		Min	Max	Min	Max	
TAVEL	Address Set-up Time	20		20		ns
TELAX	Address Hold Time	50		50		ns
TELQV	Enable Access Time		300		350	ns
TAVQV	Address Access Time		320		370	ns
TWLQZ	Output Disable from Write ($\overline{W}$)		100		100	ns
TDVWH	Data Set-up Time	200		250		ns
TWHDX	Data Hold Time	0		0		ns
TWLEH	Write Pulse Width ($\overline{W}$ and $\overline{E}$ Low)	300		350		ns
TQVWL	Data Valid to Write Time	0		0		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	300		350		ns
TELQX	Output Enable from Enable ($\overline{E}$)		100		100	ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	120		150		ns
TWHEL	$\overline{W}$ Read Mode Set-up Time	0		0		ns

Read-Modify-Write Cycle Waveforms



* Avoid bus contention