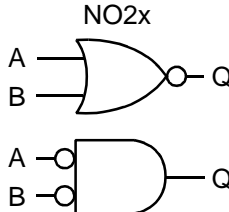


## AMI5HG 0.5 micron CMOS Gate Array

### Description

NO2x is a family of 2-input gates which perform the logical NOR function.

Logic Symbol	Truth Table															
 <p>The image shows two logic symbols. The top one is a NOR gate with two inputs labeled A and B, and one output labeled Q. The bottom one is an AND gate with two inputs labeled A and B, and one output labeled Q. Both inputs of the AND gate have small circles (bubbles) next to them, indicating inversion.</p>	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>H</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> </tr> </tbody> </table>	A	B	Q	L	L	H	L	H	L	H	L	L	H	H	L
A	B	Q														
L	L	H														
L	H	L														
H	L	L														
H	H	L														

### HDL Syntax

Verilog ..... NO2x *inst\_name* (Q, A, B);

VHDL..... *inst\_name*: NO2x port map (Q, A, B);

### Pin Loading

Pin Name	Equivalent Loads				
	NO21	NO22	NO23	NO24	NO26
A	1.0	2.1	4.1	2.1	2.1
B	1.0	2.1	4.2	2.1	2.1

### Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics <sup>a</sup>	
		Static I <sub>DD</sub> (T <sub>J</sub> = 85°C) (nA)	EQL <sub>pd</sub> (Eq-load)
NO21	1.0	TBD	0.9
NO22	2.0	TBD	2.0
NO23	4.0	TBD	3.9
NO24	6.0	TBD	10.7
NO26	6.0	TBD	11.6

a. See page 2-15 for power equation.

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### Propagation Delays (ns)

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

	Number of Equivalent Loads		1	2	5	8	10 (max)
	NO21	From: Any Input	$t_{PLH}$	0.14	0.20	0.36	0.52
To: Q		$t_{PHL}$	0.13	0.17	0.28	0.37	0.42
NO22	Number of Equivalent Loads		1	4	8	13	17 (max)
	From: Any Input	$t_{PLH}$	0.09	0.18	0.29	0.42	0.51
	To: Q	$t_{PHL}$	0.10	0.16	0.23	0.31	0.37
NO23	Number of Equivalent Loads		1	8	15	22	30 (max)
	From: Any Input	$t_{PLH}$	0.09	0.17	0.25	0.35	0.46
	To: Q	$t_{PHL}$	0.09	0.16	0.22	0.26	0.31
NO24	Number of Equivalent Loads		1	14	28	42	56 (max)
	From: Any Input	$t_{PLH}$	0.35	0.45	0.56	0.66	0.75
	To: Q	$t_{PHL}$	0.30	0.45	0.58	0.71	0.83
NO26	Number of Equivalent Loads		1	21	42	62	83 (max)
	From: Any Input	$t_{PLH}$	0.41	0.51	0.61	0.69	0.79
	To: Q	$t_{PHL}$	0.35	0.50	0.61	0.70	0.79

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Core  
Logic