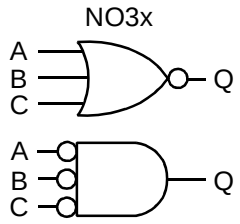
Description

NO3x is a family of 3-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

HDL Syntax

Verilog ..... NO3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: NO3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads				
	NO31	NO32	NO33	NO34	NO36
A	1.0	2.1	2.1	2.1	2.1
B	1.0	2.1	2.1	2.1	2.1
C	1.0	2.1	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NO31	2.0	TBD	1.9
NO32	3.0	TBD	3.2
NO33	6.0	TBD	8.7
NO34	7.0	TBD	10.7
NO36	7.0	TBD	13.3

a. See page 2-15 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NO31	**Number of Equivalent Loads**		**1**	**2**	**4**	**6**	**8 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.19 0.14	0.27 0.18	0.43 0.26	0.58 0.32	0.73 0.38
NO32	**Number of Equivalent Loads**		**1**	**3**	**6**	**9**	**12 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.13 0.11	0.20 0.15	0.31 0.21	0.41 0.26	0.52 0.30
NO33	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.40 0.31	0.49 0.43	0.59 0.54	0.70 0.64	0.81 0.76
NO34	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.43 0.30	0.55 0.42	0.66 0.52	0.76 0.62	0.89 0.74
NO36	**Number of Equivalent Loads**		**1**	**21**	**42**	**62**	**83 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.42 0.38	0.53 0.50	0.64 0.61	0.73 0.70	0.84 0.80

Delay will vary with input conditions. See page 2-17 for interconnect estimates.