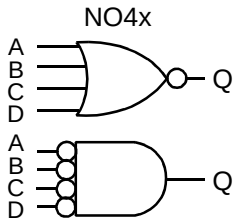
Description

NO4x is a family of 4-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

HDL Syntax

Verilog ..... NO4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: NO4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads				
	NO41	NO42	NO43	NO44	NO46
A	1.0	1.0	2.1	2.1	2.1
B	1.0	1.0	2.1	2.1	2.1
C	1.0	1.0	2.1	2.1	2.1
D	1.0	1.0	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NO41	2.0	TBD	2.2
NO42	4.0	TBD	7.0
NO43	6.0	TBD	9.4
NO44	7.0	TBD	11.4
NO46	8.0	TBD	14.1

a. See page 2-15 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NO41	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.24 0.16	0.34 0.19	0.53 0.26	0.63 0.29	0.83 0.36
NO42	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.40 0.34	0.50 0.45	0.62 0.58	0.77 0.73	0.90 0.85
NO43	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.46 0.32	0.57 0.45	0.66 0.56	0.75 0.66	0.85 0.77
NO44	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.52 0.34	0.63 0.47	0.75 0.55	0.86 0.65	0.97 0.77
NO46	**Number of Equivalent Loads**		**1**	**21**	**42**	**62**	**83 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.57 0.37	0.68 0.49	0.79 0.60	0.88 0.69	0.96 0.79

Delay will vary with input conditions. See page 2-17 for interconnect estimates.