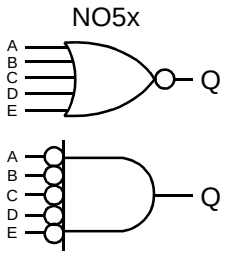
Description

NO5x is a family of 5-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	H
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L

HDL Syntax

Verilog ..... NO5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: NO5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads				
	NO51	NO52	NO53	NO54	NO56
A	1.0	1.0	2.1	2.1	2.1
B	1.0	1.0	2.1	2.1	2.1
C	1.0	1.0	2.1	2.1	2.1
D	1.0	1.0	2.1	2.1	2.1
E	1.0	1.0	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static IDD (TJ = 85°C) (nA)	EQLpd (Eq-load)
NO51	3.0	TBD	3.2
NO52	4.0	TBD	7.6
NO53	8.0	TBD	10.7
NO54	10.0	TBD	18.1
NO56	12.0	TBD	17.9

a. See page 2-15 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NO51	**Number of Equivalent Loads**		**1**	**2**	**3**	**4**	**6 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.22 0.15	0.33 0.18	0.43 0.22	0.54 0.25	0.78 0.31
NO52	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.40 0.34	0.51 0.44	0.63 0.57	0.78 0.73	0.89 0.85
NO53	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.42 0.34	0.55 0.47	0.65 0.58	0.75 0.69	0.85 0.80
NO54	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.46 0.36	0.58 0.50	0.68 0.61	0.76 0.70	0.84 0.79
NO56	**Number of Equivalent Loads**		**1**	**21**	**42**	**62**	**83 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.51 0.34	0.62 0.52	0.71 0.65	0.81 0.75	0.92 0.83

Delay will vary with input conditions. See page 2-17 for interconnect estimates.