NOIL1SM4000A

LUPA4000: 4 MegaPixel High Speed CMOS Sensor

ON Semiconductor®

http://onsemi.com

Features

- 2048 x 2048 Active Pixels
- 12 μm x 12 μm Square Pixels
- 24.6 mm x 24.6 mm Optical Format
- Monochrome or Color Digital Output
- 15 Frames per Second (fps) at Full Resolution
- Pipelined Global Shutter
- Random Programmable Region of Interest (ROI) Readout and Subsampling Modes
- Serial Peripheral Interface (SPI)
- Operational Range: 0°C to 60°C
- 127-Pin PGA Package
- 220 mW Power Dissipation
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Intelligent Traffic System
- High Speed Machine Vision

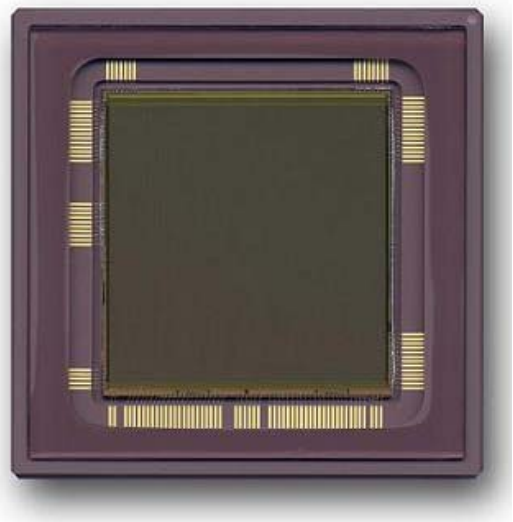


Figure 1. LUPA4000 Photo

Overview

The LUPA4000 is a CMOS image sensor (CIS) with a 4.0 megapixel resolution 2048 x 2048 pixel format.

This document describes the interfacing and driving of the LUPA4000 image sensor. This 4 megapixel CMOS active pixel sensor features synchronous shutter and a maximal frame rate of 15 fps in full resolution. The readout speed can be boosted by sub-sampling and windowed ROI readout. High dynamic range scenes can be captured using the double and multiple slope functionality.

The sensor uses a 3-wire SPI and is housed in a 127-pin ceramic PGA package. The LUPA4000 is available in mono and color option.

ORDERING INFORMATION

Marketing Part Number	Description	Package
NOIL1SM4000A-GDC	Mono with Glass	127−pin PGA
NOIL1SC4000A-GDC	Color with Glass	

NOTE: Refer to Ordering Code Definition on page 26 for more information.

CONTENTS

SPECIFICATIONS

Key Specifications

GENERAL SPECIFICATIONS

Parameter	Specifications
Active pixels	2048 x 2048
Pixel size	12 μm x 12 μm
Optical format	24.6 mm x 24.6 mm
Pixel type	Global shutter pixel architecture
Shutter type	Pipelined global shutter
Master clock	33 MHz
Windowing (ROI)	Randomly programmable ROI
Readout	Windowed and subsampled readout possible
Power dissipation	200 mW
Package type	127 PGA

ELECTRO−OPTICAL SPECIFICATIONS

Parameter	Typical Specifications
Frame rate	15 fps at full resolution
Conversion gain	11.5 μV/e^-
Responsivity at 550 nm	1550 (V/s)/(W/m^2)
Fill factor (FF)	37.5%
Parasitic light sensitivity	< 1/7600 at 550 nm
Full well charge	95700 e^-
Quantum efficiency (QE)	36% (QE x FF)
Fixed pattern noise (FPN)	16 mV
Photo response nonuniformity (PRNU)	3% of signal
Dynamic range	66 dB (single slope), 90 dB (multiple slope)
Dark signal	22 mV/s at +20°C with 50 ms integration time
Dark signal doubling temperature	8.65°C

Absolute Maximum Ratings

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Description	Min	Max	Units
ABS (2.5 V supply group)	ABS rating for 2.5 V supply group	−0.5	2.9	V
ABS (3.3 V supply group)	ABS rating for 3.3 V supply group	−0.5	4.0	V
Electrostatic discharge (ESD) (Note 3)	Human body model (HBM)	(Note 4)		
	Charged device model (CDM)			
Latch−up	Latch−up rating	(Note 5)		
T_S (Note 3)	ABS Storage temperature range	−40	+150	°C
	ABS Storage humidity range at 85°C		85	%RH

RECOMMENDED OPERATING RATINGS

T_J (Note 2)	Humidity (Relative)	0	60	°C

1. Absolute maximum ratings are limits beyond which damage may occur. Exceeding the maximum ratings may impair the useful life of the device.
2. Operating ratings are conditions at which operation of the device is intended to be functional.
3. ON Semiconductor recommends that customers become familiar with, and follow the procedures in, JEDEC Standard JESD625−A. Refer to Application Note AN52561.
4. The LUPA4000 complies with JESD22−A114 HBM Class 0 and JESD22−C101 Class I. It is recommended that extreme care be taken while handling these devices to avoid damages due to ESD event.
5. The LUPA4000 does not have latch−up protection.

Electrical Specifications

POWER SUPPLY RATINGS

Limits in **bold** apply for $T_J = T_{MIN}$ to T_{MAX}, all other limits $T_J = +30°C$ (Notes 1 and 3)

Parameter	Description	Min	Typ	Max[2]	Units
Power Supply Parameters					
Vdd	Core digital supply	**−10%**	2.5	**+10%**	V
Idd	Core digital current	–	1	200	mA
Vaa	Analog supply voltage	**−10%**	2.5	**+10%**	V
Iaa	Analog supply current	–	7	50	mA
Vpix	Pixel supply voltage	**−5%**	2.6	**+5%**	V
Ipix	Pixel supply current	–	12	500	mA
Voo	Output stage power supply	**−10%**	2.5	**+10%**	V
Ioo	Output stage current	–	20	–	mA
Va3	Column readout module supply	**−1%**	3.3	**+1%**	V
Ia3	Column readout module current	–	10	50	mA
Vmem_l	Power supply memory element (low level)	**−5%**	2.6	**+5%**	V
Imem_l	Power supply memory element current (low level)	–	1	200	mA
Vmem_h	Power supply memory element (high level)	**−5%**	3.3	**+5%**	V
Imem_h	Power supply memory element current (high level)	–	1	200	mA
Vres	Power supply to reset drivers	**−5%**	3.5	**+5%**	V
Ires	Power supply current to reset drivers	–	1	200	mA
Vres_ds	Power supply to multiple slope drivers	**−5%**	2.5	**+5%**	V
Ires_ds	Power supply current to multiple slope drivers	–	1	200	mA
Vpre_l	Power supply for pre-charge off-state	**−0.4**	0	**0**	V
Vddd	Digital supply to ADC drivers	**−10%**	2.5	**+10%**	V
Iddd	Digital supply current to ADC drivers	–	1	200	mA
Vdda	Analog supply to ADC drivers	**−5%**	2.5	**+5%**	V
Idda	Analog supply current to ADC drivers	–	1	200	mA
Pd	Total power consumption	–	200	–	mW
Sensor Requirements					
fps	Frame rate at full resolution (global shutter)	–	–	15	fps
fps_roi1	Xres x Yres = 1024 x 2048	–	–	31	fps
fps_roi2	Xres x Yres = 1024 x 1024	–	–	62	fps
fps_roi3	Xres x Yres = 640 x 480	–	–	210	fps
FOT	Frame overhead time	–	5	–	μs
ROT	Row overhead time (can be further reduced)	–	200	–	ns

1. All parameters are characterized for DC conditions after thermal equilibrium is established.
2. The maximum currents are peak currents which occur once per frame.
3. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high−impedance circuit.

OVERVIEW

The LUPA4000 CMOS active pixel sensor features a global shutter with a maximum frame rate of 15 fps in full resolution. The readout speed is boosted by sub sampling and the windowed ROI readout. High dynamic range scenes can be captured using the multiple slope functionality. Subsampling reduces resolution while maintaining the constant field of view and an increased frame rate.

The sensor uses a 3-wire SPI. It requires only one master clock for operation up to 15 fps. The sensor is available in a monochrome version or Bayer (RGB) patterned color filter array. It is placed in a 127-pin ceramic PGA package.

Color Filter Array

The color version of LUPA4000 is available in Bayer (RGB) patterned color filter array. The orientation of RGB is shown in Figure 2.

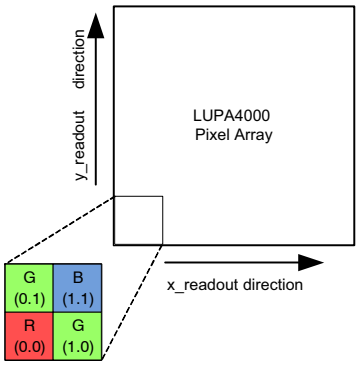


Figure 2. Color Filter Array

The spectral response for the mono and color device is shown in Figure 3.

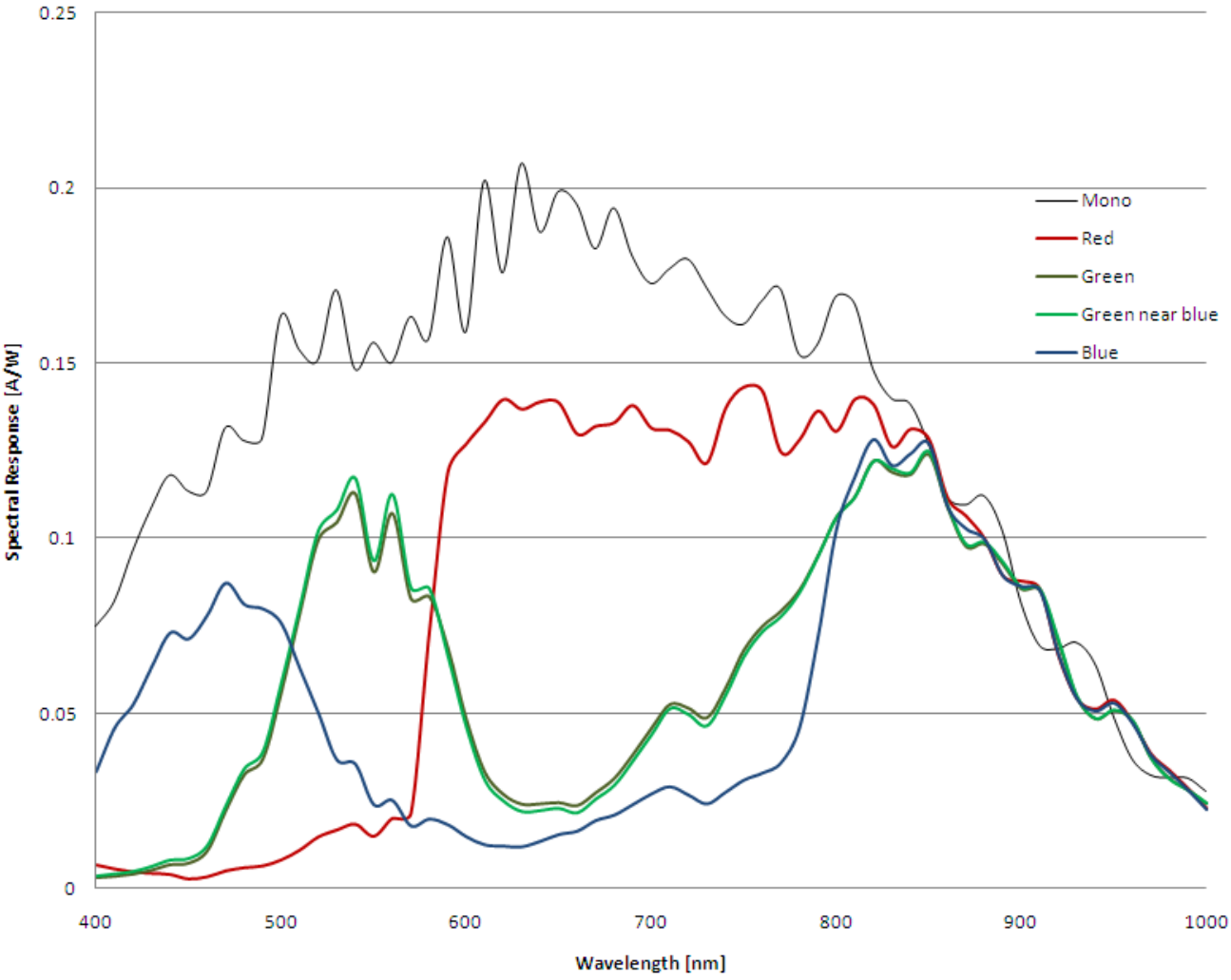


Figure 3. Spectral Response Curve for Mono and Color

SENSOR ARCHITECTURE

The LUPA4000 architecture is shown in Figure 4.

Image Core

The image core consists of a pixel array, one X-addressing and two Y-addressing registers (only one drawn), pixel array drivers, and column amplifiers.

The active pixel area is read out in progressive scan by one or two output amplifiers. The output amplifiers operate at a nomimal speed of 66-MHz pixel rate, or 33-MHz pixel rate if two output amplifiers are used to read out the imager. The image sensor is designed for operation up to 66 MHz.

The structure allows having a programmable addressing in the x-direction and y-direction in steps of two. Only even start addresses in x-direction and y-direction are possible. The starting point of the address can be uploaded using the SPI.

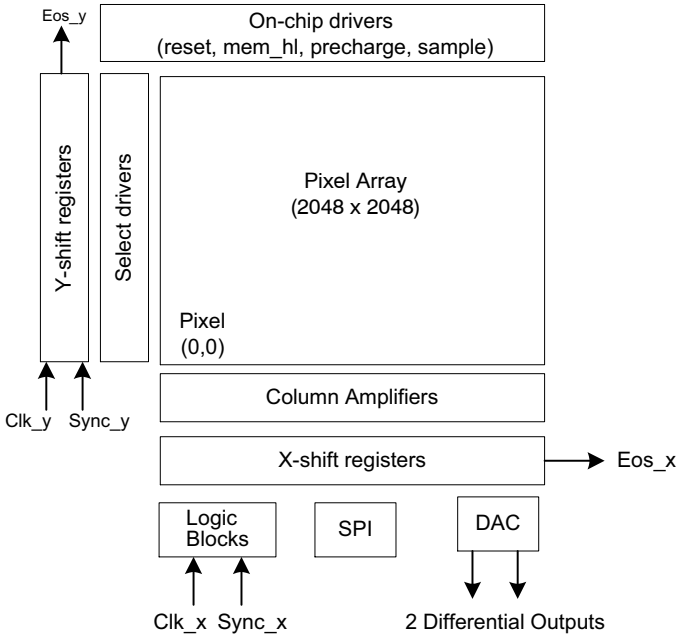


Figure 4. Block Diagram of Image Sensor

Output Amplifier

The sensor has two output amplifiers. A single amplifier can be operated at 66 Mpixels/sec to bring the whole pixel array of 2048 by 2048 pixels at the required frame rate. The second output amplifier can be enabled in parallel if the clock frequency is decreased to 33 Msamples/sec. Using only one output-stage, the output signal is the result of multiplexing between the two internal buses. When using two output-stages, both outputs are in phase.

Each output-stage has two outputs. One output is the pixel signal; the second output is a DC signal, which offset can be programmed using a 7-bit word. The DC signal is used for common mode rejection between the two signals. The disadvantage is an increase in power dissipation. However, this can be reduced by setting the highest DAC voltage using the SPI.

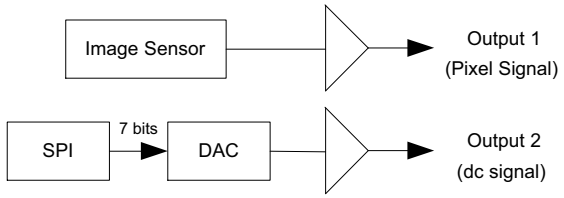


Figure 5. Output Stage Architecture

The output voltage of Output 1 is between 1.3 V (dark level) and 0.3 V (white level) and depends on process variations and voltage supply settings. The output voltage of Output2 is determined by the DAC.

Pixel Array Drivers

The image sensor has on-chip drivers for the pixel array signals The driving on system level is easy and flexible; the maximum currents applied to the sensor are also controlled on-chip. This means that the charging on sensor level is fixed; the sensor cannot be overdriven externally. The operation of the on-chip drivers is explained in Timing and Readout of Image Sensor on page 13.

Column Amplifiers

The column amplifiers are designed for minimum power dissipation and minimum loss of signal, resulting in multiple biasing signals.

The column amplifiers have an integrated ‘voltage-averaging’ feature. In the voltage-averaging mode, the voltage average between two columns is read out. In this mode, only 2:1 pixels must be read out.

To achieve the voltage-averaging mode, an additional external digital signal called voltage-averaging is required in combination with a bit from the SPI.

Analog-to-Digital Converter

The LUPA4000 has two 10-bit flash ADCs running nominally at 10 Msamples/s. The ADC block is electrically separated from the image sensor. The inputs of the ADC must be tied externally to the outputs of the output amplifiers. If the internal ADC is not used, then the power supply pins to the ADC and the I/Os must be grounded.

Even in this configuration, the internal ADCs are not able to sustain the 66 Mpixel/sec provided by the output amplifier when run at full speed.

One ADC samples the even columns and the second ADC samples the odd columns. Although the input range of the ADC is between 1 V and 2 V and the output range of the analog signal is between 0.3 V and 1.3 V, the analog output and digital input may be tied to each other directly. This is possible because there is an on-chip level-shifter located in front of the ADC to lift up the analog signal to the ADC range.

Errata for Internal ADCs

Use external ADCs due to the limitation of the internal ADC clock, not operational at system clock. No fix is intended to resolve this limitation.

Table 1. ADC SPECIFICATIONS

Parameter	Specification
Input range	1 V to 2 V (Note 1)
Quantization	10 bits
Normal data rate	10 Msamples/s
Differential nonlinearity (DNL) - linear conversion mode	Typ. < 0.4 LSB RMS
Integral nonlinearity (INL) - linear conversion mode	Typ. < 3.5 LSB
Input capacitance	< 2 pF
Power dissipation at 33 MHz	50 mW
Conversion law	Linear/Gamma−corrected

1. The internal ADC range is typically 50 mW lower than the external applied ADC_VHIGH and ADC_VLOW voltages due to voltage drops over parasitic internal resistors in the ADC.

ADC Timing

The ADC converts the pixel data on the falling edge of the ADC_CLOCK, but it takes two clock cycles before this pixel data is at the output of the ADC. This pipeline delay is shown in Figure 6.

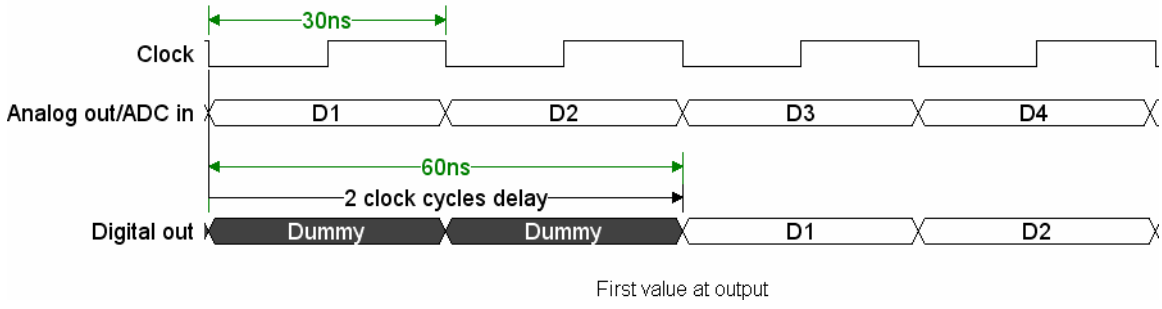


Figure 6. ADC Timing

Setting ADC Reference Voltages

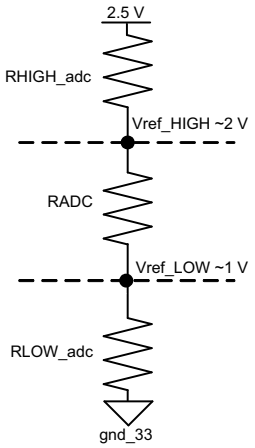


Figure 7. Internal and External ADC Connections

The internal resistor R_{ADC} has a value of approximately 300 Ω. The value of this resistor is not tested at sort or at final test. Some modification may be required as the recommended resistors in Figure 7 are determined by trade−off between speed and power consumption.

Resistor	Typical Value (Ω)
R_{ADC_VHIGH}	75
R_{ADC}	300
R_{ADC_VLOW}	220

OPERATING MODES

The LUPA4000 sensor operates in the global shutter mode.

Global Shutter Mode

In the global shutter mode, light integration takes place on all pixels in parallel, although subsequent readout is sequential. Figure 8 shows the integration and readout sequence for the synchronous shutter. All pixels are light sensitive at the same period of time. The whole pixel core is reset simultaneously; after the integration time, all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that the integration and readout can occur in parallel or sequentially.

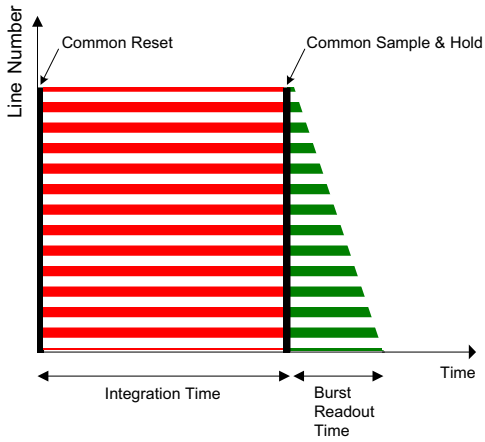


Figure 8. Global Shutter Operation

Pipelined Global Shutter

In pipelined global shutter mode, the integration and readout are done in parallel. Images are continuously read and integration of frame N is ongoing during readout of the previous frame N-1. The readout of every frame starts with an FOT, during which the analog value on the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line by line and the readout of each line is preceded by the ROT. Figure 9 shows the exposure and readout timeline in pipelined global shutter mode.

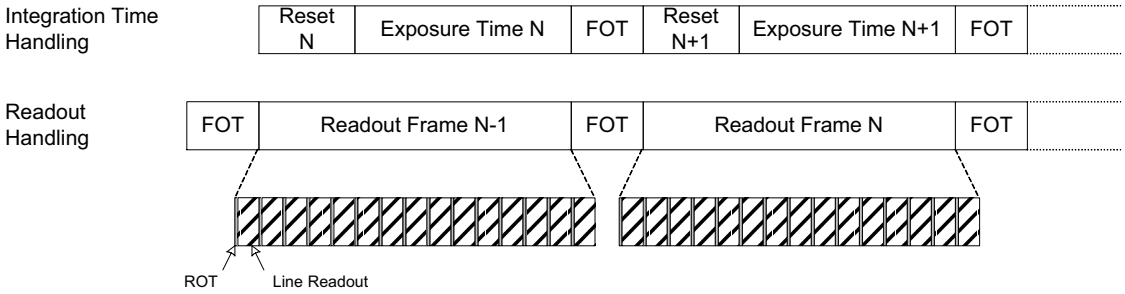


Figure 9. Integration and Readout for Pipelined Shutter

Non Destructive Readout (NDR)

The sensor can also be read out in a non destructive way. After a pixel is initially reset, it can be read multiple times without resetting. The initial reset level and all intermediate signals can be recorded. High light levels saturate the pixels quickly, but a useful signal is obtained from the early samples. For low light levels, use the latest samples.

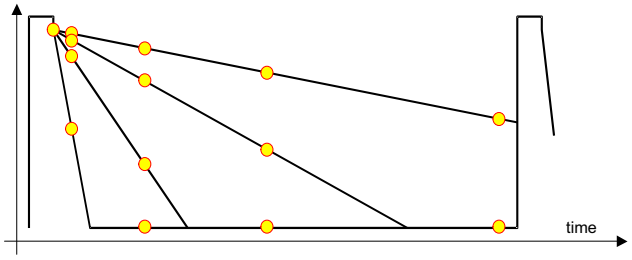


Figure 10. Principle of NDR

An active pixel array is read multiple times and reset only once. The external system intelligence takes care of the interpretation of the data. Table 2 summarizes the advantages and disadvantages of non-destructive readout.

Table 2. ADVANTAGES & DISADVANTAGES OF NDR

Advantages	Disadvantages
Low noise, because it is true correlated double sampling (CDS).	System memory required to record the reset level and the intermediate samples.
High sensitivity, because the conversion capacitance is kept low.	Requires multiples readings of each pixel, thus higher data throughput.
High dynamic range, because the results includes signal for short and long integrations times.	Requires system level digital calculations.

OPERATION AND SIGNALLING

The signals are classified into the following groups:

- Power supplies and grounds
- Biasing and analog signals
- Pixel array signals
- Digital signals
- Test signals

Power Supplies and Ground

Every module on chip including column amplifiers, output stages, digital modules, and drivers has its own power supply and ground. Off chip, the grounds can be combined, but not all power supplies may be combined. This results in several different power supplies, but this is required to reduce electrical cross-talk and improve shielding, dynamic range, and output swing.

On chip, the ground lines of every module are kept separately to improve shielding and electrical cross talk between them.

An overview of the supplies is given in Electrical Specifications on page 4. The maximum currents mentioned in the specifications table are peak currents which occur once per frame (except for Vres_ds in multiple slope mode). All power supplies should be able to deliver these currents except for Vmem_l and Vpre_l, which must be able to sink this current.

The maximum peak current for Vpix should not be higher than 500 mA. Note that no power supply filtering on chip is implemented and noise on these power supplies can contribute immediately to the noise on the signal. The voltage supplies Vpix and Vaa must be noise free.

Startup Sequence

The LUPA4000 goes in latch-up (draw high current) when all power supplies are turned on simultaneously. The sensor comes out of latch-up and starts working normally as soon as it is clocked. A power supply current limit of 400 mA is recommended to avoid damage to the sensor. Avoid the time that the device is in the latch-up state, so clocking of the sensor should start as soon as the system is turned on.

To avoid latch-up of the sensor, follow this sequence:

1. Apply Vdd
2. Apply clocks and digital pulses to the sensor to count 1024 clock_x and 2048 clock_y pulses to empty the shift registers
3. Apply other supplies

Biasing and Analog Signals

The expected analog output levels are between 0.3 V for a white, saturated, pixel and 1.3 V for a black pixel.

There are two output stages, each consisting of two output amplifiers, resulting in four outputs. One output amplifier is used for the analog signal resulting from the pixels. The second amplifier is used for a DC reference signal. The DC level from the buffer is defined by a DAC, which is controlled by a 7-bit word downloaded in the SPI. Additionally, an extra bit in the SPI defines if one or two output stages are used.

Table 3 summarizes the biasing signals required to drive this image sensor. To optimize biasing of column amplifiers to power dissipation, several biasing resistors are required. This optimisation results in an increase of signal swing and dynamic range.

Table 3. OVERVIEW OF BIAS SIGNALS

Signal	Comment	Related Module	DC Level
Out_load	Connect with 60 KΩ to Voo and capacitor of 100 nF to Gnd	Output stage	0.7 V
dec_x_load	Connect with 2 MΩ to Vdd and capacitor of 100 nF to Gnd	X-addressing	0.4 V
muxbus_load	Connect with 25 KΩ to Vaa and capacitor of 100 nF to Gnd	Multiplex bus	0.8 V
nsf_load	Connect with 5 KΩ to Vaa and capacitor of 100 nF to Gnd	Column amplifiers	1.2 V
uni_load_fast	Connect with 10 KΩ to Vaa and capacitor of 100 nF to Gnd	Column amplifiers	1.2 V
uni_load	Connect with 1 MΩ to Vaa and capacitor of 100 nF to Gnd	Column amplifiers	0.5 V
pre_load	Connect with 3 KΩ to Vaa and capacitor of 100 nF to Gnd	Column amplifiers	1.4 V
col_load	Connect with 1 MΩ to Vaa and capacitor of 100 nF to Gnd	Column amplifiers	0.5 V
dec_y_load	Connect with 2 MΩ to Vdd and capacitor of 100 nF to Gnd	Y-addressing	0.4 V
psf_load	Connect with 1 MΩ to Vaa and capacitor of 100 nF to Gnd	Column amplifiers	0.5 V
precharge_bias	Connect with 1 kΩ to Vdd and capacitor of at least 200 nF to Gnd	Pixel drivers	1.4 V

Each biasing signal determines the operation of a corresponding module in the sense that it controls speed and dissipation. Some modules have two biasing resistors: one to achieve the high speed and another to minimize power dissipation.

Pixel Array Signals

The pixel array of the image sensor requires digital control signals and several different power supplies. This section explains the relation between the control signals and the applied supplies, and the internal generated pixel array signals.

Figure 11 illustrates the internal generated pixel array signals: Reset, Sample, Precharge, Vmem, and Row_select. These are internal generated signals derived by on-chip drivers from external applied signals. Row_select is generated by the y-addressing and is not discussed in this section

Reset: Resets the pixel and initiates the integration time. If reset is high, then the photodiode is forced to a certain voltage. This depends on Vpix (pixel supply) and the high level of reset signal. The higher these signals or supplies, the higher the voltage-swing. The limitation on the high level of reset and Vpix is 3.3 V. It does not help to increase Vpix without increasing the reset level. The opposite is true. Additionally, it is the reset pulse that also controls the dual or multiple slope feature inside the pixel. By giving a reset pulse during integration, but not at full reset level, the photodiode is reset to a new value, only if this value is decreased due to light illumination.

The low level of reset is 0 V, but the high level is 2.5 V or higher (3.3 V) for the normal reset and a lower (<2.5 V) level for the multiple slope reset.

Precharge: Precharge serves as a load for the first source follower in the pixel and is activated to overwrite the current information on the storage node by the new information on the photodiode. Precharge is controlled by an external digital signal between 0 V and 2.5 V.

Sample: Samples the photodiode information onto the memory element. This signal is also a standard digital level between 0 V and 2.5 V.

Vmem: This signal increases the information on the memory element with a certain offset. This increases the output voltage variation. Vmem changes between Vmem_l (2.5 V) and Vmem_h (3.3 V).

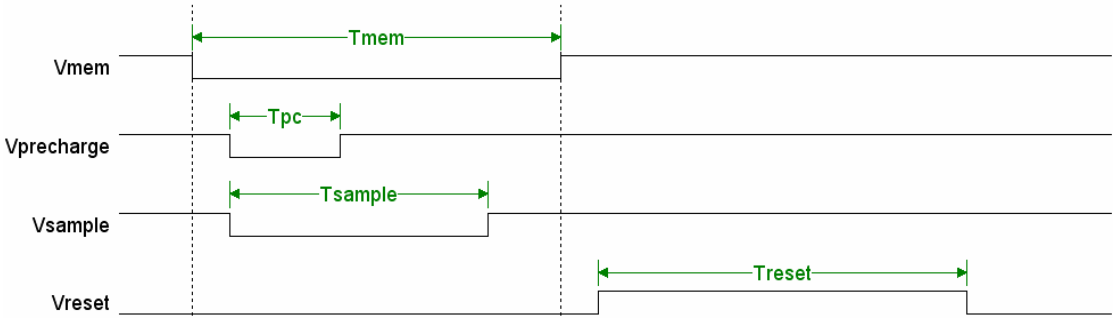


Figure 11. Internal Timing of Pixel

In Figure 11, levels are defined by the pixel array voltage supplies; for correct polarities of the signals see Table 4. The signals in Figure 11 are generated from the on-chip drivers. These on-chip drivers need two types of signals to generate the exact type of signal. It needs digital control signals between 0 V and 3.3 V (internally converted to 2.5 V) with normal driving capability and power supplies. The control signals are required to indicate when they must occur and the power supplies indicate the level.

Vmem is made of a control signal Mem_hl and 2 supplies Vmem_h and Vmem_l. If the signal Mem_hl is the logic '0' than the internal signal Vmem is low, if Mem_hl is logic '1' the internal signal Vmem is high.

Reset is made with two control signals, Reset and Reset_ds, and two supplies, Vres and Vres_ds. Depending on the signal that becomes active, the corresponding supply level is applied to the pixel.

Table 4 summarizes the relation between the internal and external pixel array signals.

Table 4. OVERVIEW OF INTERNAL AND EXTERNAL PIXEL ARRAY SIGNALS

Internal Signal	Vlow	Vhigh	External Control Signal	Low DC Level	High DC Level
Precharge	0	0.45 V	Precharge (AL)	Vpre_l	Controlled by bias-resistor
Sample	0	2.5 V	Sample (AL)	Gnd	Vdd
Reset	0	2.5 V to 3.3 V	Reset (AH) and Reset_ds (AH)	Gnd	Vres and Vres_ds
Vmem	2.0 V to 2.5 V	2.5 V to 3.3 V	Mem_hl (AL)	Vmem_l	Vmem_h

For dual slope operation, give a second reset pulse to a lower reset level during integration. This is done by the control signal Reset_ds and by the power supply Vres_ds that defines the level to which the pixel must be reset.

Note that Reset is dominant over Reset_ds, which means that the high voltage level is applied for reset, if both pulses occur at the same time.

Multiple slopes are possible having multiple Reset_ds pulses with a lower Vres_ds level for each pulse given within the same integration time.

The rise and fall times of the internal generated signals are not very fast (200 ns). In fact they are made rather slow to limit the maximum current through the power supply lines (Vmem_h, Vmem_l, Vres, Vres_ds, Vdd). Current limitation of those power supplies is not required. However, limit the currents to not higher than 400 mA.

The power supply Vmem_l must be able to sink this current because it must be able to discharge the internal capacitance from the level Vmem_h to the level Vmem_l. The external control signals should be capable of driving input capacitance of about 10 pF.

Digital Signals

The digital signals control the readout of the image sensor. These signals are:

- Sync_y (AH[10]): Starts the readout of the frame. This pulse synchronises the y-address register: active high. This signal is also the end of the frame or window and determines the window width.
- Clock_y (AH[10]): Clock of the y-register. On the rising edge of this clock, the next line is selected.
- Sync_x (AH[10]): Starts the readout of the selected line at the address defined by the x-address register. This pulse synchronises the x-address register: active high. This signal is also the end of the line and determines the window length.
- Clock_x (AH[10]): Determines the pixel rate. A clock of 33 MHz is required to achieve a pixel rate of 66 MHz.
- Spi_data (AH[10]): Data for the SPI.
- Spi_clock (AH[10]): Clock of the SPI. This clock downloads the data into the SPI register.

- Spi_load (AH[10]): When the SPI register is uploaded, then the data is internally available on the rising edge of SPI_load.
- Sh_kol (AL[11]): Control signal of the column readout. It is used in sample and hold mode and binning mode.
- Norowsel (AH[10]): Control signal of the column readout (see Timing and Readout of Image Sensor).
- Pre_col (AL[11]): Control signal of the column readout to reduce row blanking time.
- Voltage averaging (AH[10]): Signal required obtaining voltage averaging of two pixels.

NOTES: 10. AH: Active High
11. AL: Active Low

Test Signals

The test structures implemented in this image sensor are:

- Array of pixels (6 x 12) that outputs are tied together: used for spectral response measurement.
- Temperature diode (2): Apply a forward current of 10 μA to 100 μA and measure the voltage V_T of the diode. V_T varies linear with the temperature (V_T decreases with approximately 1.6 mV/°C).
- End of scan pulses (do not use to trigger other signals):
  - Eos_x: end of scan signal: is an output signal, indicating when the end of line is reached. It is not generated when windowing.
  - Eos_y: end of scan signal: is an output signal, indicating when the end of frame is reached. It is not generated when windowing.
  - Eos_spi: output signal of the SPI to check if the data is transferred correctly through the SPI.

Frame Rate and Windowing

Frame Rate

To acquire a frame rate of 15 frames/sec, the output amplifier should run at 66 MHz pixel rate or two output amplifiers should run at 33 MHz each, assuming an ROT of 200 ns.

The frame period of the LUPA4000 sensor is calculated as follows:

Frame period = FOT + (Nr. Lines x (ROT + pixel period x Nr. Pixels) with:

FOT = 5 μs

Nr. Lines: Number of Lines read out each frame (Y)

Nr. Pixels: Number of pixels read out each line (X)

ROT = 200 ns (nominal; can be further reduced)

Pixel period: 1/66 MHz = 15.15 ns

Example read out of the full resolution at nominal speed (66 MHz pixel rate):

Frame period = 5 μs + (2048 x (200 ns + 15.15 ns x 2048) = 64 ms ≥ 15 fps.

ROI Readout (Windowing)

Windowing is achieved by an SPI in which the starting point of the x-address and y-address is uploaded. This downloaded starting point initiates the shift register in the x-direction and y-direction triggered by the Sync_x and Sync_y pulse. The minimum step size for the x-address and the y-address is 2 (only even start addresses can be chosen). The size of both address registers is 10-bits. For instance, when the addresses 0000000001 and 0000000001 are uploaded, the readout starts at line 2 and column 2.

Table 5. FRAME RATE AS FUNCTION OF ROI READ OUT AND SUB SAMPLING

Image Resolution (X*Y)	Frame Rate [frames f/S]	Frame Readout Time [mS]	Comment
2048 x 2048	15	67	Full resolution.
1024 x 2048	31	32	Subsample in X-direction.
1024 x 1024	62	16	ROI read out.
640 x 480	210	4.7	ROI read out.

TIMING AND READOUT OF IMAGE SENSOR

The timing of the LUPA4000 sensor consists of two parts. The first part is related to the control of the pixels, the integration time, and the signal level. The second part is related to the readout of the image sensor. As full synchronous shutter is possible with this image sensor, integration time and readout can be in parallel or sequential.

In the parallel mode, the integration time of the frame I is ongoing during readout of frame I-1. Figure 12 shows this parallel timing structure.

The control of the frame's readout and integration time are independent of each other with the only exception that the end of the integration time from frame I+1 is the beginning of the readout of frame I+1.

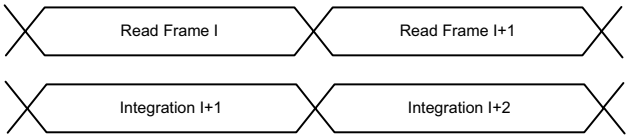


Figure 12. Integration and Readout in Parallel

The LUPA4000 sensor is also used in sequential mode (triggered snapshot mode) where readout and integration is sequential. Figure 13 shows this sequential timing.

Figure 13. Integration and Readout in Sequence

Timing of Pixel Array

The first part of the timing is related to the timing of the pixel array. This implies control of integration time, synchronous shutter operation, and sampling of the pixel information onto the memory element inside each pixel. The signals required for this control are described in Pixel Array Signals and in Figure 11.

Figure 14 shows the external applied signals required to control the pixel array. At the end of the integration time from frame I+1, the signals Mem_hl, precharge, and sample must be given. The reset signal controls the integration time, which is defined as the time between the falling edge of reset and the rising edge of sample.

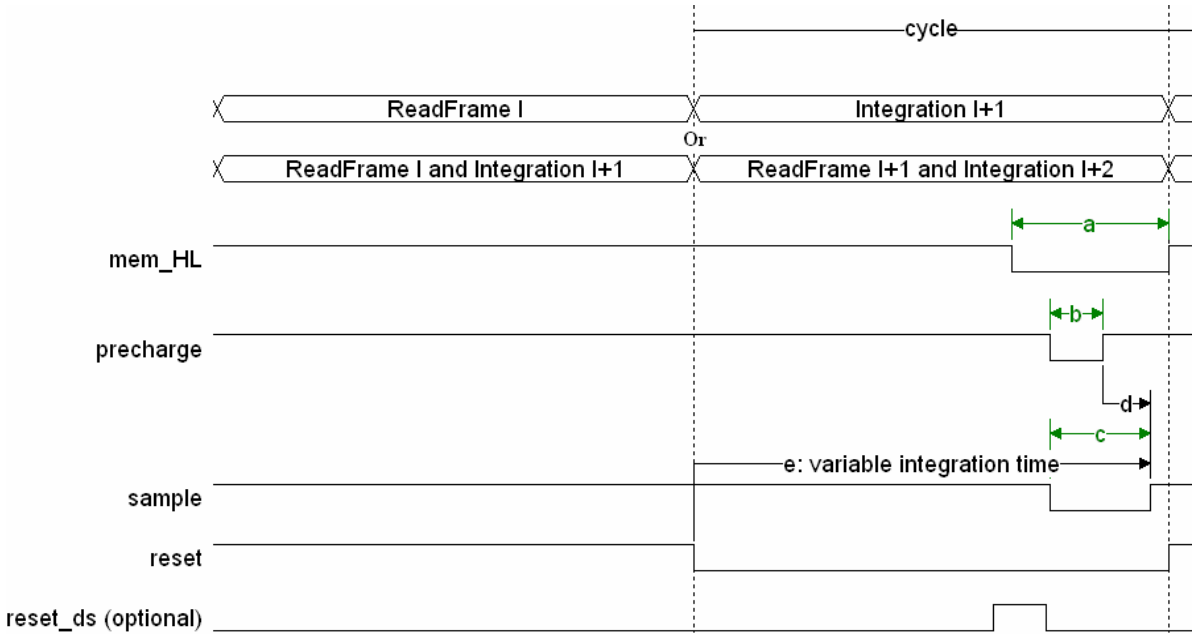


Figure 14. Pixel Array Timing

The integration time is determined by the falling edge of the reset pulse. The longer the pulse is high, the shorter the integration time. At the end of the integration time, the information must be stored onto the memory element for readout.

Timing specifications for each signal are shown in Table 6.

- Falling edge of precharge is equal or later than falling edge of Vmem.
- Sample is overlapping with precharge.
- Rising edge of Vmem is more than 200 ns after rising edge of sample.
- Rising edge of reset is equal or later than rising edge of Vmem.

Table 6. TIMING SPECIFICATIONS

Symbol	Name	Value
a	Mem_HL	5 – 8.2 μs
b	Precharge	3 – 6 μs
c	Sample	5 – 8 μs
d	Precharge−Sample	> 2 μs
e	Integration time	> 1 μs

The timing of the pixel array is straightforward. Before the frame is read, the information on the photodiode must be stored onto the memory element inside the pixels. This is done with the signals Mem_hl, precharge, and sample. When precharge is activated, it serves as a load for the first source follower in the pixel. Sample stores the photodiode information onto the memory element. Mem_hl pumps up this value to reduce the loss of signal in the pixel and this signal must be the envelop of precharge and sample. After Mem_hl is high again, the readout of the pixel array starts. The frame blanking time or frame overhead time is thus the time that Mem_hl is low, which is about 5 μs. After the readout starts, the photodiodes can all be initialised by reset for the next integration time. The minimal integration time is the minimal time between the falling edge of reset and the rising edge of sample. Keeping the slow fall times of the corresponding internal generated signals in mind, the minimal integration time is about 2 μs.

An additional reset pulse of minimum 2 μs can be given during integration by asserting Reset_ds to implement the double slope integration mode.

Readout of Image Sensor

When the pixel information is stored in the memory element of each pixel, it can be read out sequentially. Integration and readout can also be done in parallel.

The readout timing is straightforward and is controlled by sync and clock pulses.

Figure 15 shows the top level concept of this timing. The readout of a frame consists of the frame overhead time, the selection of the lines sequentially, and the readout of the pixels of the selected line.

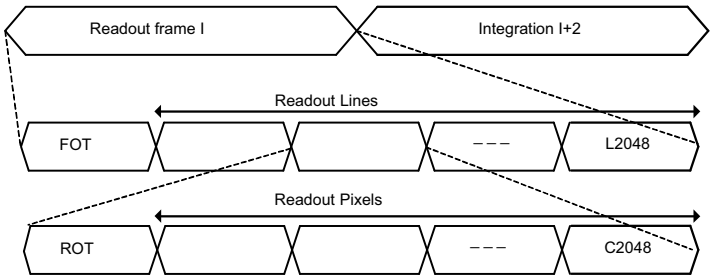


Figure 15. Readout of Image Sensor (L: line selection, C: column selection)

The readout of an image consists of the FOT and the sequential selection of all pixels. The FOT is the overhead time between two frames to transfer the information on the photodiode to the memory elements. Figure 14 shows that at this time Mem_hl is low (typically 5 ms). After the FOT, the information is stored into the memory elements and a sequential selection of rows and columns makes sure the frame is read.

X and Y Addressing

To read out a frame, the lines are selected sequentially. Figure 16 gives the timing to select the lines sequentially. This is done with a Clock_y and Sync_y signal. The Sync_y signals synchronizes the y-addressing and initializes the y-address selection registers. The start address is the address downloaded in the SPI multiplied by two.

On the rising edge of Clock_y the next line is selected. The Sync_y signal is dominant and from the moment it occurs, the y-address registers are initialized. If a Sync_y pulse is given before the end of the frame is reached, only a part of the frame is read. To obtain a correct initialization, Sync_y must contain at least one rising edge of Clock_y when it is active.

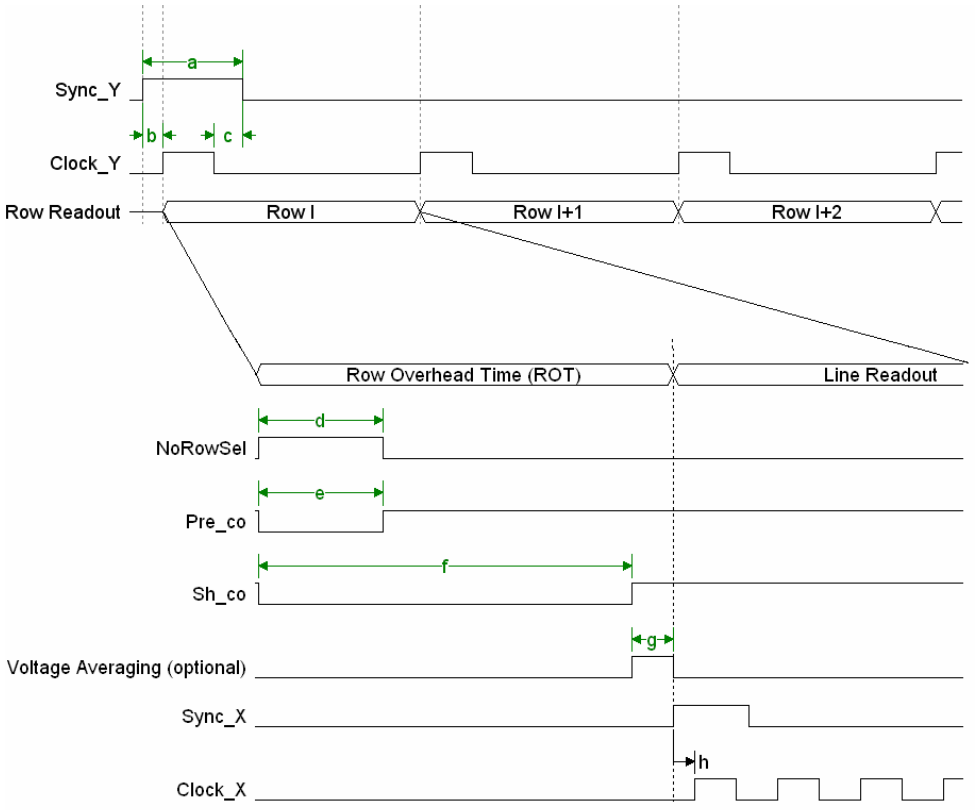


Figure 16. X and Y Addressing

Table 7. READOUT TIMING SPECIFICATIONS

Symbol	Name	Value
a	Sync_Y	> 20 ns
b	Sync_Y−Clock_Y	> 0 ns
c	Clock_Y−Sync_Y	> 0 ns
d	NoRowSel	> 50 ns
e	Pre_col	> 50 ns
f	Sh_col	200 ns
g	Voltage averaging	> 20 ns
h	Sync_X−Clock_X	> 0 ns

As soon as a new line is selected, it must be read out by the output amplifiers. Before the pixels of the selected line can be multiplexed onto the output amplifiers, wait for a certain time, indicated as the ROT shown in Figure 16. This is the time to get the data stable from the pixels to the output bus before the output stages. This ROT is in fact lost time and rather critical in a high-speed sensor. Different timings to reduce this ROT are explained later in this section.

During the selection of one line, 2048 pixels are selected. These 2048 pixels must be read out by one (or two) output amplifier.

The pixel rate is the double frequency of the Clock_x frequency. To obtain a pixel rate of 66 MHz, apply a pixel clock Clock_x of 33MHz. When only one analog output is used, two pixels are output every Clock_x period. When Clock_x is high, the first pixel is selected; when Clock_x is low, the next pixel is selected. Consequently, during one complete period of Clock_x two pixels are read out by the output amplifier.

If two analog outputs are used each Clock-X period one pixel is presented at each output.

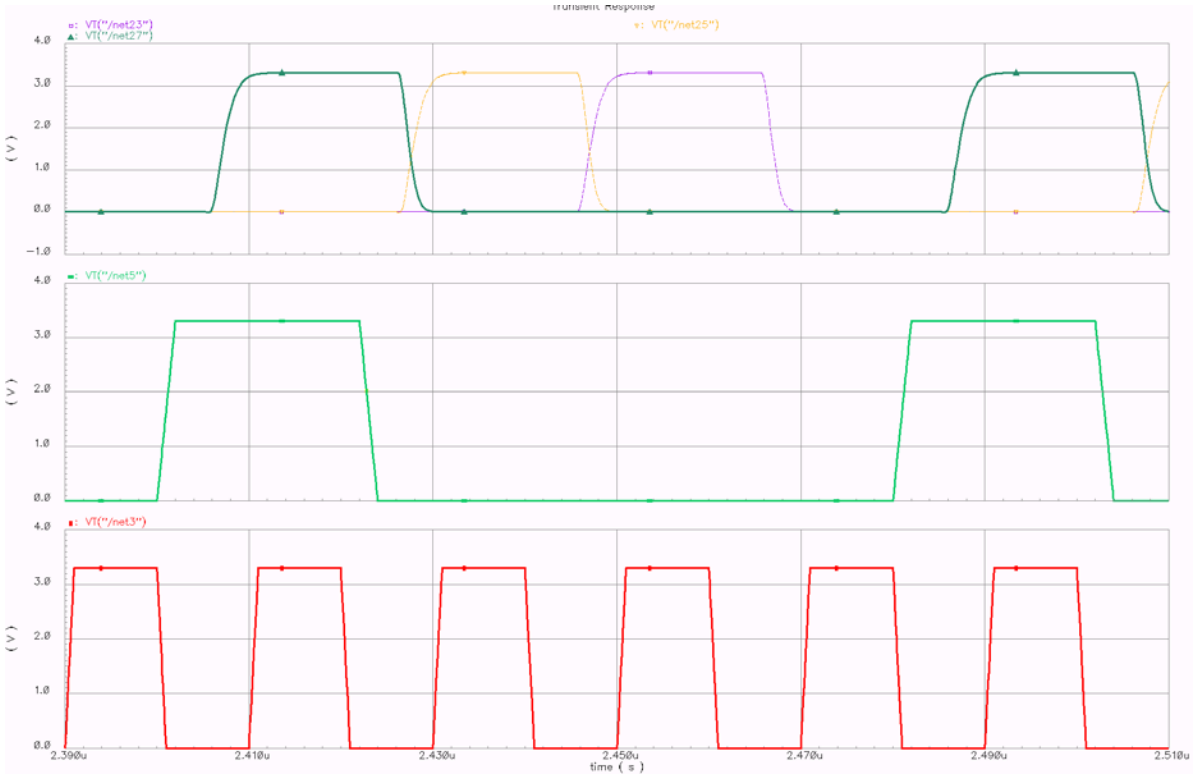


Figure 17. X−Addressing

The figure shows Clock_x, Sync_x, internal selection pixel 1 and 2, internal selection pixel 3 and 4, internal selection pixel 5 and 6. The first pixel selected is the x-address downloaded in the SPI. The starting address is the number downloaded into the SPI, multiplied by 2.

Windowing is achieved by a starting address downloaded in the SPI and the size of the window. In the x-direction, the size is determined by the moment a new Clock_y is given. In the y-direction, the sync_y pulse determines the size. The best way to obtain a window is by using an internal counter in the controller.

Figure 17 is the simulation result after extraction of the layout module from a different sensor to show the principle. In this figure, the pixel clock has a frequency of 50 MHz, which results in a pixel rate of 100 Msamples/sec.

Figure 18 on page 17 shows the relation between the applied Clock_x and the output signal.

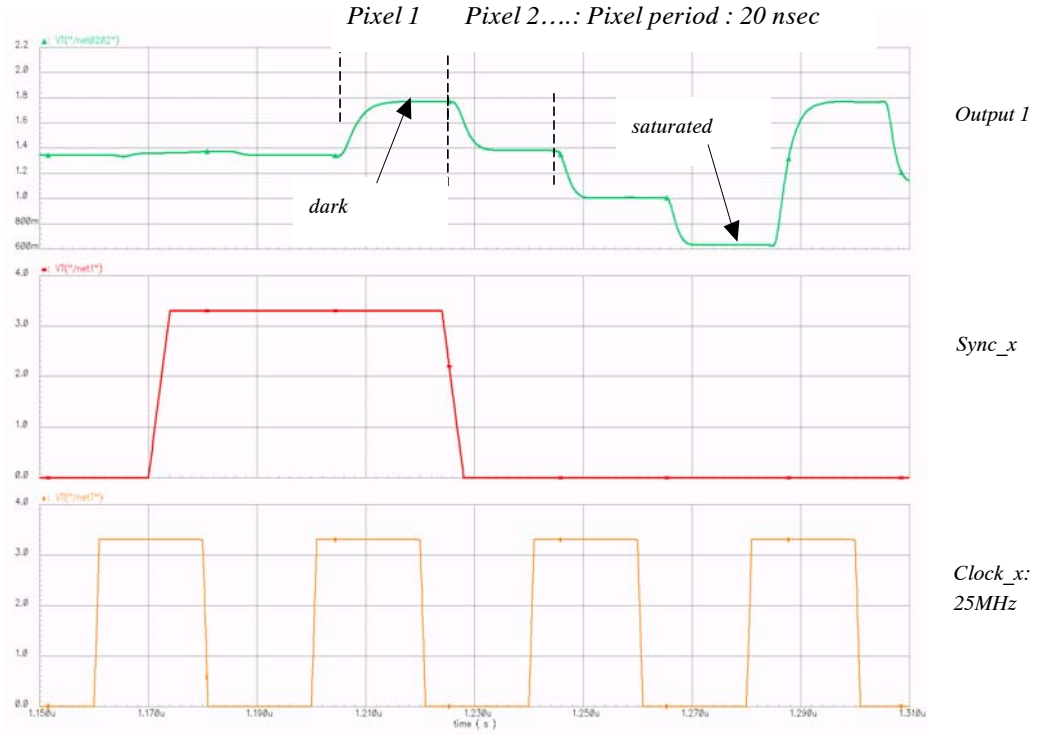


Figure 18. Output Signal Related to Clock_x Signal

In the figure, shown from bottom to top: Clock_x, Sync_x and output. Output level before the first pixel is the level of the last pixel on previous line.

As soon as Sync_x is high and one rising edge of Clock_x occurs, the pixels are brought to the analog outputs. This is again the simulation result of a comparable sensor to show the principle.

Note the time difference between the clock edge and the moment the data is seen at the output. Because it is difficult to predict this time difference in advance, have the ADC sampling clock flexible to set an optimal ‘add sampling’ point. The time differences can easily vary between 5 ns and 15 ns and must be tested on the real devices.

Reduced ROT Timing

The ROT is the time between the selection of lines that you must wait to get the data stable at the column amplifiers. It is a loss in time, which should be reduced as much as possible.

Standard Timing (200 ns)

In this case, the control signals Norowsel and pre_col are made active for about 20 ns from the moment the next line is selected. The time these pulses must be active is related to the biasing resistance Pre_load. The lower this resistance, the shorter the pulse duration of Norowsel and pre_col may be. After these pulses are given, wait for at least 180 ns before the first pixel is sampled. For this mode, Sh_col must always be active (low).

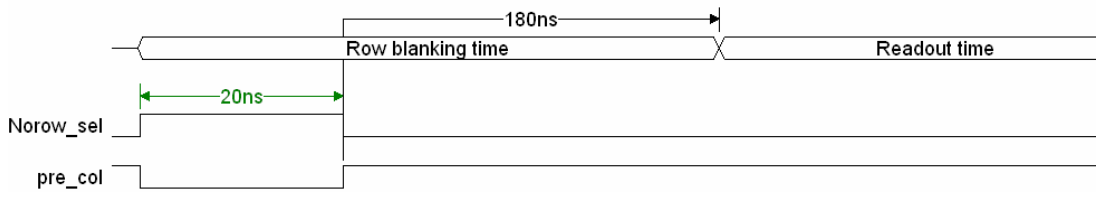


Figure 19. Standard Timing for ROT (only pre_col and No_row_sel control signals are required)

In this case, the control signals Norowsel and pre_col are made active for about 20 ns from the moment the next line is selected. The time these pulses must be active is related to the biasing resistance Pre_load. The lower this resistance, the shorter the pulse duration of Norowsel and pre_col may be. After these pulses are given, wait for at least 180 ns before the first pixel is sampled. For this mode Sh_col must be made active (low) all the time.

Backup Timing (ROT = 100 to 200 ns)

Use a sample and hold function to reduce the ROT.

Track the analog data using Sh_col during the first 100 ns during the selection of a new set of lines. After 100 ns, the analog data is stored. The ROT is reduced to 100 ns, but as the internal data is not stable yet, dynamic range is lost. This is because the complete analog levels are not reached after 100 ns.

Figure 20 shows this principle. Sh_col is now a pulse of 100 ns to 200 ns starting at the same time as pre_col and Norowsel. The duration of Sh_col is equal to the ROT. The shorter this time the shorter the ROT; however, this also lowers the dynamic range.

If voltage-averaging is required, the sensor must work in this mode with Sh_col signal and a voltage-averaging signal must be generated after Sh_col drops and before the readout starts (see Figure 16 on page 15).

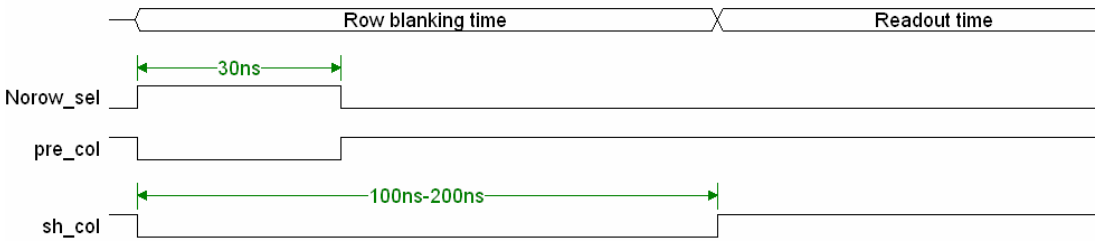


Figure 20. Reduced Standard ROT with Sh_col Signal
pre_col (short pulse), Norowsel (short pulse) and Sh_col (large pulse)

Precharging the Buses

This timing mode is similar to the mode without sample and hold, except that the prebus1 and prebus2 signals are activated. Note that precharging of the buses can be combined with all the timing modes discussed earlier. The idea is to have a short pulse of about 5 ns to precharge the output buses to a known level. This mode makes the ghosting of bad columns impossible. In this mode, Nsf_load must be made much larger (at least 1 MΩ).

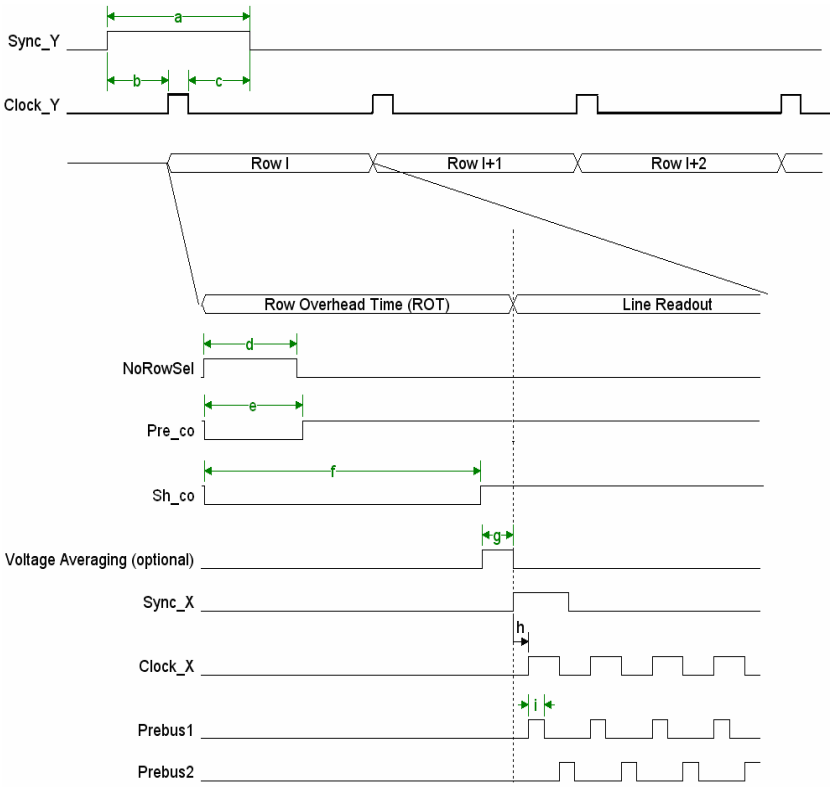


Figure 21. X and Y Addressing with Precharging of Buses

Table 8. READOUT TIMING SPECIFICATIONS WITH PRECHARGING OF BUSES

Symbol	Name	Value
a	Sync_Y	> 20 ns
b	Sync_Y-Clock_Y	> 0 ns
c	Clock_Y-Sync_Y	> 0 ns
d	NoRowSel	> 50 ns
e	Pre_col	> 50 ns
f	Sh_col	200 ns (or cst low, depending on timing mode)
g	Voltage averaging	> 20 ns
h	Sync_X-Clock_X	> 0 ns
i	Prebus pulse	As short as possible

Serial Peripheral Interface

The SPI is required to upload different modes. Table 9 shows the parameters and their bit position.

Table 9. SPI PARAMETERS

Parameter	Bit #	Remarks
Y-direction	0	1: From bottom to top
Y-address	1 to 10	Bit 1 is LSB
X-voltage averaging enable	11	1: Enabled
X-subsampling	12	1: Subsampling
X-direction	13	0: From left to right
X-address	14 to 23	Bit 14 is LSB
Number of output amplifiers	24	0: 1 Output
DAC	25 to 31	Bit 25 is LSB

When all zeros are loaded into the SPI, the sensor starts at pixel 0,0. The scanning is from left to right and from top to bottom. There is no sub sampling or voltage averaging and only one output is used. The DAC has the lowest level at its output. When using sub sampling, only even X-addresses should be applied.

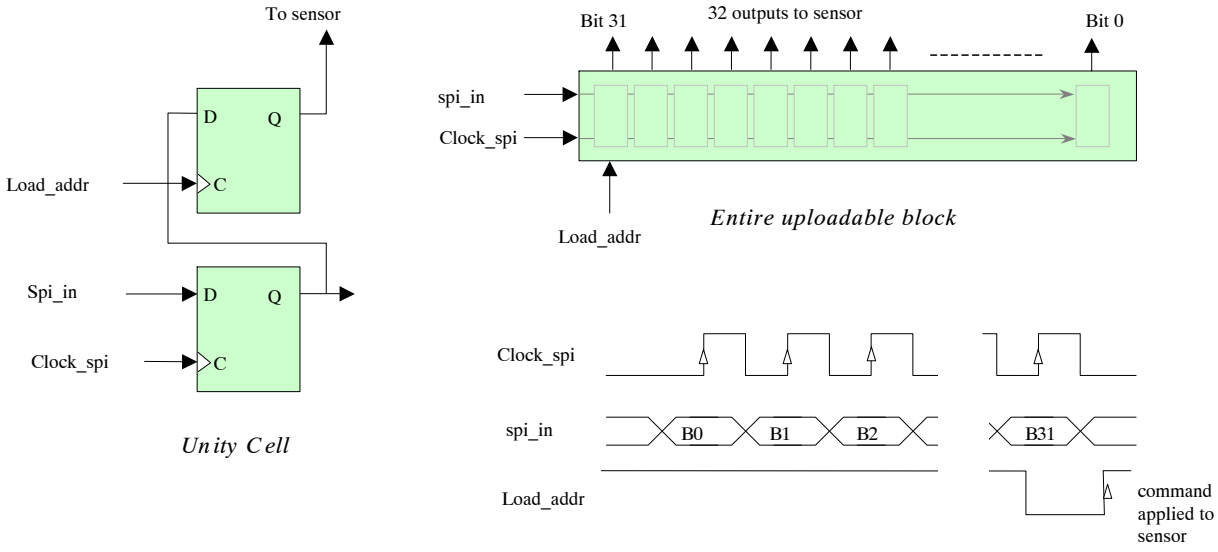


Figure 22. SPI Block Diagram and Timing

PIN LIST

Table 10 lists the pins and their functionalities.

Table 10. PIN LIST (Notes 1, 2 and 3)

Pad	Pin	Pin Name	Pin Type	Description
1	E1	sync_x	Input	Digital input. Synchronises the X-address register.
2	F1	eos_x	Testpin	Indicates when the end of the line is reached.
3	D2	vdd	Supply	Power supply digital modules.
4	G2	clock_x	Input	Digital input. Determines the pixel rate.
5	G1	eos_spi	Testpin	Checks if the data is transferred correctly through the SPI.
6	F2	spi_data	Input	Digital input. Data for the SPI.
7	H1	spi_load	Input	Digital input. Loads data into the SPI.
8	H2	spi_clock	Input	Digital input. Clock for the SPI.
9	J2	gndo	Ground	Ground output stages
10	J1	out2	Output	Analog output 2.
11	K1	out2DC	Output	Reference output 2.
12	M2	voo	Supply	Power supply output stages
13	L1	out1DC	Output	Reference output 1.
14	M1	out1	Output	Analog output 1.
15	N2	gndo	Ground	Ground output stages.
16	P1	vaa	Supply	Power supply analog modules.
17	P2	gnda	Ground	Ground analog modules.
18	N1	va3	Supply	Power supply column modules.
19	P3	vpix	Supply	Power supply pixel array.
20	Q1	psf_load	Input	Analog reference input. Biasing for column modules. Connect with R = 1 MΩ to Vaa and decouple with C = 100 nF to gnda.
21	Q2	nsf_load	Input	Analog reference input. Biasing for column modules. Connect with R = 5 kΩ to Vaa and decouple with C = 100 nF to gnda.
22	R1	muxbus_load	Input	Analog reference input. Biasing for multiplex bus. Connect with R = 25 kΩ to Vaa and decouple with C = 100 nF to gnda.
23	R2	uni_load_fast	Input	Analog reference input. Biasing for column modules. Connect with R = 10 kΩ to Vaa and decouple with C = 100 nF to gnda.
24	Q3	pre_load	Input	Analog reference input. Biasing for column modules. Connect with R = 3 kΩ to Vaa and decouple with C = 100 nF to gnda.
25	Q4	out_load	Input	Analog reference input. Biasing for output stage. Connect with R = 60 kΩ to Vaa and decouple with C = 100 nF to gnda.
26	N3	dec_x_load	Input	Analog reference input. Biasing for X-addressing. Connect with R = 2 MΩ to Vdd and decouple with C = 100 nF to gndd.
27	Q5	uni_load	Input	Analog reference input. Biasing for column modules. Connect with R = 1 MΩ to Vaa and decouple with C = 100 nF to gnda.
28	Q6	col_load	Input	Analog reference input. Biasing for column modules. Connect with R = 1 MΩ to Vaa and decouple with C = 100 nF to gnda.
29	Q7	dec_y_load	Input	Analog reference input. Biasing for Y-addressing. Connect with R = 2 MΩ to Vdd and decouple with C = 100 nF to gndd.
30	R3	vdd	Supply	Power supply digital modules.
31	M3	gndd	Ground	Ground digital modules.
32	L2	prebus1	Input	Digital input. Control signal to reduce readout time.
33	L3	prebus2	Input	Digital input. Control signal to reduce readout time.

Table 10. PIN LIST (Notes 1, 2 and 3)

Pad	Pin	Pin Name	Pin Type	Description
34	Q8	sh_col	Input	Digital input. Control signal of the column readout.
35	R4	pre_col	Input	Digital input. Control signal of the column readout to reduce row-blanking time.
36	R5	norowsel	Input	Digital input. Control signal of the column readout.
37	R6	clock_y	Input	Digital input. Clock of the Y-addressing.
38	R7	sync_y	Input	Digital input. Synchronizes the Y-address register.
39	K2	eos_y_r	Testpin	Indicates when the end of frame is reached when scanning in the 'right' direction.
40	Q9	temp_diode_p	Testpin	Anode of temperature diode.
41	Q10	temp_diode_n	Testpin	Cathode of temperature diode.
42	R8	vpix	Supply	Power supply pixel array.
43	R9	vmem_l	Supply	Power supply Vmem drivers.
44	R10	vmem_h	Supply	Power supply Vmem drivers.
45	R11	vres	Supply	Power supply reset drivers.
46	Q11	vres_ds	Supply	Power supply reset drivers.
47	R12	adc1_ref_low	Input	Analog reference input. Low reference voltage of ADC (see Figure 7 on page 8 for exact resistor value.)
48	Q12	adc1_linear_conv	Input	Digital input. 1= linear conversion; 0= gamma correction.
49	P15	adc1_bit_9	Output	Digital output 1 <9> (MSB).
50	Q14	adc1_bit_8	Output	Digital output 1 <8>.
51	Q15	adc1_bit_7	Output	Digital output 1 <7>.
52	R13	adc1_bit_6	Output	Digital output 1 <6>.
53	R14	adc1_bit_5	Output	Digital output 1 <5>.
54	R15	adc1_bit_4	Output	Digital output 1 <4>.
55	P14	adc1_bit_3	Output	Digital output 1 <3>.
56	Q13	adc1_bit_2	Output	Digital output 1 <2>.
57	R16	adc1_bit_1	Output	Digital output 1 <1>.
58	Q16	adc1_bit_0	Output	Digital output 1 <0> (LSB).
59	P16	adc1_clock	Input	ADC clock input.
60	N14	adc1_gndd	Supply	Digital GND of ADC circuitry.
61	N15	adc1_vddd	Supply	Digital supply of ADC circuitry (nominal 2.5 V).
62	L16	adc1_gnda	Supply	Analog GND of ADC circuitry.
63	L15	adc1_vdda	Supply	Analog supply of ADC circuitry (nominal 2.5 V).
64	N16	adc1_bit_inv	Input	Digital input. 0 = no inversion of output bits; 1 = inversion of output bits.
65	M16	adc1_CMD_SS	Input	Analog reference input. Biasing of second stage of ADC. Connect to V_{DDA} with R = 50 kΩ and decouple with C = 100 nF to gnda.
66	L14	adc1_nalog_in	Input	Analog input of first ADC.
67	M15	adc1_CMD_FS	Input	Analog reference input. Biasing of first stage of ADC. Connect to V_{DDA} with R = 50 kΩ and decouple with C = 100 nF to gnda.
68	M14	adc1_ref_high	Input	Analog reference input. High reference voltage of ADC. See Figure 7 on page 8 for exact resistor value.
69	K14	vres_ds	Supply	Power supply reset drivers.
70	J14	vres	Supply	Power supply reset drivers.

Table 10. PIN LIST (Notes 1, 2 and 3)

Pad	Pin	Pin Name	Pin Type	Description
71	J15	vpre_l	Supply	Power supply precharge drivers. Must be able to sink current. Can also be connected to ground.
72	J16	vdd	Supply	Power supply digital modules.
73	K15	vmem_h	Supply	Power supply Vmem drivers.
74	K16	vmem_l	Supply	Power supply Vmem drivers.
75	H15	adc2_ref_low	Input	Analog reference input. Low reference voltage of ADC. See Figure 7 on page 8 for exact resistor value.
76	H16	adc2_linear_conv	Input	Digital input. 1= linear conversion; 0= gamma correction.
77	G16	adc2_bit_9	Output	Digital output 2 <9> (MSB).
78	F16	adc2_bit_8	Output	Digital output 2 <8>.
79	E16	adc2_bit_7	Output	Digital output 2 <7>.
80	G15	adc2_bit_6	Output	Digital output 2 <6>.
81	G14	adc2_bit_5	Output	Digital output 2 <5>.
82	F14	adc2_bit_4	Output	Digital output 2 <4>.
83	E14	adc2_bit_3	Output	Digital output 2 <3>.
84	D16	adc2_bit_2	Output	Digital output 2 <2>.
85	E15	adc2_bit_1	Output	Digital output 2 <1>.
86	F15	adc2_bit_0	Output	Digital output 2 <0> (LSB).
87	D15	adc2_clock	Input	ADC clock input.
88	C15	adc2_gndd	Supply	Digital GND of ADC circuitry.
89	D14	adc2_vddd	Supply	Digital supply of ADC circuitry (nominal 2.5 V).
90	B16	adc2_gnda	Supply	Analog GND of ADC circuitry.
91	B14	adc2_vdda	Supply	Analog supply of ADC circuitry (nominal 2.5 V).
92	C16	adc2_bit_inv	Input	Digital input. 0 = no inversion of output bits; 1 = inversion of output bits.
93	A16	adc2_CMD_SS	Input	Biasing of second stage of ADC. Connect to V_{DDA} with R = 50 kΩ and decouple with C = 100 nF to gnda.
94	B15	adc2_analog_in	Input	Analog input second ADC.
95	A15	adc2_adc2_CMD_FS	Input	Analog reference input. Biasing of first stage of ADC. Connect to V_{DDA} with R = 50 kΩ and decouple with C = 100 nF to gnda.
96	A14	adc2_ref_high	Input	Analog reference input. High reference voltage of ADC. See Figure 7 on page 8 for exact resistor value.
97	C14	vres_ds	Supply	Power supply reset drivers.
98	B13	vres	Supply	Power supply reset drivers.
99	A13	vmem_h	Supply	Power supply Vmem drivers.
100	A9	vmem_l	Supply	Power supply Vmem drivers.
101	A10	vpix	Supply	Power supply pixel array.
102	A11	reset	Input	Digital input. Control of reset signal in the pixel.
103	A12	reset_ds	Input	Digital input. Control of double slope reset in the pixel.
104	B7	mem_hl	Input	Digital input. Control of Vmem signal in pixel.
105	B8	precharge	Input	Digital input. Control of Vprecharge signal in pixel.
106	B9	sample	Input	Digital input. Control of Vsample signal in pixel.
107	B10	temp_diode_n	Testpin	Cathode of temperature diode.
108	B11	temp_diode_p	Testpin	Anode of temperature diode.

Table 10. PIN LIST (Notes 1, 2 and 3)

Pad	Pin	Pin Name	Pin Type	Description
109	B6	precharge_bias	Input	Analog reference input. Biasing for pixel array. See Table 3 on page 10 for exact resistor and capacitor value.
110	A8	photodiode	Testpin	Output photodiode.
111	A7	gndd	Ground	Ground digital modules.
112	B12	vdd	Supply	Power supply digital modules.
113	A6	eos_y_l	Testpin	Indicates when the end of frame is reached when scanning in the 'left' direction.
114	A1	sync_y	Input	Digital input. Synchronizes the Y-address register.
115	A5	clock_y	Input	Digital input. Clock of the Y-addressing.
116	A2	norowsel	Input	Digital input. Control signal of the column readout.
117	A3	volt. averaging	Input	Digital input. Control signal of the voltage averaging in the column readout.
118	B5	pre_col	Input	Digital input. Control signal of the column readout to reduce row-blanking time.
119	A4	sh_col	Input	Digital input. Control signal of the column readout.
120	B1	prebus2	Input	Digital input. Control signal to reduce readout time.
121	B2	prebus1	Input	Digital input. Control signal to reduce readout time.
122	C1	dec_y_load	Input	Analog reference input. Biasing for Y-addressing.
123	D1	vpix	Supply	Power supply pixel array.
124	B4	va3	Supply	Power supply column modules.
125	B3	gnda	Ground	Ground analog modules.
126	C2	vaa	Supply	Power supply analog modules.
127	E2	gndd	Ground	Ground digital modules.

1. All pins with the same name can be connected together.
2. All digital input are active high (unless mentioned otherwise).
3. All unused inputs should be tied to a non active level (For example, V_{DD} or GND).

Package Drawing

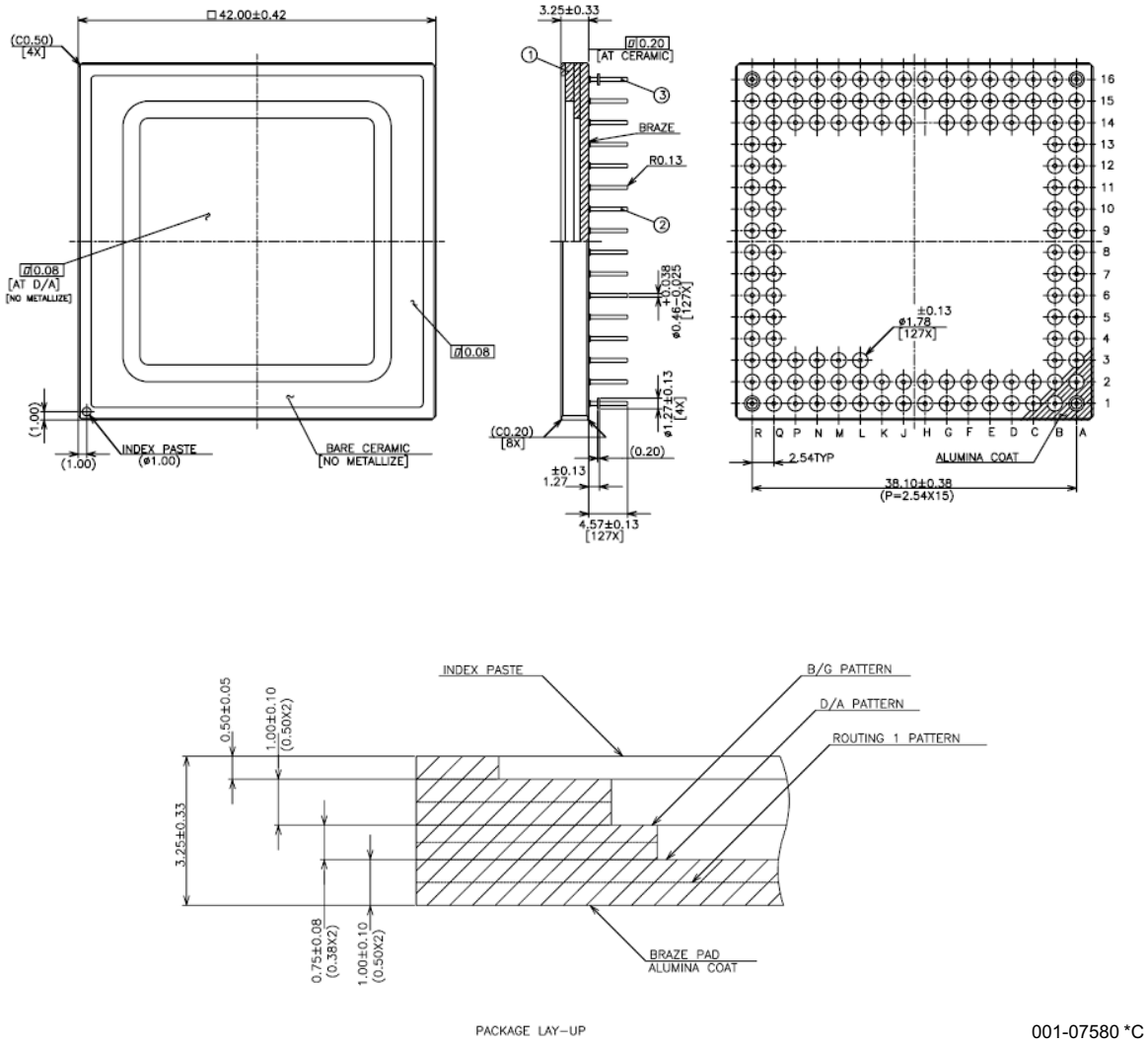


Figure 23. LUPA4000: 127 Pin PGA Package Drawing

Mechanical Package Specification

Mechanical Specifications		Min	Typ	Max	Units
Package (Pin 1 bottom left)	Cavity Size		27000 x 29007		μm
Die (with Pin 1 to the bottom left, Top View)	Die size		25610 x 27200		μm
	Die center, X offset to the center of package	(−50)	0	(+50)	μm
	Die center, Y offset to the center of package	(−50)	0	(+50)	μm
	Die position, X tilt	1		1	deg
	Die position, Y tilt	1		1	deg
	Die placement accuracy in package	(−50)		(+50)	μm
	Die rotation accuracy	−1		1	deg
	Optical center referenced from package center (X−dir)	(−50)	15	(+50)	μm
	Optical center referenced from package center (Y−dir)	(−50)	−80	(+50)	μm
Glass Lid	Glass window size	(−10%)	38.5 x 38.5	(+10%)	mm
	Glass window thickness		0.7		mm
	Spectral range for window	400		1000	nm
	Transmission of the glass window			92	%
Mechanical shock	JESD22−B104C; Condition G			2000	G
Vibration	JESD22−B103B; Condition 1	20		2000	Hz
Mounting Profile	Pb−free wave soldering profile for pin grid array package				
Recommended socket	Andon Electronics (www.andonelectronics.com)	575−16−24−127−01S−R29−L14			

Glass Lid

The LUPA4000 image sensor uses a glass lid without any coatings. Figure 24 shows the transmission characteristics of the glass lid.

As seen in Figure 24, the sensor does not use infrared attenuating color filter glass. You must provide a filter in the optical path when using color devices.

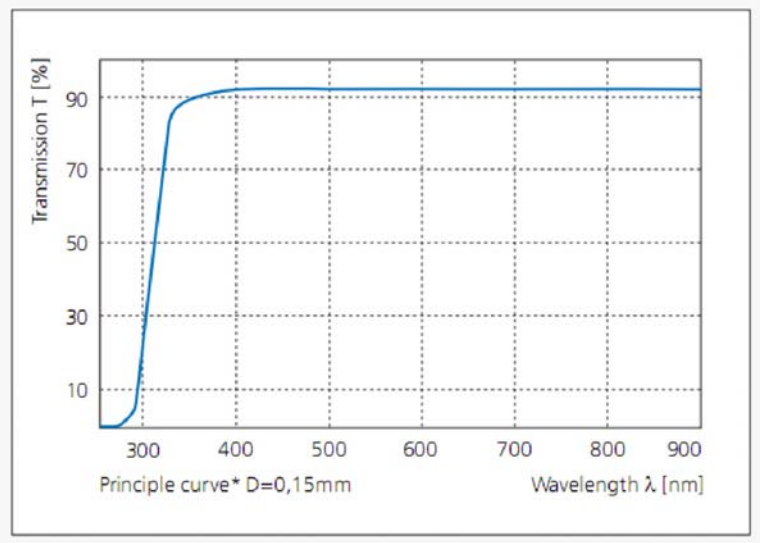


Figure 24. Transmission Characteristics of Glass Lid

HANDLING PRECAUTIONS

For proper handling and storage conditions, refer to the ON Semiconductor application note AN52561.

LIMITED WARRANTY

ON Semiconductor's Image Sensor Business Unit warrants that the image sensor products to be delivered hereunder, if properly used and serviced, will conform to Seller's published specifications and will be free from defects in material and workmanship for two (2) years following the date of shipment. If a defect were to manifest itself within 2 (two) years period from the sale date, ON Semiconductor will either replace the product or give credit for the product.

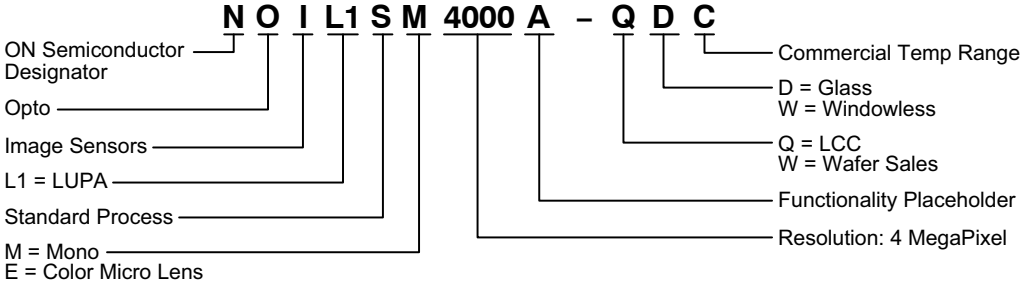
Return Material Authorization (RMA)

ON Semiconductor packages all of its image sensor products in a clean room environment under strict handling procedures and ships all image sensor products in ESD-safe, clean-room-approved shipping containers. Products returned to ON Semiconductor for failure analysis should be handled under these same conditions and packed in its original packing materials, or the customer may be liable for the product.

ACCEPTANCE CRITERIA SPECIFICATION

The Product Acceptance Criteria is available on request. This document contains the criteria to which the LUPA4000 is tested before being shipped.

ORDERING CODE DEFINITION



ACRONYMS

Acronym	Description
ADC	analog-to-digital converter
AFE	analog front end
ANSI	American National Standards Institute
BGA	ball grid array
BL	black pixel data
CDM	Charged Device Model
CDS	correlated double sampling
CIS	CMOS image sensor
CMOS	complementary metal oxide semiconductor
CMY	cyan magenta yellow
CRC	cyclic redundancy check
DAC	digital-to-analog converter
DDR	double data rate
DFT	design for test
DNL	differential nonlinearity
DSNU	dark signal nonuniformity
EIA	Electronic Industries Alliance
ESD	electrostatic discharge
FE	frame end
FF	fill factor
FOT	frame overhead time
FPN	fixed pattern noise
FPS	frames per second
FS	frame start
HBM	Human Body Model
HMUX	horizontal multiplexer
I2C	inter-integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
IMG	regular pixel data

Acronym	Description
INL	integral nonlinearity
IP	intellectual property
JTAG	Joint Test Action Group
LE	line end
LS	line start
LSB	least significant bit
LVDS	low-voltage differential signaling
MBS	mixed boundary scan
MSB	most significant bit
MTF	modulation transfer function
NDR	nondestructive readout
NIR	near infrared
PGA	programmable gain amplifier
PLS	parasitic light sensitivity
PRBS	pseudo-random binary sequence
PRNU	pixel random nonuniformity
QE	quantum efficiency
RGB	red green blue
RMS	root mean square
ROI	region of interest
ROT	row overhead time
S/H	sample and hold
SNR	signal-to-noise ratio
SPI	serial peripheral interface
TAP	test access port
TBD	to be determined
TIA	Telecommunications Industry Association
TR	training pattern
uPGA	micro pin grid array

GLOSSARY

blooming	The leakage of charge from a saturated pixel into neighboring pixels.
camera gain constant	A constant that converts the number of electrons collected by a pixel into digital output (in DN). It can be extracted from photon transfer curves.
column noise	Variation of column mean signal strengths. The human eye is sensitive to line patterns so this noise is analyzed separately.
conversion gain	A constant that converts the number of electrons collected by a pixel into the voltage swing of the pixel. Conversion gain = q/C where q is the charge of an electron (1.602E 19 Coulomb) and C is the capacitance of the photodiode or sense node.
CDS	Correlated double sampling. This is a method for sampling a pixel where the pixel voltage after reset is sampled and subtracted from the voltage after exposure to light.
CFA	Color filter array. The materials deposited on top of pixels that selectively transmit color.
color crosstalk	The leakage of signal from one color channel into another when the imager is NOT saturated. The signal can leak through either optical means, in which a photon enters a pixel of the ¿wrong¿ color, or electrical means, in which a charge carrier generated within one pixel diffuses into a neighboring pixel.
CRA	Chief ray angle. Oblique rays that pass through the center of a lens system aperture stop. Color filter array, metal, and micro lens shifts are determined by the chief ray angle of the optical system. In general, optical systems with smaller CRA are desired to minimize color artifacts
DN	Digital number. The number of bits (8, 12, 14, …) should also be specified.
DNL	Differential nonlinearity (for ADCs)
DSNU	Dark signal nonuniformity. This parameter characterizes the degree of nonuniformity in dark leakage currents, which can be a major source of fixed pattern noise.
fill-factor	A parameter that characterizes the optically active percentage of a pixel. In theory, it is the ratio of the actual QE of a pixel divided by the QE of a photodiode of equal area. In practice, it is never measured.
grating monochromator	An instrument that produces a monochromatic beam of light. It typically consists of a broadband light source such as a tungsten lamp and a diffraction grating for selecting a particular wavelength.
INL	Integral nonlinearity (for ADCs)
luminance	Light flux per unit area in photometric units (lux)
IR	Infrared. IR light has wavelengths in the approximate range 750 nm to 1 mm.
irradiance	Light flux per unit area in radiometric units (W/m^2)
Lag	The persistence of signal after pixel reset when the irradiance changes from high to low values. In a video stream, lag appears as ‘ghost’ images that persist for one or more frames.
Lux	Photometric unit of luminance (at 550 nm, 1 lux = 1 lumen/m^2 = 1/683 W/m^2)
NIR	Near Infrared. NIR is part of the infrared portion of the spectrum and has wavelengths in the approximate range 750 nm to 1400 nm.
pixel noise	Variation of pixel signals within a region of interest (ROI). The ROI typically is a rectangular portion of the pixel array and may be limited to a single color plane.
photometric units	Units for light measurement that take into account human physiology.
photon transfer	Measurement in which a bare imager (no external lens) is irradiated with uniform light from dark to saturation levels. Typically the source is collimated, monochromatic 550 nm light. Chapter 2 of J. Janesick’s book, *Scientific Charge Coupled Devices,* describes the technique in detail.
PLS	Parasitic light sensitivity. Parasitic discharge of sampled information in pixels that have storage nodes.
PRNU	Photo-response nonuniformity. This parameter characterizes the spread in response of pixels, which is a source of FPN under illumination.
QE	Quantum efficiency. This parameter characterizes the effectiveness of a pixel in capturing photons and converting them into electrons. It is photon wavelength and pixel color dependent.
radiometric units	Units for light measurement based on physics.
read noise	Noise associated with all circuitry that measures and converts the voltage on a sense node or photodiode into an output signal.
reset	The process by which a pixel photodiode or sense node is cleared of electrons. Soft reset occurs when the reset transistor is operated below the threshold. Hard reset occurs when the reset transistor is operated above threshold.

reset noise	Noise due to variation in the reset level of a pixel. In 3T pixel designs, this noise has a component (in units of volts) proportionality constant depending on how the pixel is reset (such as hard and soft). In 4T pixel designs, reset noise can be removed with CDS.
responsivity	The standard measure of photodiode performance (regardless of whether it is in an imager or not). Units are typically A/W and are dependent on the incident light wavelength. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units.
reverse saturation	Phenomenon in which the signal level decreases with increasing light intensity. It typically occurs at irradiance levels much higher than saturation, such as an image taken of the sun.
ROI	Region of interest. The area within a pixel array chosen to characterize noise, signal, crosstalk, and so on. The ROI can be the entire array or a small subsection; it can be confined to a single color plane.
row noise	Variation of row mean signal strengths. The human eye is sensitive to line patterns, so this noise is analyzed separately.
sense node	In 4T pixel designs, a capacitor used to convert charge into voltage. In 3T pixel designs it is the photodiode itself.
sensitivity	A measure of pixel performance that characterizes the rise of the photodiode or sense node signal in Volts upon illumination with light. Units are typically V/(W/m^2)/sec and are dependent on the incident light wavelength. Sensitivity measurements are often taken with 550 nm incident light. At this wavelength, 1 683 lux = 1 W/m^2; the units of sensitivity are quoted in V/lux/sec. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units.
shot noise	Noise that arises from measurements of discretised quanta (electrons or photons). It follows a Poisson distribution with the strength of the noise increasing as the square root of the signal.
spectral response	The photon wavelength dependence of sensitivity or responsivity.
SNR	Signal-to-noise ratio. This number characterizes the ratio of the fundamental signal to the noise spectrum up to half the Nyquist frequency.
temporal noise	Noise that varies from frame to frame. In a video stream, temporal noise is visible as twinkling pixels.
tint	Integration time.

APPENDIX A: FREQUENTLY ASKED QUESTIONS

Q: How does the dual (multiple) slope extended dynamic range mode work?

A: The green lines in Figure 27 are the analog signal on the photodiode, which decrease as a result of exposure. The slope is determined by the amount of light at each pixel (the more light the steeper the slope). When the pixels reach the saturation level, the analog signal does not change despite further exposure. Without any double slope, pulse pixels p3 and p4 reaches saturation before the sample moment of the analog values, no signal is acquired without double slope. When double slope is enabled a second reset pulse is given (blue line) at a certain time before the end of the integration time. This double slope reset pulse resets the analog signal of the pixels below this level to the reset level. After the reset the analog signal starts to decrease with the same slope as before the double slope reset pulse. If the double slope reset pulse is placed at the end of the integration time (90% for instance) the analog signal that reaches the saturation levels are not saturated anymore (this increases the optical dynamic range) at read out. Note that pixel signals above the double slope reset level are not influenced by this double slope reset pulse (p1 and p2).

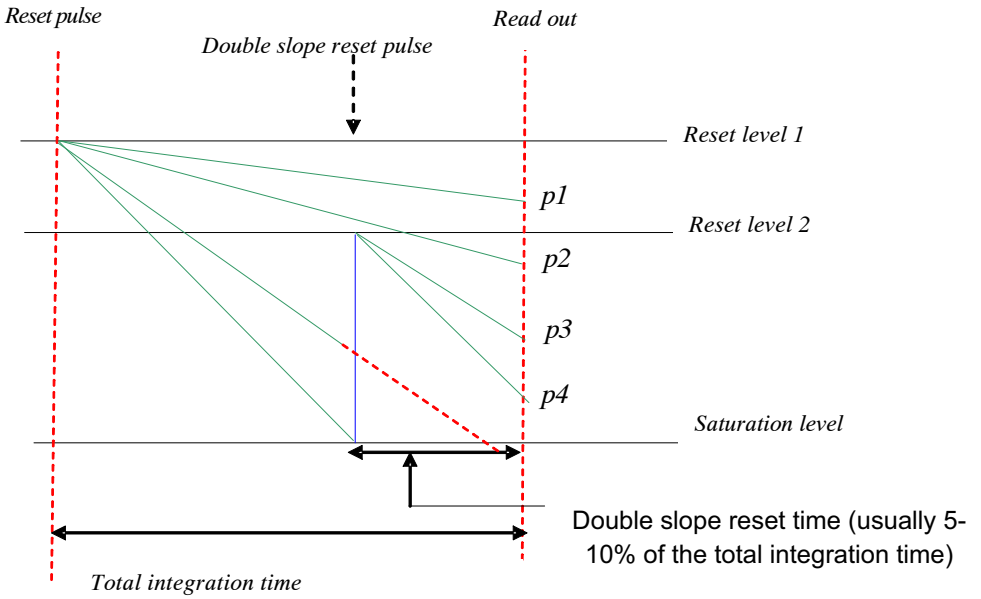


Figure 25. Dual Slope Diagram

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