

NP119N04NUK

40 V – 120 A – N-channel Power MOS FET Application: Automotive

R07DS1252EJ0100 Rev.1.00 Mar 30, 2015

Description

The NP119N04NUK is N-channel MOS Field Effect Transistors designed for high current switching applications.

Features

- Super low on-state resistance $R_{DS(on)} = 2.15 \ m\Omega \ MAX. \ (V_{GS} = 10 \ V, \ I_D = 60 \ A)$
- Low C_{iss} : $C_{iss} = 7400 \text{ pF TYP.} (V_{DS} = 25 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Part No. Lead Plating		Package
NP119N04NUK-S18-AY *1	Pure Sn (Tin)	Tube 50 p/tube	TO-262 (MP-25SK)

Note: *1 Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	40	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±120	А
Drain Current (pulse) *1	I _{D(pulse)}	±480	А
Total Power Dissipation (T _C = 25°C)	P _{T1}	250	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.8	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	-55 to +175	°C
Repetitive Avalanche Current *2	I _{AR}	56	А
Repetitive Avalanche Energy *2	Ear	313	mJ

Notes: *1 T_C = 25°C, $P_W \le 10 \mu s$, Duty Cycle $\le 1\%$

Thermal Resistance

^{*2} R_G = 25 Ω , V_{GS} = 20 V \rightarrow 0 V

Electrical Characteristics (T_A = 25°C)

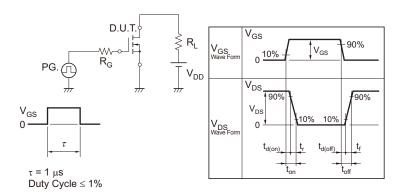
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	IDSS	_	_	1	μΑ	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	Igss	_	_	±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	>	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$
Forward Transfer Admittance *1	y _{fs}	50	114	_	S	$V_{DS} = 5 \text{ V}, I_{D} = 60 \text{ A}$
Drain to Source On-state Resistance *1	R _{DS(on)}	_	1.80	2.15	mΩ	$V_{GS} = 10 \text{ V}, I_D = 60 \text{ A}$
Input Capacitance	C _{iss}	_	7400	11100	pF	V _{DS} = 25 V
Output Capacitance	Coss	_	1000	1500	pF	$V_{GS} = 0 V$
Reverse Transfer Capacitance	C _{rss}	_	390	710	pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)}	_	30	70	ns	$V_{DD} = 20 \text{ V}, I_D = 60 \text{ A}$
Rise Time	t _r	_	11	30	ns	V _{GS} = 10 V
Turn-off Delay Time	t _{d(off)}	_	105	210	ns	$R_G = 0 \Omega$
Fall Time	t _f	_	13	40	ns	
Total Gate Charge	Q_G	_	130	195	nC	V _{DD} = 32 V
Gate to Source Charge	Q _{GS}	_	32	_	nC	$V_{GS} = 10 \text{ V}$
Gate to Drain Charge	Q_{GD}	_	31	_	nC	I _D = 120 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$	_	0.9	1.5	V	$I_F = 120 \text{ A}, V_{GS} = 0 \text{ V}$
Reverse Recovery Time	t _{rr}	_	56	_	ns	I _F = 120 A, V _{GS} = 0 V
Reverse Recovery Charge	Qrr		80	_	nC	di/dt = 100 A/μs

Note: *1 Pulsed test

TEST CIRCUIT 1 AVALANCHE CAPABILITY

$V_{GS} = 20 \rightarrow 0 \text{ V}$ V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DS} V_{DS} V_{DS} V_{DS} V_{DS}

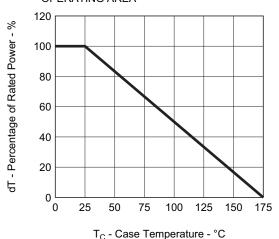
TEST CIRCUIT 2 SWITCHING TIME



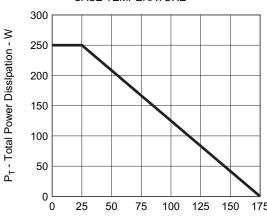
TEST CIRCUIT 3 GATE CHARGE

Typical Characteristics $(T_A = 25^{\circ}C)$

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

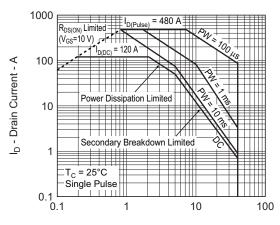


TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



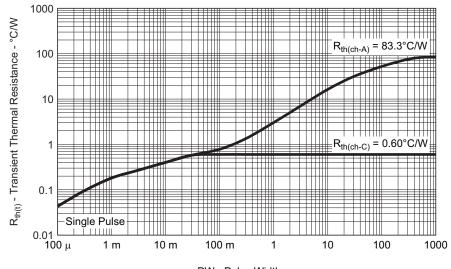
T_C - Case Temperature - °C

FORWARD BIAS SAFE OPERATING AREA



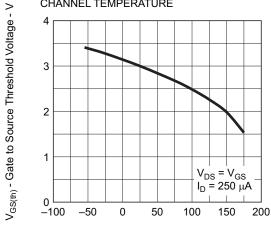
 V_{DS} - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



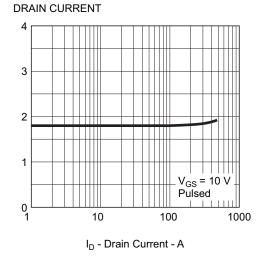
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE 600 500 I_D - Drain Current - A 400 300 200 100 V_{GS} = 10 VPulsed 0 0.2 0.4 0.6 1.0 0 8.0 V_{DS} - Drain to Source Voltage - V



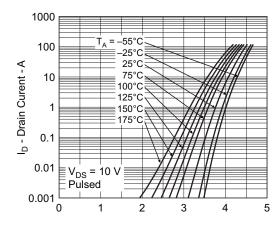


DRAIN TO SOURCE ON-STATE RESISTANCE vs.

T_{ch} - Channel Temperature - °C

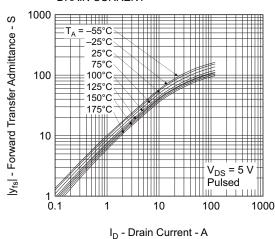


FORWARD TRANSFER CHARACTERISTICS

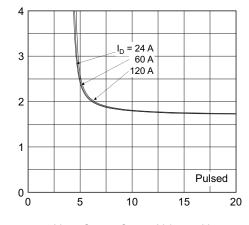


V_{GS} - Gate to Source Voltage - V

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



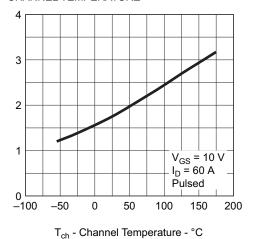
 V_{GS} - Gate to Source Voltage - V

 $R_{DS(on)}$ - Drain to Source On-State Resistance - $m\Omega$

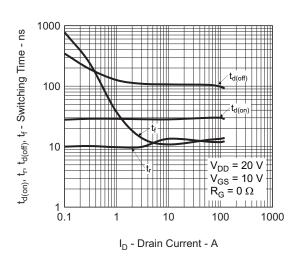
 $R_{DS(on)}$ - Drain to Source On-State Resistance - $m\Omega$

 $R_{\text{DS(on)}}$ - Drain to Source On-State Resistance - $m\Omega$

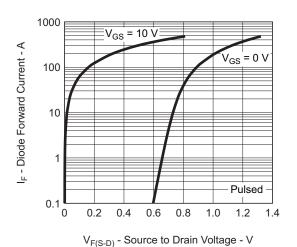
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



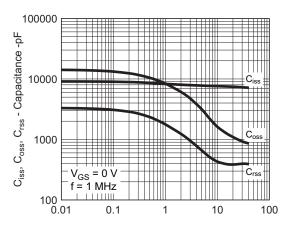
SWITCHING CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

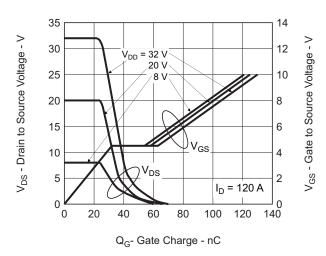


CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

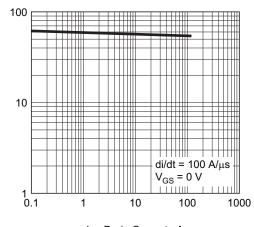


 V_{DS} - Drain to Source Voltage - V

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REVERSE RECOVERY TIME vs. DRAIN CURRENT

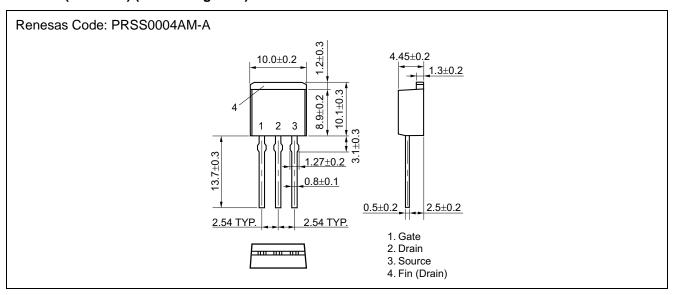


I_F - Drain Current - A

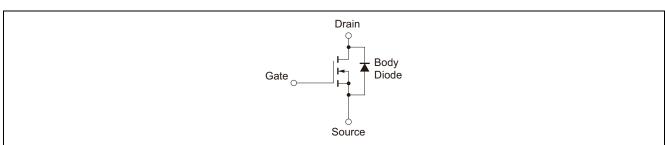
t_{rr} - Reverse Recovery Time - ns

Package Drawing (Unit: mm)

TO-262 (MP-25SK) (Mass: 1.8 g TYP.)



Equivalent Circuit



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History

NP119N04NUK Data Sheet

			Description			
	Rev.	Date	Page Summary			
1.	.00	Mar 30, 2015	_	First Edition Issued		

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