NP120N04NUK

40 V – 120 A – N-channel Power MOS FET
Application: Automotive

R07DS1253EJ0100
Rev.1.00
Mar 30, 2015

Description

The NP120N04NUK is N-channel MOS Field Effect Transistors designed for high current switching applications.

Features

- Super low on-state resistance
  $R_{DS(on)}$ = 1.95 mΩ MAX. (V_{GS} = 10 V, I_D = 60 A)
- Low C_{iss}: C_{iss} = 8300 pF TYP. (V_{DS} = 25 V)
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Packing	Package
NP120N04NUK-S18-AY *1	Pure Sn (Tin)	Tube 50 p/tube	TO-262 (MP-25SK)

Note: *1 Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	40	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±120	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±480	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	288	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.8	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Repetitive Avalanche Current *2	I_{AR}	66	A
Repetitive Avalanche Energy *2	E_{AR}	435	mJ

Notes: *1 T_C = 25°C, $P_W \leq$ 10 μs, Duty Cycle ≤ 1%
*2 R_G = 25 Ω, V_{GS} = 20 V → 0 V

Thermal Resistance

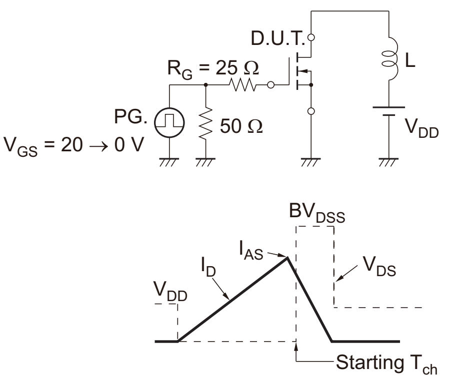
Channel to Case Thermal Resistance	$R_{th(ch-C)}$	0.52	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	°C/W

Electrical Characteristics (T_A = 25°C)

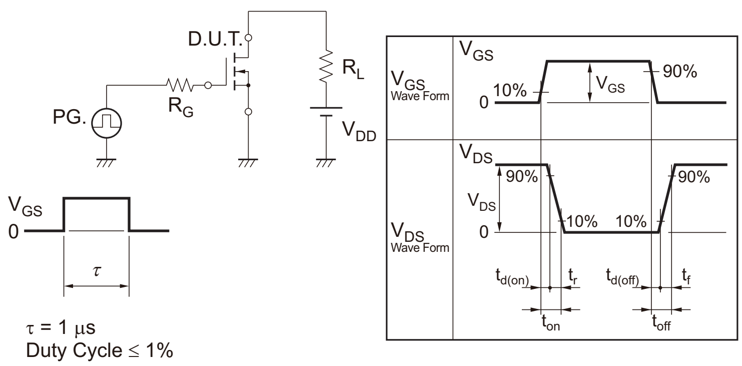
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 40 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	±100	nA	V_{GS} = ±20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	V_{DS} = V_{GS}, I_D = 250 µA
Forward Transfer Admittance *1	$\| y_{fs} \|$	60	125	—	S	V_{DS} = 5 V, I_D = 60 A
Drain to Source On-state Resistance *1	$R_{DS(on)}$	—	1.65	1.95	mΩ	V_{GS} = 10 V, I_D = 60 A
Input Capacitance	C_{iss}	—	8300	12450	pF	V_{DS} = 25 V V_{GS} = 0 V f = 1 MHz
Output Capacitance	C_{oss}	—	1200	1800	pF	
Reverse Transfer Capacitance	C_{rss}	—	440	800	pF	
Turn-on Delay Time	$t_{d(on)}$	—	30	70	ns	V_{DD} = 20 V, I_D = 60 A V_{GS} = 10 V R_G = 0 Ω
Rise Time	t_r	—	11	30	ns	
Turn-off Delay Time	$t_{d(off)}$	—	115	230	ns	
Fall Time	t_f	—	13	40	ns	
Total Gate Charge	Q_G	—	160	240	nC	V_{DD} = 32 V V_{GS} = 10 V I_D = 120 A
Gate to Source Charge	Q_{GS}	—	42	—	nC	
Gate to Drain Charge	Q_{GD}	—	42	—	nC	
Body Diode Forward Voltage *1	$V_{F(S-D)}$	—	0.9	1.5	V	I_F = 120 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	—	61	—	ns	I_F = 120 A, V_{GS} = 0 V di/dt = 100 A/µs
Reverse Recovery Charge	Q_{rr}	—	100	—	nC	

Note: *1 Pulsed test

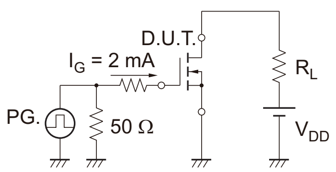
TEST CIRCUIT 1 AVALANCHE CAPABILITY



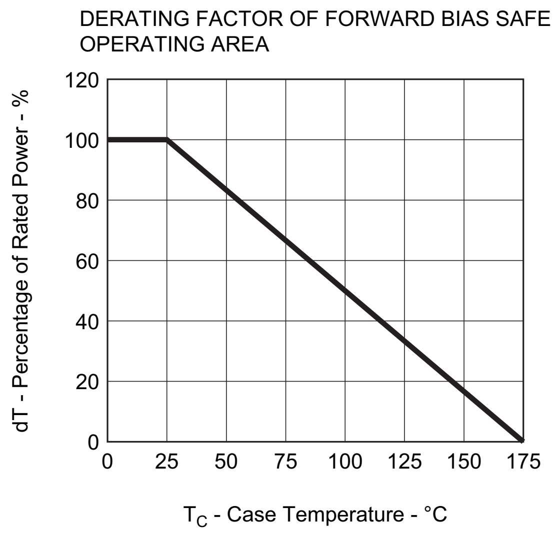
TEST CIRCUIT 2 SWITCHING TIME

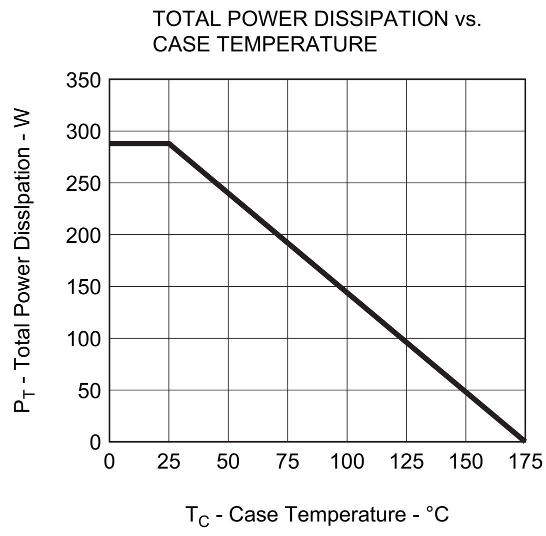


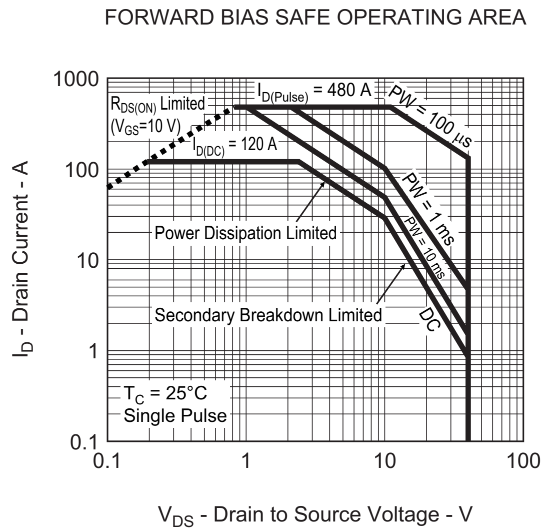
TEST CIRCUIT 3 GATE CHARGE

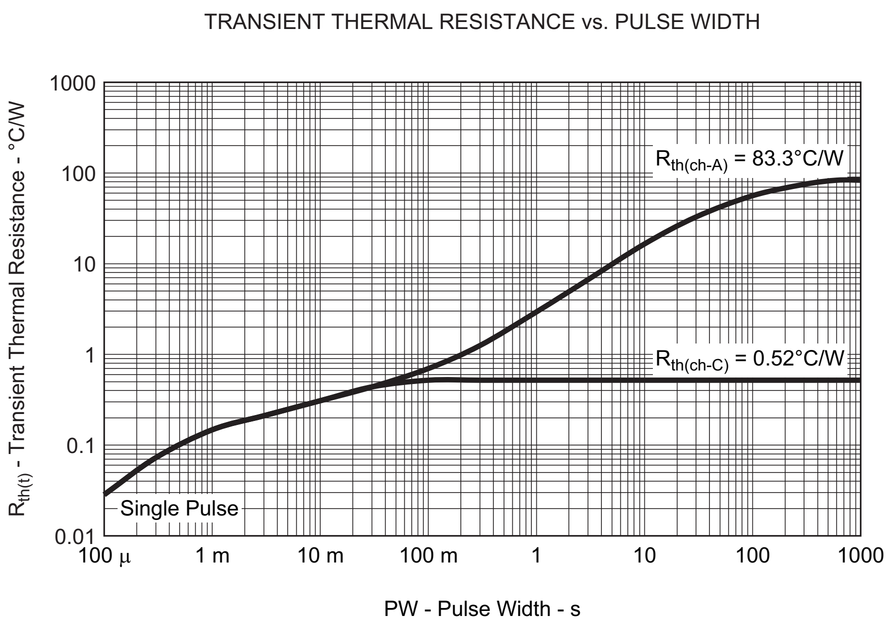


Typical Characteristics (T_A = 25°C)

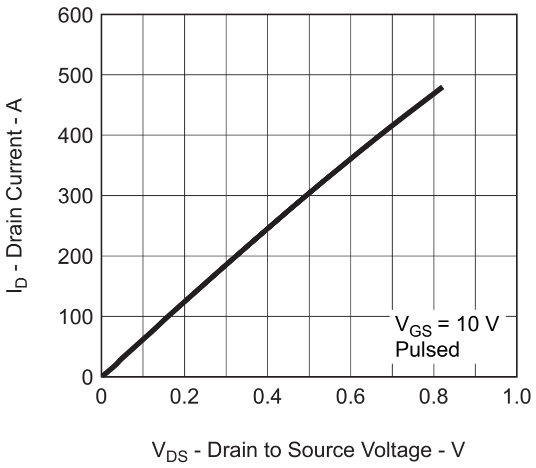




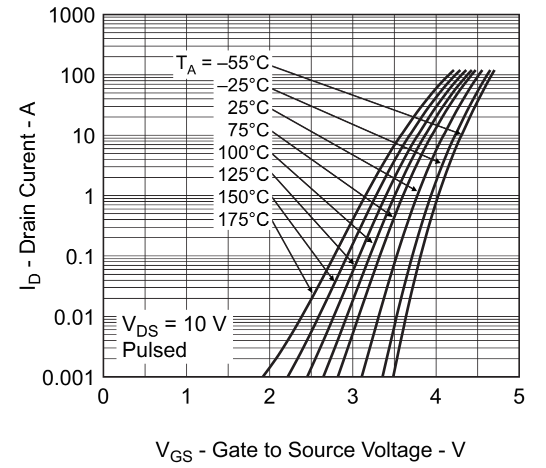




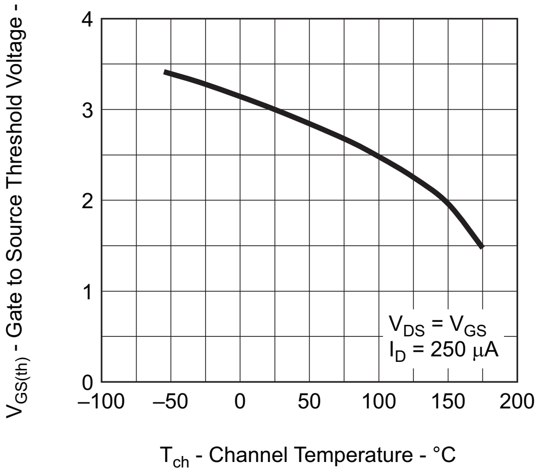
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



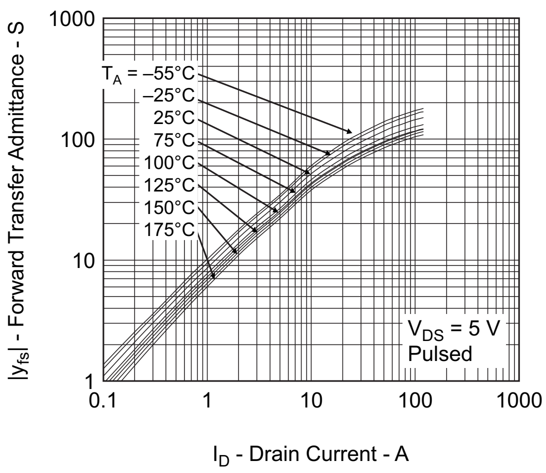
FORWARD TRANSFER CHARACTERISTICS



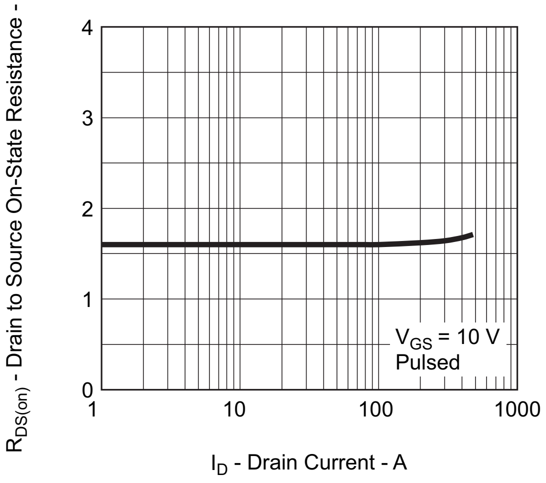
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



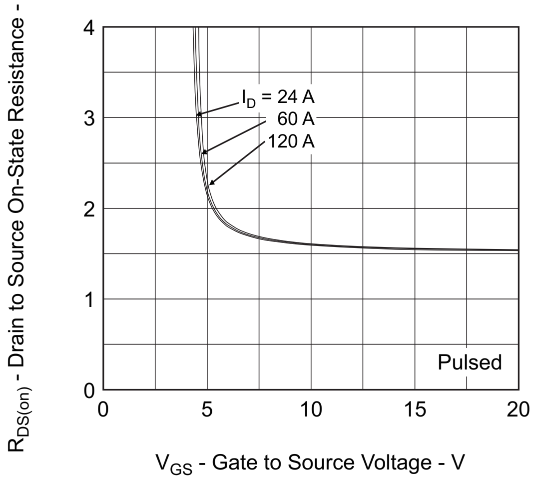
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



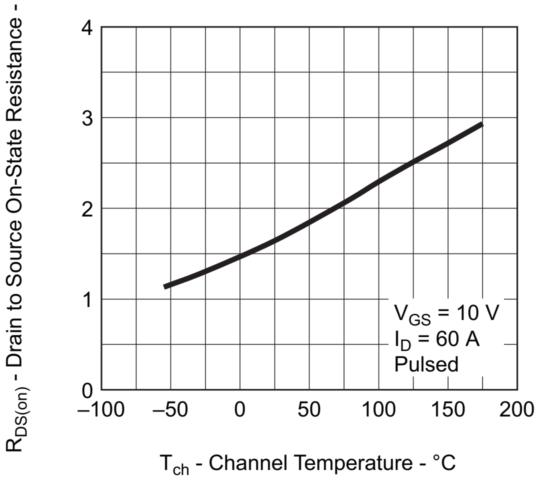
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



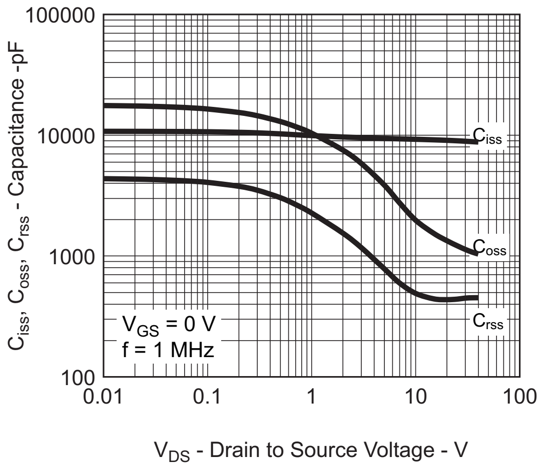
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



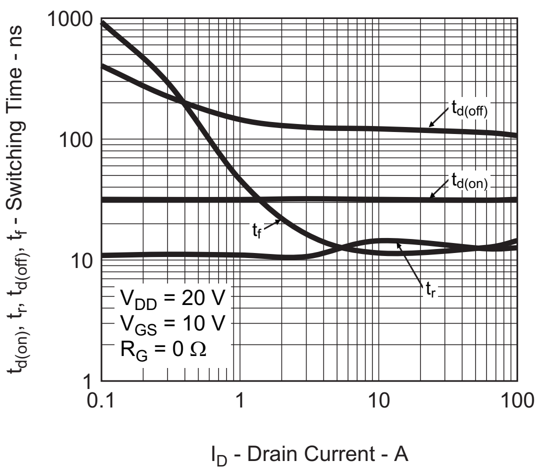
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



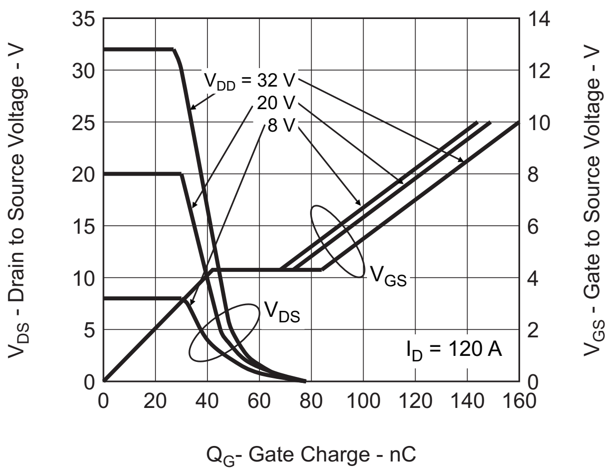
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



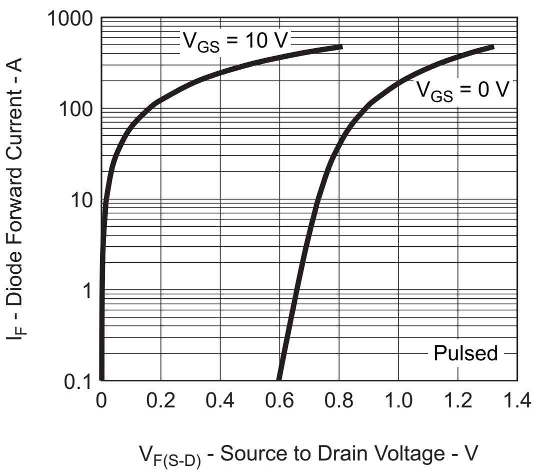
SWITCHING CHARACTERISTICS



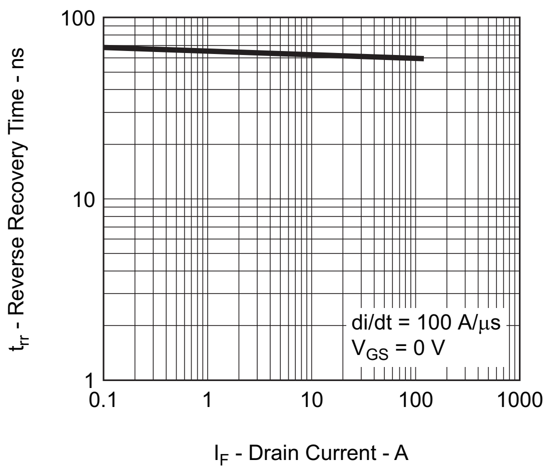
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



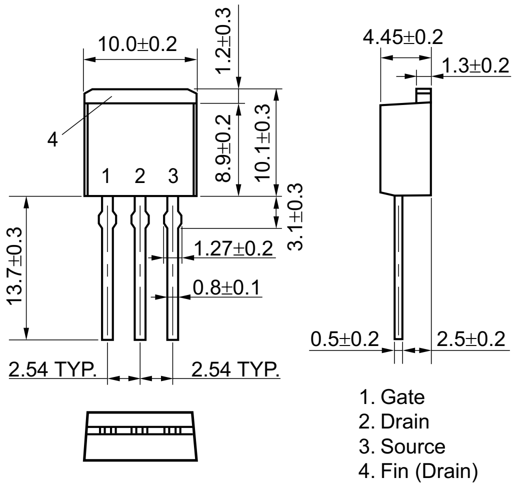
REVERSE RECOVERY TIME vs. DRAIN CURRENT



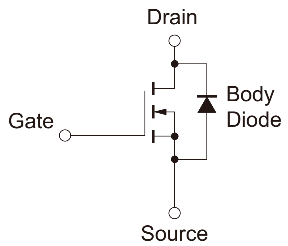
Package Drawing (Unit: mm)

TO-262 (MP-25SK) (Mass: 1.8 g TYP.)

Renesas Code: PRSS0004AM-A



Equivalent Circuit



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History	NP120N04NUK Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Mar 30, 2015	—	First Edition Issued

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