DATA SHEET



MOS FIELD EFFECT TRANSISTOR NP160N04TDG

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The NP160N04TDG is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE		
NP160N04TDG-E1-AY Note					
NP160N04TDG-E2-AY Note	Pure Sn (Tin)	Tape 800 p/reel	TO-263-7pin (MP-25ZT) typ. 1.5 g		

Note Pb-free (This product does not contain Pb in the external electrode).

FEATURES

• Super low on-state resistance

 $R_{DS(on)1}$ = 1.6 m Ω TYP. / 2.0 m Ω MAX. (VGS = 10 V, ID = 80 A)

 $R_{DS(on)2}$ = 2.2 m Ω TYP. / 5.4 m Ω MAX. (VGS = 4.5 V, ID = 80 A)

High Current Rating
 I_{D(DC)} = ±160 A

· Logic level drive type

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C)

Drain to Source Voltage (Vos = 0 V)	VDSS	40	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	I _{D(DC)}	±160	Α
Drain Current (pulse) Note1	D(pulse)	±640	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	220	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.8	W
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	-55 to +175	°C
Single Avalanche Energy Note2	Eas	372	mJ
Repetitive Avalanche Current Note3	IAR	61	Α
Repetitive Avalanche Energy Note3	Ear	372	mJ

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = 20 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V, L = 100 μ H

3. Rg = 25 Ω , Tch(peak) $\leq 150^{\circ}$ C

THERMAL RESISTANCE

Channel to Case Thermal Resistance	Rth(ch-C)	0.68	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	83.3	°C/W

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Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

NEC 102851

(TO-263-7pin)

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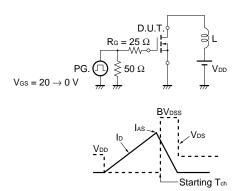
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ELECTRICAL CHARACTERISTICS (TA = 25°C)

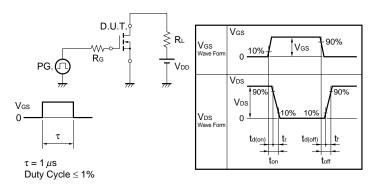
	1					
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 40 V, V _{GS} = 0 V			1	μА
Gate Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	yfs	V _{DS} = 5 V, I _D = 40 A	37	94		S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = 10 V, I _D = 80 A		1.6	2.0	mΩ
	RDS(on)2	V _{GS} = 4.5 V, I _D = 80 A		2.2	5.4	mΩ
Input Capacitance	Ciss	V _{DS} = 25 V,		10500	15750	pF
Output Capacitance	Coss	V _{GS} = 0 V,		980	1470	pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		630	1140	pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 20 V, I _D = 80 A,		35	80	ns
Rise Time	tr	V _{GS} = 10 V,		55	140	ns
Turn-off Delay Time	t _{d(off)}	R _G = 0 Ω		107	220	ns
Fall Time	tr			17	50	ns
Total Gate Charge Note	Q _G	V _{DD} = 32 V,		180	270	nC
Gate to Source Charge	Q _G s	V _{GS} = 10 V,		30		nC
Gate to Drain Charge	Q _{GD}	I _D = 160 A		57		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 160 A, V _{GS} = 0 V		0.9	1.5	V
Reverse Recovery Time	trr	I _F = 160 A, V _{GS} = 0 V,		49		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ <i>µ</i> s		60		nC

Note Pulsed test

TEST CIRCUIT 1 AVALANCHE CAPABILITY



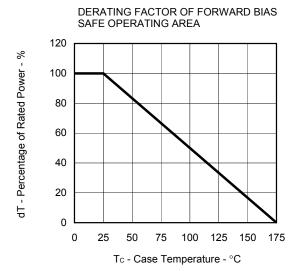
TEST CIRCUIT 2 SWITCHING TIME

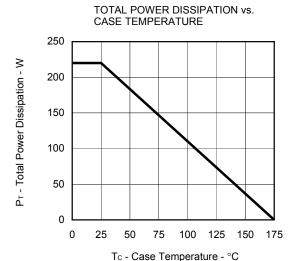


TEST CIRCUIT 3 GATE CHARGE

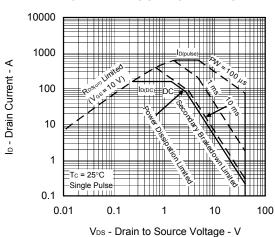
$$\begin{array}{c|c} D.U.T. \\ \hline IG = 2 \text{ mA} \\ \hline WV - 0 \end{array} \begin{array}{c} \\ \\ \\ \\ \end{array} \begin{array}{c} \\ \\ \\ \\ \\ \end{array} \begin{array}{c} \\ \\ \\ \\ \end{array} \begin{array}{c} \\ \\ \\ \\ \end{array} \begin{array}{c} \\ \\ \\ \\ \\ \end{array} \begin{array}{c} \\ \\ \\ \\ \\$$

TYPICAL CHARACTERISTICS (TA = 25°C)

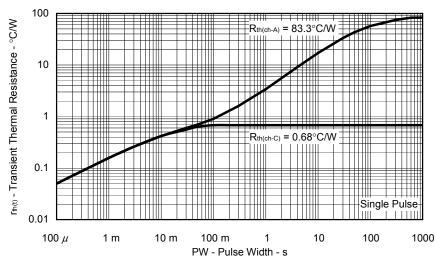


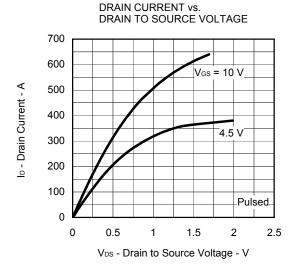


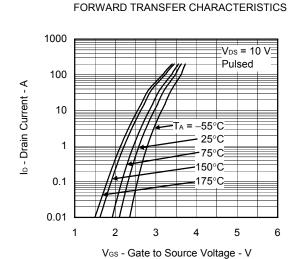
FORWARD BIAS SAFE OPERATING AREA

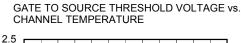


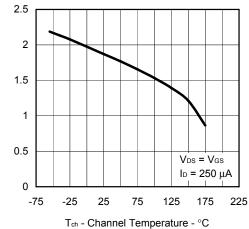
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



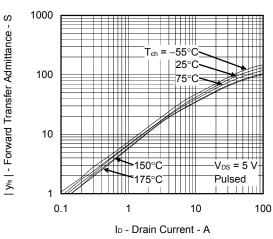




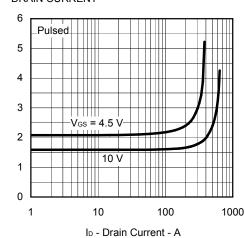




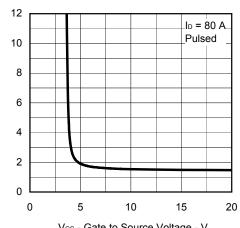
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. **DRAIN CURRENT**



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

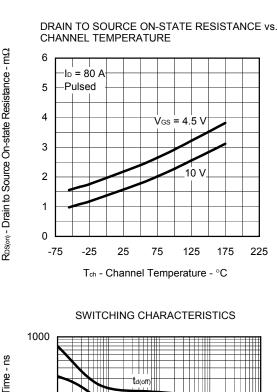


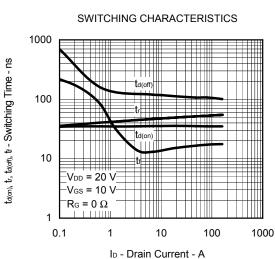
V_{GS} - Gate to Source Voltage - V

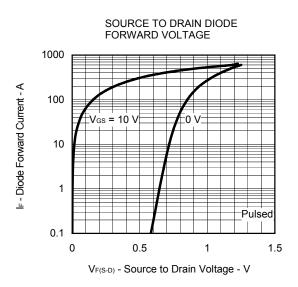
 $\mathsf{Res}_{(\mathsf{on})}$ - Drain to Source On-state Resistance - $m\Omega$

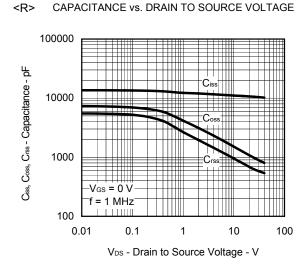
Ves(th) - Gate to Source Threshold Voltage - V

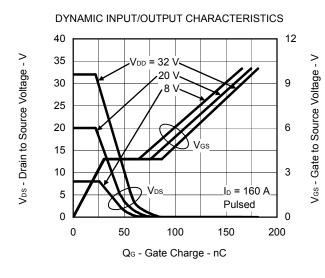
R_{DS(on)} - Drain to Source On-state Resistance - mΩ

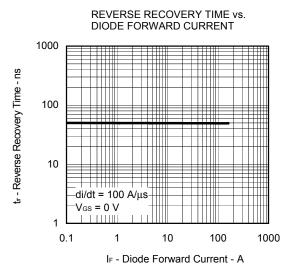




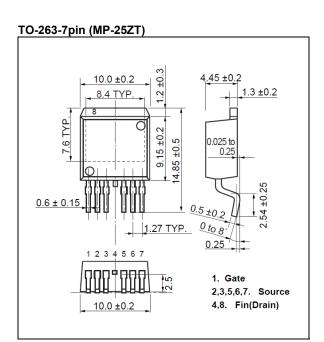




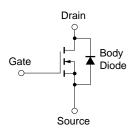




PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT

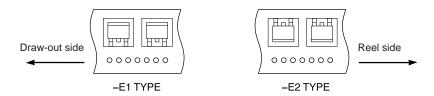


Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

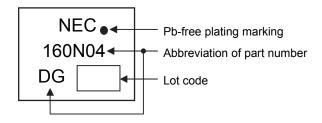
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TAPE INFORMATION

There are two types (-E1, -E2) of taping depending on the direction of the device.



MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

The NP160N04TDG should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol	
Infrared reflow	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	IR60-00-3	
Partial heating	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350	

Caution Do not use different soldering methods together (except for partial heating).

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