

**100V N-Channel Enhancement Mode MOSFET**
**Description**

The NP2N11MR uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and high density cell Design for ultra low on-resistance. This device is suitable for use as a load switch or in PWM applications.

**General Features**

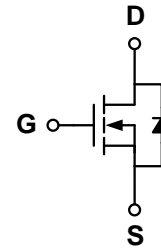
- ◆  $V_{DS} = 110V$ ,  $I_D = 2A$   
 $R_{DS(ON)}(Typ.) = 220m\Omega$  @  $V_{GS} = 10V$   
 $R_{DS(ON)}(Typ.) = 240m\Omega$  @  $V_{GS} = 4.5V$
- ◆ High power and current handling capability
- ◆ Lead free product is acquired
- ◆ Surface mount package

**Application**

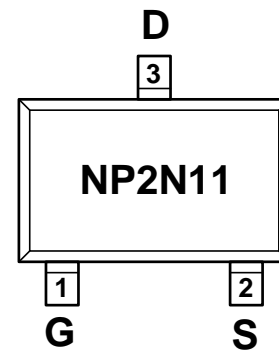
- ◆ PWM applications
- ◆ Load switch

**Package**

- ◆ SOT-23-3L


**Schematic diagram**

**Marking and pin assignment**

SOT-23-3L  
(TOP VIEW)


**Ordering Information**

Part Number	Storage Temperature	Package	Devices Per Reel
NP2N11MR-G	-55°C to +150°C	SOT-23-3L	3000

**Absolute Maximum Ratings (TA=25°C unless otherwise noted)**

parameter	symbol	limit	unit
Drain-source voltage	$V_{DS}$	110	V
Gate-source voltage	$V_{GS}$	±20	V
Drain current-continuous@Tj=125°C -pulse $d^C$	$I_D$	2	A
	$I_{DM}$	8	A
Drain-source Diode forward current	$I_S$	2	A
Avalanche Current	$I_{AS}$	4.8	A
Single Pulse Avalanche Energy	$E_{AS}$	6.3	mJ
Maximum power dissipation <sup>B</sup>	$P_D$	1.25	W
Operating junction Temperature range	$T_j$	-55—150	°C

**Electrical Characteristics** (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>OFF Characteristics</b>						
Drain-source breakdown voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	110	-	-	V
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=110V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-body leakage	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	$\pm 100$	nA
<b>ON Characteristics</b>						
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.9	2.5	V
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=2A$	-	220	240	m $\Omega$
		$V_{GS}=4.5V, I_D=2A$		240	260	
Forward transconductance	$g_{fs}$	$V_{GS}=5V, I_D=1A$	1	-	-	S
<b>Dynamic Characteristics</b>						
Input capacitance	$C_{ISS}$	$V_{DS}=55V, V_{GS}=0V$ $f=1.0MHz$	-	190	-	pF
Output capacitance	$C_{OSS}$		-	22	-	
Reverse transfer capacitance	$C_{RSS}$		-	13	-	
<b>Switching Characteristics</b>						
Turn-on delay time	$t_{D(ON)}$	$V_{DD}=55V$ $R_L=39\text{ ohm}$ $V_{GS}=10V$ $R_G=1\text{ ohm}$	-	6	-	ns
Rise time	$t_r$		-	10	-	
Turn-off delay time	$t_{D(OFF)}$		-	10	-	
Fall time	$t_f$		-	6	-	
Total gate charge	$Q_g$	$V_{DS}=55V$ $I_D=1.3A$ $V_{GS}=10V$	-	5.2	-	nC
Gate-source charge	$Q_{gs}$		-	0.75	-	
Gate-drain charge	$Q_{gd}$		-	1.4	-	
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
Diode forward voltage	$V_{SD}$	$V_{GS}=0V, I_s=2A$	-	0.76	1.16	V

**Thermal Characteristics**

Parameter	Symbol	Typ.	Max.	Unit
Maximum Junction-to-Ambient <sup>A</sup>	$t \leq 10s$	70	90	$^{\circ}C/W$
Maximum Junction-to-Ambient <sup>A D</sup>	Steady-State	100	125	
Maximum Junction-to-Lead	Steady-State	62	80	

A. The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^{\circ}C$ . The value in any given application depends on the user's specific board design.

B. The power dissipation PD is based on  $T_{J(MAX)}=150^{\circ}C$ , using  $\leq 10s$  junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=150^{\circ}C$ . Ratings are based on low frequency and duty cycles to keep initial  $T_J=25^{\circ}C$ .

D. The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to lead  $R_{\theta JL}$  and lead to ambient.

## Typical Performance Characteristics

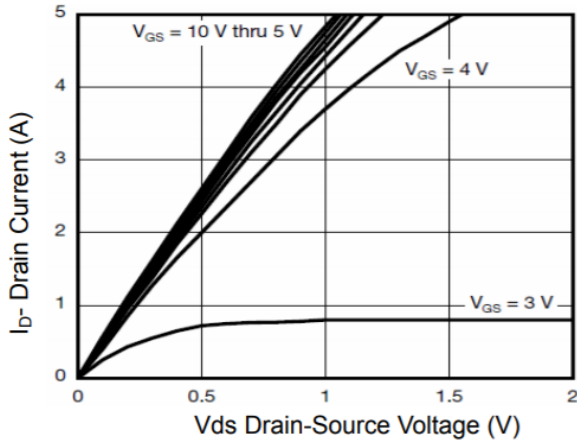


Figure 1 Output Characteristics

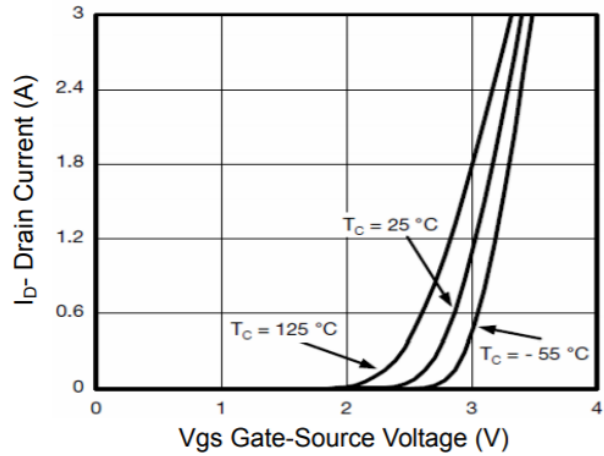


Figure 2 Transfer Characteristics

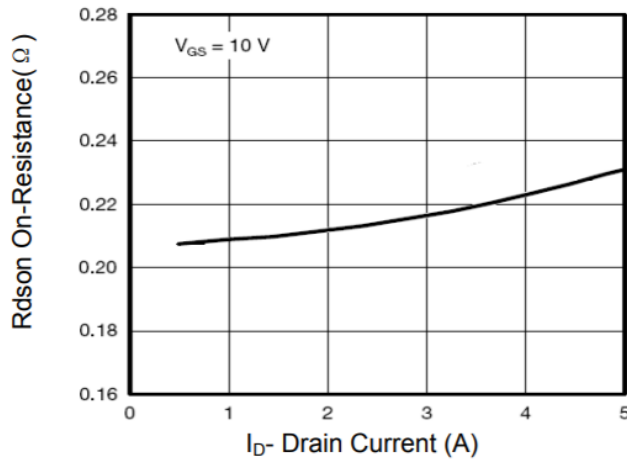


Figure 3 Rdson- Drain Current

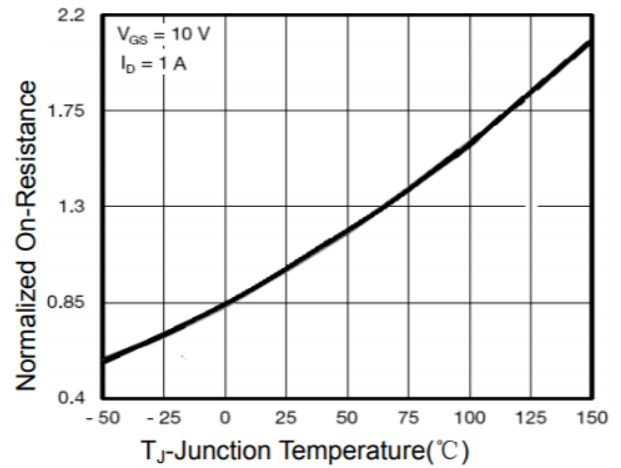


Figure 4 Rdson-Junction Temperature

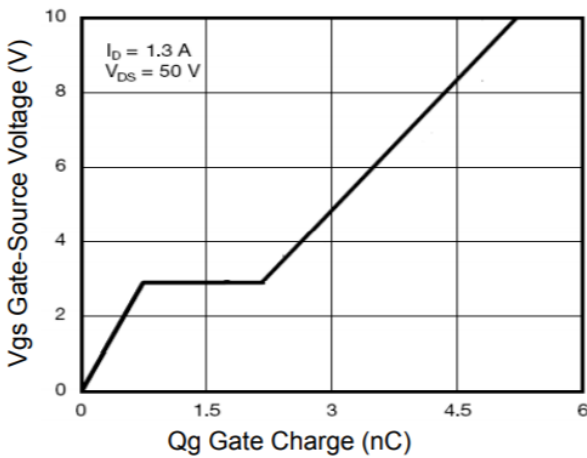


Figure 5 Gate Charge

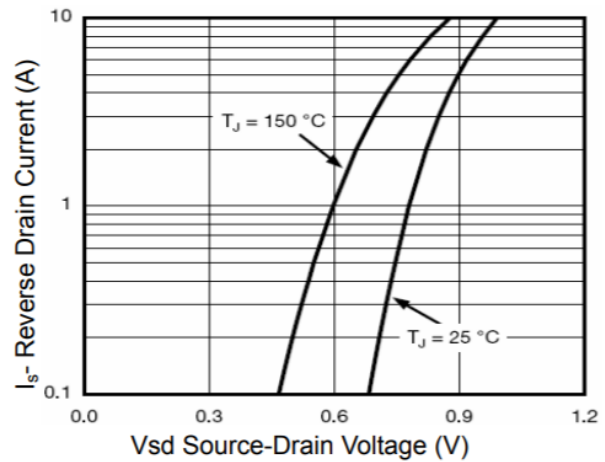


Figure 6 Source- Drain Diode Forward

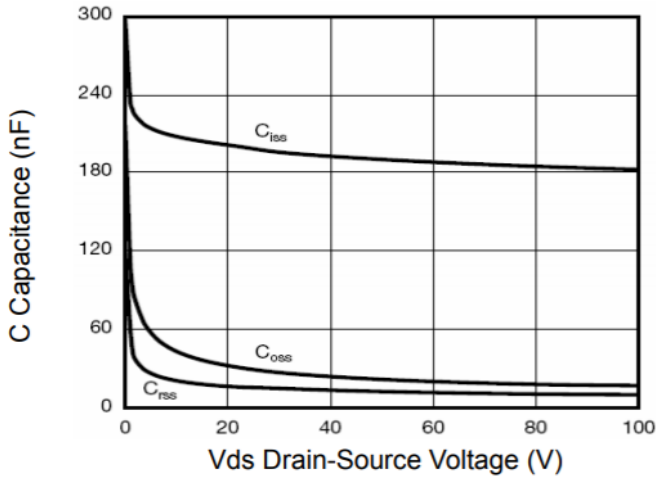


Figure 7 Capacitance vs Vds

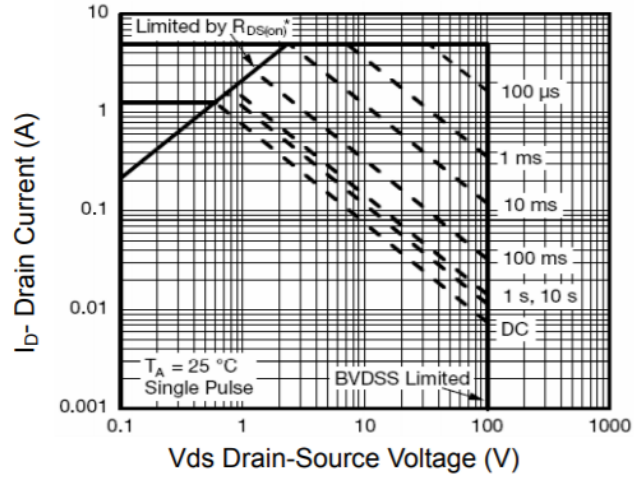


Figure 8 Safe Operation Area

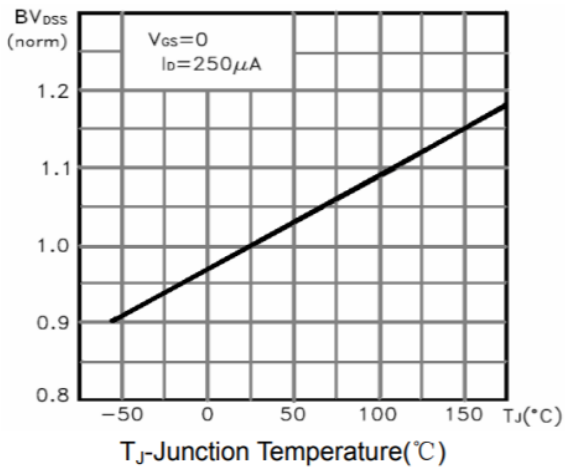


Figure 9  $BV_{DSS}$  vs Junction Temperature

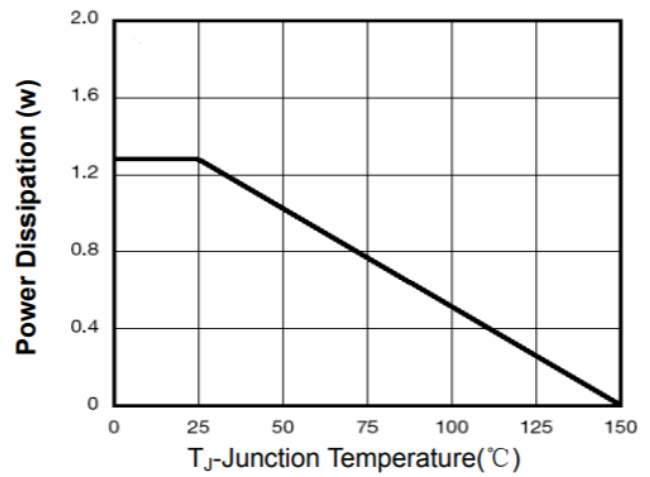


Figure 10 Power De-ratin

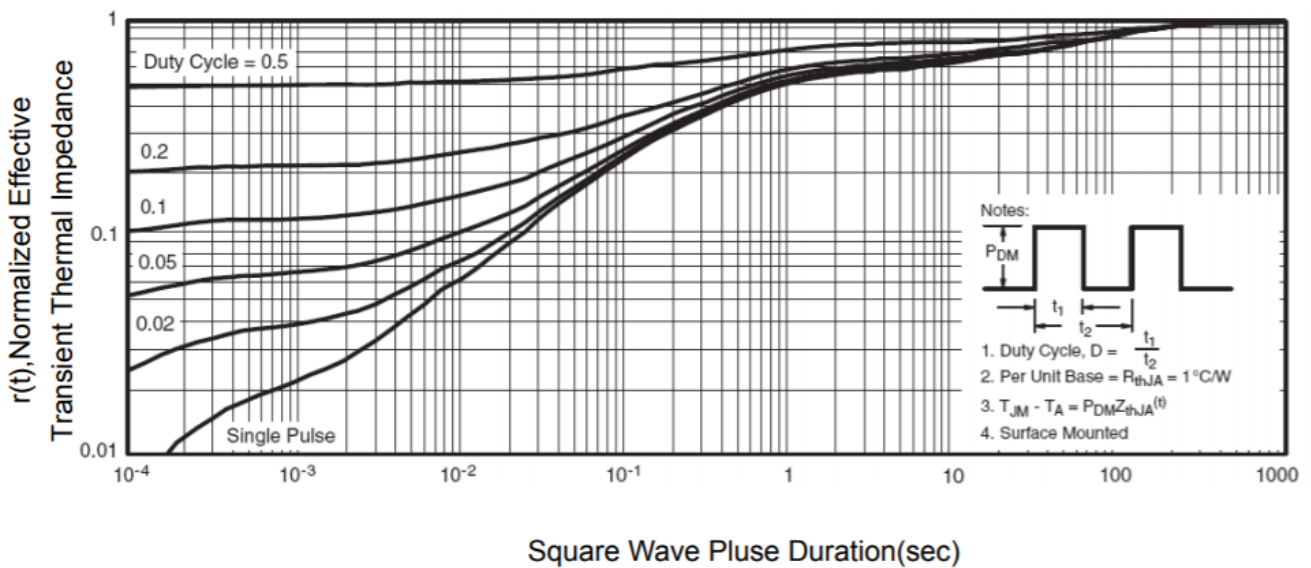
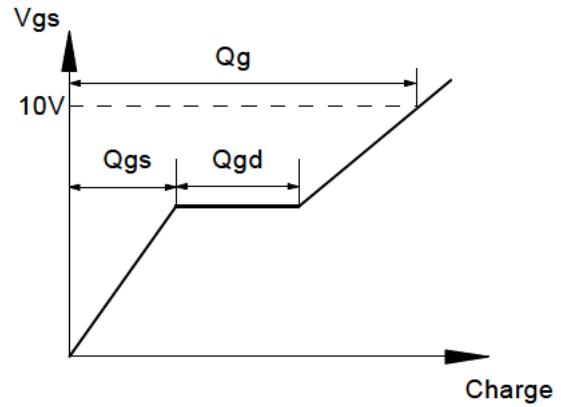
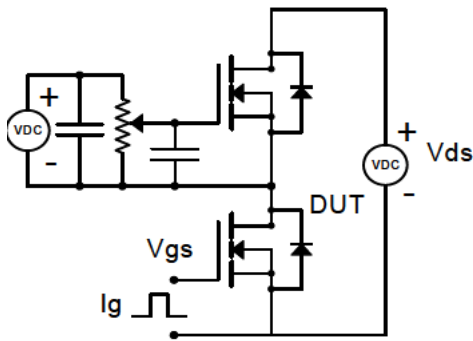


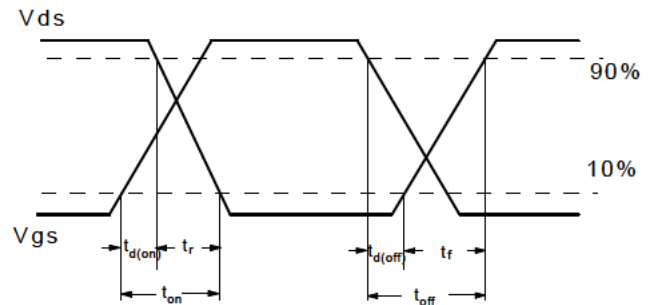
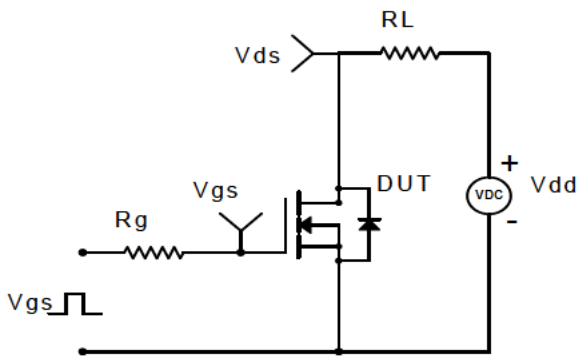
Figure 11 Normalized Maximum Transient Thermal Impedance

Gate Charge Test Circuit & Waveform

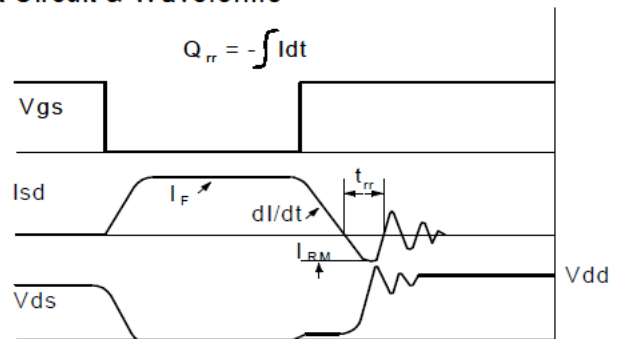
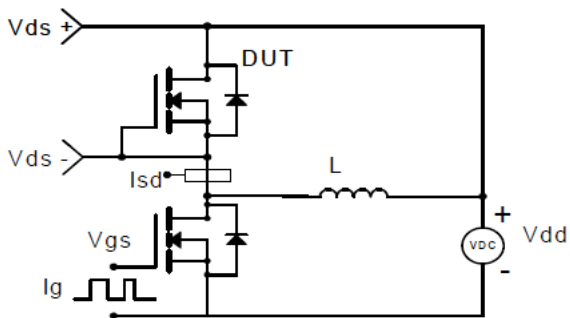


Resistive Switching Test Circuit & Waveforms

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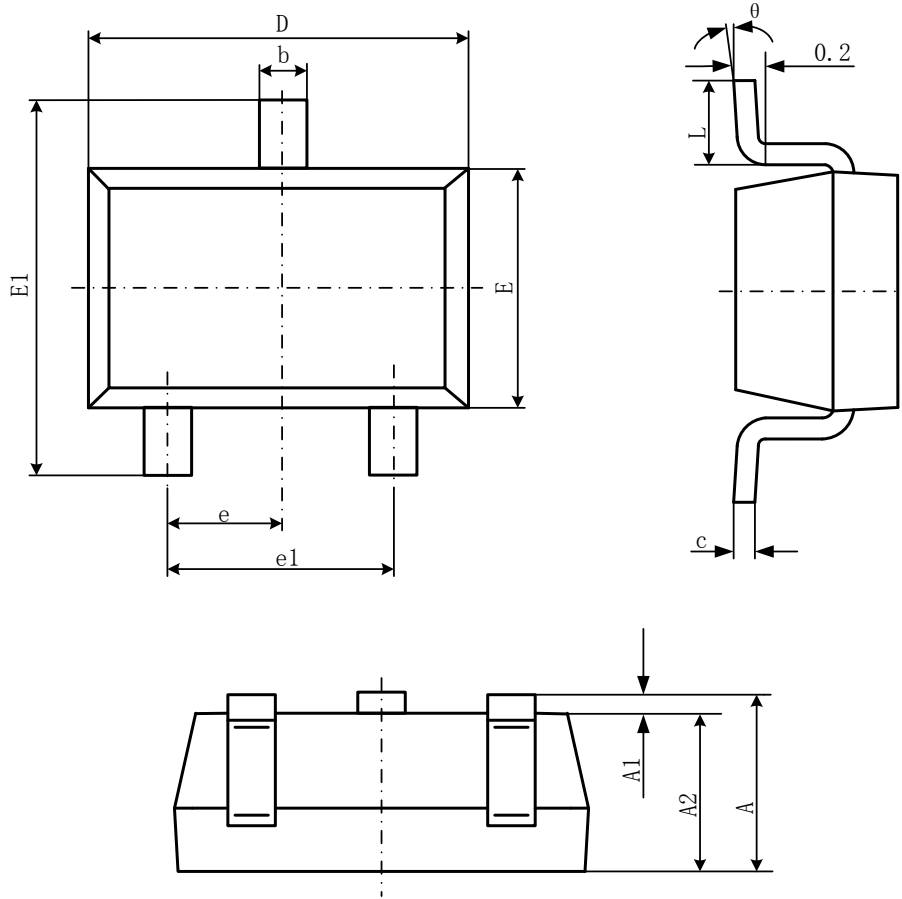


Diode Recovery Test Circuit & Waveforms



**Package Information**

- SOT-23-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°