Overview

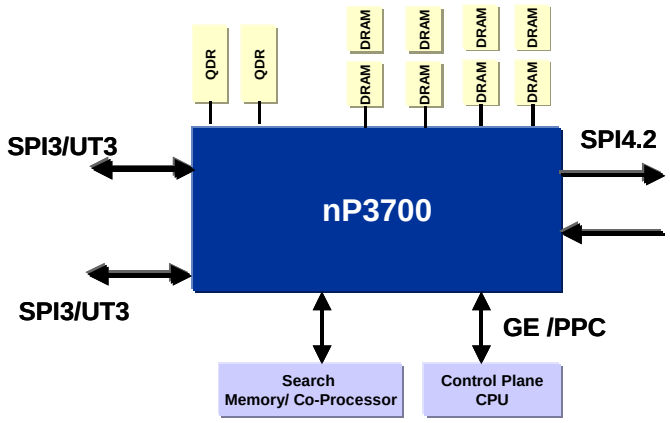
The nP3700 family of integrated network processors from AMCC are the first to incorporate the latest nP^{5}™ technology. Developed over several generations of traffic management and network processor products, nP^{5} unites the flexibility of the industry's highest performance network processing nPcore with the most widely deployed and mature traffic management technology. This unique combination enables developers to deliver extremely fine-grained control of subscriber traffic, without impacting the ability to perform complex protocol inter-working at media speeds. The nP3700 family is designed from the ground up to provide software compatibility with the earlier generations of AMCC Network Processors. The single-stage programming model dramatically simplifies software development and troubleshooting and enables quickest time-to-market.

Industry Leading Integration and Performance

The nP3700 is a 5-Gbps network processing and traffic management solution – the highest performance integrated solution in the industry. In addition to high-performance packet processing and fine-grained traffic management, the nP3700 includes specialized coprocessors that perform classification, policing, and coherent database management for unparalleled line-rate performance. The nP3700 supports high-performance memory interfaces such as RLDRAM II, DDR DRAM, and DDR SRAM. The devices are offered in different speed grades to provide a range of performance and cost options tuned to the application.

Rapid Application Development

AMCC's nPsoft™ development environment speeds the development, debugging, and delivery of feature-rich, wire-speed, Layer 2-7 applications by combining the simplified nPcore™ programming model of all AMCC NPUs with open, layered nPsoft Services, advanced development tools, rich reference application libraries, and both simulation and real hardware-based development systems. Because the nP3700 allows easy API access to on-chip coprocessors for complex tasks, customer differentiating features can be created faster and with fewer lines of code.



nP3700 Interface Diagram

– At a Glance –

Features

Supports 5-Gbps Traffic

- nP^{5} Technology
- Mix and match Gigabit Ethernet, POS, and ATM traffic
- Standalone or as a line card in a larger system

Proven nPcore Architecture

- 3 nPcores at 700 MHz optimized for network processing
- Single-stage single-image programming model
- High-speed RLDRAM-II, DDR-II memory interfaces for payload and context storage
- Per-flow metering and statistics for millions of flows

Integrated Traffic Manager

- Per-flow queuing and scheduling
- Sophisticated, fine-grained scheduling algorithms

Standards-Compliant Interfaces

- Integrated GE MACs (GMII)
- OIF SPI-3, OIF SPI-4 Phase 2

Applications

- Multi-Service Switches
- Core, Edge Routers, DSLAMs
- OC-48 AAL5 SAR
- L4-L7 Applications

Benefits

- High integration: Significant form factor, cost, and power savings
- Hardware-based Traffic Manager for guaranteed performance
- Software compatibility with previous generation nP devices: nP34xx, nP7250
- Simple programming model for rapid development and quick time-to-market
- Software portability
- ATM and packet internetworking for multi-service applications

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nP3700 Family Highlights

Interfaces

- Line Interfaces – cell and packet

	SPI-3	GE	SPI-4.2
nP3700	2	1	1

- Support for Deep Channelization: for OC-1s, T3/E3s, T1/E1s, etc.
- Fabric Interface: OIF SPI-4 Phase 2
  - 800 MHz
- External Memory Interfaces: RLDRAM II memory controllers
  - Payload Memory – 2 banks of 36-bit RLDRAM II or DDR SDRAM operating at up to 250 MHz (32 Gbps with ECC)
  - Context Memory: 2 banks of 36-bit RLDRAM II or DDR SRAM operating at up to 250 MHz (32 Gbps with ECC)
  - Channel Service Memory: One bank of 36-bit QDR-II SRAM operating at up to 250 MHz
  - Flow Database Memory: Two banks of 18-bit QDR-II SRAM operating at up to 250 MHz
- CPU Interfaces: PowerPC and Gigabit Ethernet
- External Search Interface
  - Compliant with NPF
  - Backward compatibility mode with existing TCAMs
- Debug port
- JTAG port

High Performance nPcores

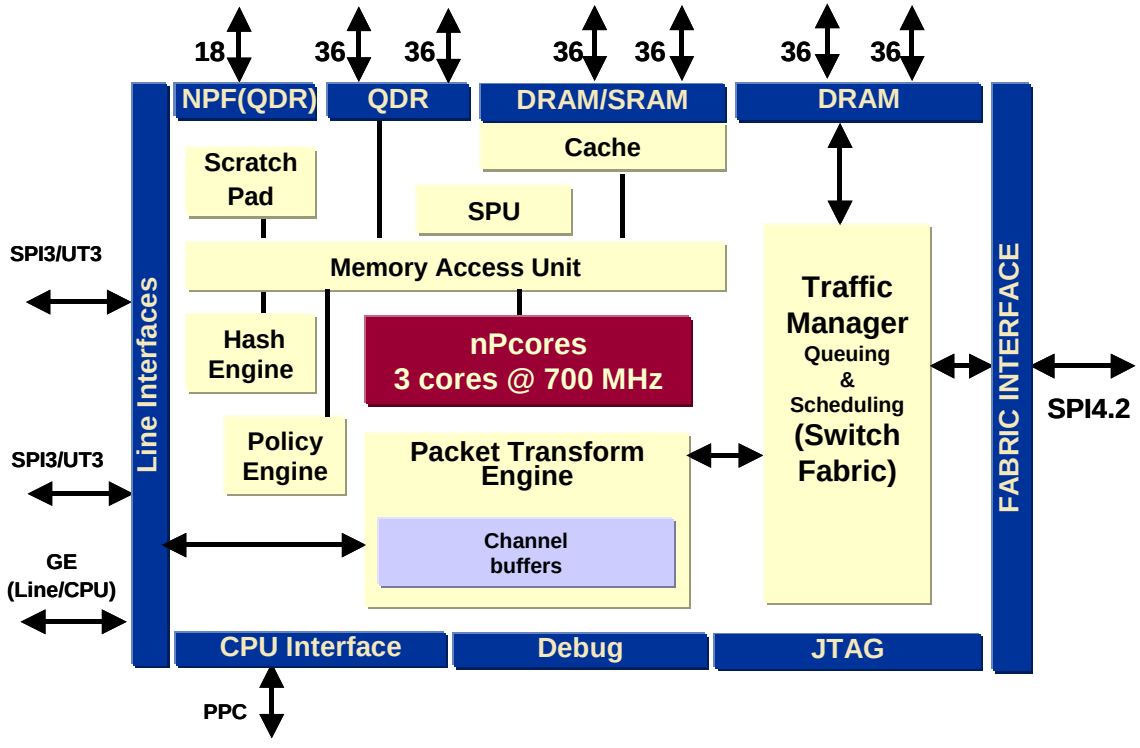
- 3 nPCores at 700 MHz

Integrated Coprocessors

- Policy Engine for efficient packet classification
- Special Purpose Unit (SPU) for per-flow policing
- Hashing Unit
- On-Chip Debugger (OCD)

Integrated Traffic Manager

- Hierarchical Traffic Manager with fine-grained flow-based traffic management
- Leverages field-proven nPX5710 and nPX5720 technology



nP3700 Block Diagram

nPcore Architecture

AMCC's software programmable nPcores are built from the ground up for both packet- and cell-based networking data-plane operations. The nP3700 supports 5-Gbps full-duplex operation utilizing a cluster of three nPcores. Each nPcore has 24 separate tasks, yielding a total of 72, which are all available for either ingress or egress processing. The nPcores implement zero-cycle task switching and zero-cycle branching for enhanced performance.

The nPcores are surrounded by on-chip coprocessing engines to accelerate sophisticated network processing functions, such as packet classification, route and context searching, statistics gathering, metering, policing, and packet transformations. The nPcores, in combination with these on-chip coprocessing engines, implement Network Instruction Set Computing (NISC) Architecture. This NISC architecture dramatically reduces the number of lines of code required to implement many advanced networking tasks. A key addition to the fifth generation of NISC architecture is the exception channel processing that provides flexibility in handling packets that require increased processing time. This exception channel handles special packets through a secondary path, without affecting the deterministic line-rate performance of the regular packets in the primary path. Another key addition to the fifth generation architecture is the Channel Service Memory that enables deep channelization in the line interfaces at all packet sizes and can handle very large bursts in the incoming traffic without affecting line rate performance.

Single-Stage, Single-Image Programming

AMCC's nPcore architecture implements a simple single-stage programming model. In this model each cell or packet is processed in its entirety, from start to finish, by a single task in a single nPcore. With this single-stage model, the entire data flow algorithm can be created as a single complete software program, just as it would be on a non-multiprocessor system, allowing the same program image to be executed identically by each task on each nPcore. This approach greatly simplifies programming while optimizing performance.

Traffic Management

The traffic management block in the nP3700 leverages AMCC's expertise and technology from the nPX5700 family of traffic managers.

The nP3700 family implements a hierarchical scheduling architecture to provide multiple levels of bandwidth provisioning and per-subscriber guarantees. This hierarchy consists of four logical levels: flow, pipe, subport and port. Minimum and maximum bandwidth control can be configured on multiple levels. WFQ and Strict Priority scheduling algorithms are also implemented by the traffic management block. For ATM applications, non-real-time and real-time CBR and VBR connections can be configured for a desired subset of flows.

Input Admission Control

Sophisticated cell and packet admission controls are configurable in the nP3700. This includes execution of standard discard mechanisms such as WRED, EPD, and TPD in hardware or the option to perform variations in software.

MISSION™ — Multi-Service Internetworking Solution

The nP3700, combined with AMCC's Evros (S1208) and Tigris (S4811) chips, provides a cost-effective and highly flexible multi-service solution. This solution, called MISSION, combines state-of-the-art framer, HDLC, and flexible nP^5 technology with modular internetworking software, enabling the development of single multiprotocol solutions in place of multiple single-protocol solutions. The MISSION architecture provides equipment vendors with solutions that enable their customers to save on both capital and operational expenditures (CapEx/OpEx).

MISSION Software

At the core of the MISSION value proposition is software that implements a wide variety of protocols on the chip set and enables flexible potential additions to these base software features. AMCC provides integrated drivers for Evros, Tigris, and nP3700, and extensive offerings for the programmable nP3700 Integrated Network Processors, including both rich off-the-shelf application software and a complete development environment for extending this application base if desired.

The MISSION application software includes ready-to-use Multi-Service Switching software – ATM UNI/NNI, Inverse Multiplexing over ATM (IMA), Multi-Link Frame Relay (ML-FR), Multi-Link PPP (ML-PPP), Frame Relay Interworking (FRIWF) and MPLS Martini encapsulation – as well as OEM customer-extensible libraries for the hardware-resident aspects of higher layer applications such as IPv4 and IPv6 routing, and Layer 2 packet switching.

Specifications

Network Processing

Configurations

- POS and ATM
  - 2xSPI-3, SPI-4.2
  - Any type of OC-*n* channelization
  - Flexible bandwidth allocation
    For example, Full-duplex OC-48, OC-12 plus 12xOC-3
- Ethernet
  - 10/100/1000 Ethernet Interface for Line or Host CPU
- Can mix Ethernet ports and SPI-3 ports
  For example, OC-48c and Gigabit Ethernet
- Deep Channelization
  - Allows fractional T3/E3 and T1/E1 logical channels
  - Can receive interleaved chunks of jumbo packets, perform packet processing on each chunk separately, and reassemble a jumbo packet in the fabric.

nPcore Performance

- 3 nPcores running at 700 MHz
- 24 tasks per nPcore, total 72 tasks
- 64 KB instruction space, 16K instructions
- Dynamic Task Allocation
- Zero Cycle Task Switching

Integrated Co-Processors

- Policy Engine — Efficient packet classification
- SPU — Data coherency
  - Enables Single and Dual Leaky Bucket and Token Bucket policing on cells and frames
- Hash Engine — Programmable engine to accelerate table lookups
  - Programmable Polynomial (for example, CRC generation)
- Statistics Engine
  - Programmable Statistics Collection

Traffic Management

- Standard Discard Mechanisms
  - WRED
  - Dynamic queue limits
  - EPD and CLP marking
- Payload memory requirements
  - Up to 2 million cells of storage
  - RLDRAM II or DDR SDRAM
- Supports DiffServ
- Per-flow queuing and scheduling
  - 128K ingress and egress flows
    - Strict Priority, Min, WRR
    - Rate-shaping (CBR, VBR)
  - 4K pipes
    - Strict Priority, Min, Weight, Max
  - 512 subports
    - Min, Max, WRR

nPsoft Development Environment

nPsoft Services
- Simplified multiprocessor programming model
- Powerful NPU and CPU software and messaging framework
- nPkernel NPU operating system
- Open APIs, tracking standards

nP Workbench
- Software development system
- Modular interfaces

nPsoft Application Libraries
- Reference source code for WAN and LAN protocols

nPsoft Toolkit
- Code development tools
- Graphical simulators
- Customizable debugger
- Performance analysis

Product Availability

- Samples Q1 ‘04
- Commercial and Industrial Temperature Rating

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