DATA SHEET

NEC

COLOR PLASMA DISPLAY MODULE

NP4201MF02

CosmoPlasma

106 cm (42-inch), Wide Screen (853 × 480 Pixels), Digital Module

Digital RGB signal, 8-bit signal e ch

DESCRIPTION

The NP4201MF02 is a 42-inch wide color plasma display module with a resolution of 853(H) × 480(V) pixels. The display offers vibrant colors we reproduced in a thin and low profile package. This device uses AC plasma technology by NEC and includes an 8-bit digital interface.

FEATURES

- Applied Capsulated Color Filter (CCF) technology, developed at NEC, which offers a high quality image match for CRT display. To offer remarkably pure colors, the color plasma display panel uses extremely clear, thin capsulated color filters to cut unnecessary light as the plasma discharges.
- Contrast ratio of 350:1 is achieved through a new driving method, which offers improved black levels instead of toning down the white light emitted.
- Applied Peak Luminance Enhancement (PLE) function which enable the display to operate with the ideal contrast. The PLE function makes it possible to adjust the average brightness level of the PDP display automatically in accordance with the average brightness level of an input video signal.

APPLICATIONS

- Wide Screen TV (aspect ratio 16:9)
- Public Information Display
- Video Conference Systems
- Retail
- Education and Training Systems

The information in this document is subject to change without notice.

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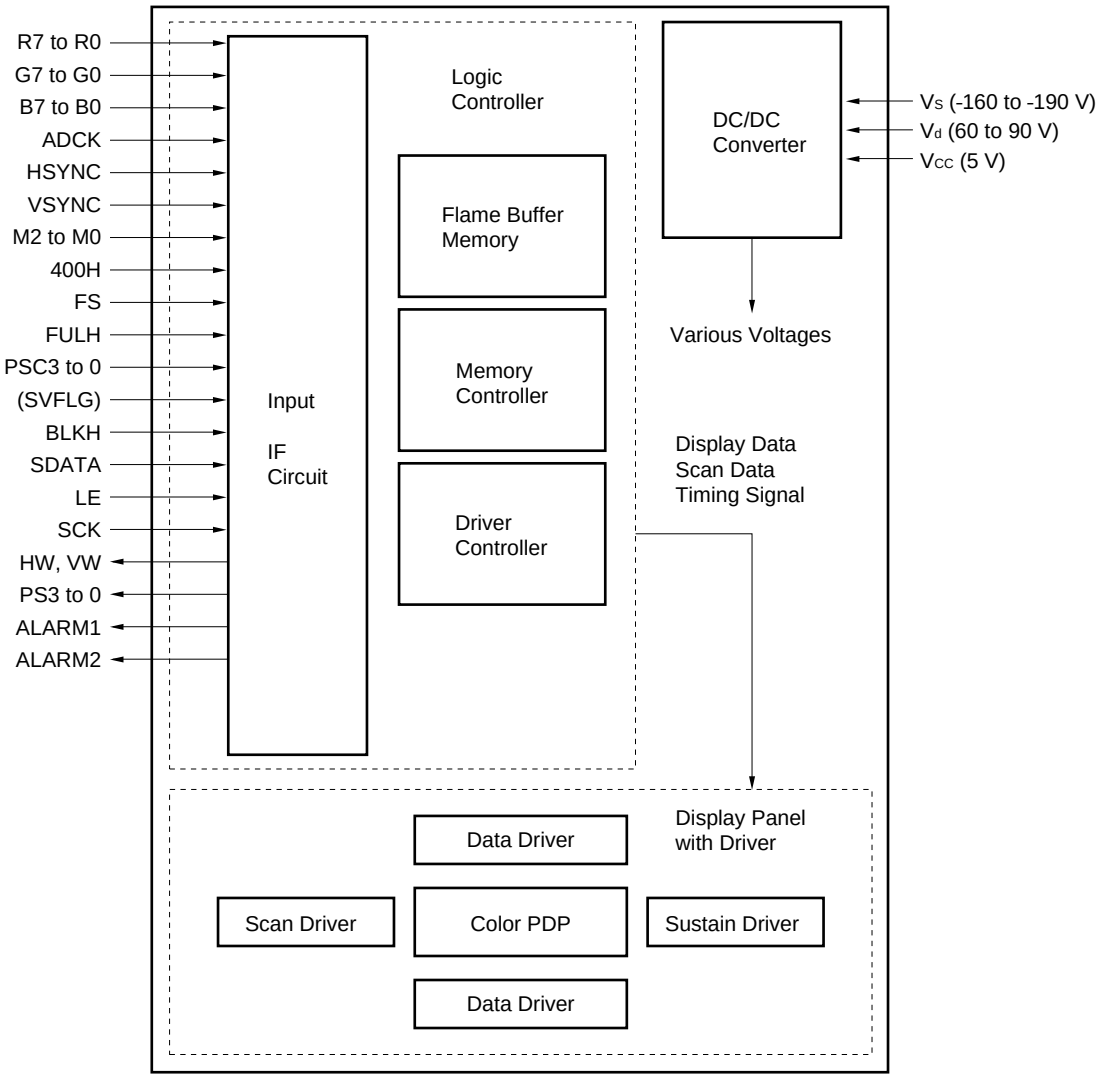
STRUCTURE AND PRINCIPLE OPERATION OF PLASMA DISPLAY

In a Plasma Display Panel, Row and Column electrodes are placed between two glass substrates. A rare gas is then filled between each substrate. When a high voltage is applied to these electrodes, the gas is activated resulting in the radiation of ultraviolet light, similar to the operation in fluorescent lamps. These ultraviolet rays then activate phosphor that has been coated on the inside of the glass substrate, and visible light is emitted from the panel.

ELECTRICAL INTERFACE OF PLASMA DISPLAY

NP4201MF02 requires 8 bits of digital video signals for each RGB color. In addition to the video signals, 12 kinds of digital control signals and 3 different DC voltages are required to operate the display. In addition, four digital signals outputs and four digital inputs are provided for a “PLE” (Peak Luminance Enhancement) function so that images can be displayed with the ideal contrast.

BASIC CONFIGURATION



Note SVFLG is used for NEC internal test mode.

GENERAL SPECIFICATION

Display area	921(H) × 518(V) mm
Outline dimensions	987(W) × 584.5(H) × 60(D) mm
Weight	19 kg
Aspect ratio	16:9
Number of pixels	853(H) × 480(V) (1 pixel = 3 RGB cells)
Pixel pitch	1.08(H) × 1.08(V) mm
Color arrangement	RGB vertical stripes
Number of gradations	176 steps for video mode 256 steps for PC mode
Peak brightness	250 cd/m^2 (typ.) (VGA signal*****, 1/25 white window, PLE****** mode set to the maximum)
Contrast ratio	350:1 (typ.) (VGA signal*****, 1/25 white window, PLE****** mode set to the maximum, measured in darkroom)
Viewing angle	160 degrees (typ.) vertical and horizontal directions (angle at which brightness becomes 1/2 of front view brightness)

***** Signal of fv = 59.94 Hz and fh = 31.47 kHz

****** See PLE (Peak Luminance Enhancement) description

OPERATION ENVIRONMENTAL CONDITIONS

Temperature	0 to 50°C (with forced-air cooling)
Humidity	20 to 80% RH (without condensation)
Atmospheric pressure	800 to 1100 hPa

STRAGE ENVIRONMENTAL CONDITIONS

Temperature	-20 to 60°C
Humidity	10 to 90% RH (without condensation)
Atmospheric pressure	700 to 1100 hPa

MECHANICAL TEST CONDITIONS

Vibration (operating)	0.5 G, 10 to 100 Hz, 3 directions, 10 minutes each
Vibration (non-operating)	0.5 G, 10 to 100 Hz, 3 directions, 2 hours each

LIFE EXPECTANCY

More than 10,000 hours of continuous operations

(Time when the brightness decreased to half to the initial)

ELECTRICAL CHARACTERISTICS

1) Interface Signals; Absolute Ratings

Common conditions: Ta = 25°C, V_{CC} = 5 V

Table 1. Absolute Ratings

Item		Parameter	Symbol	Ratings	Units
Input signals	R7 to R0, G7 to G0, B7 to B0, ADCK, HSYNC, VSYNC, M2 to M0, 400H, FS, FULH, PSC3 to PSC0, BLKH, LE, SCK, SDATA	Input Voltage	Vi	-1.5 to 6.5	V
		Input Current	Ii	±20	mA
Output Signals	HW, VW, PS3 to PS0	Output Voltage	Vo	-0.5 to 5.5	V
		Output Current	Io	±35	mA
	ALARM1, ALARM2	Output Voltage	Vo	-0.5 to 5.5	V
		Output Current	Io	±25	mA

2) Interface Signals; Electrical Characteristics

Common conditions: Ta = 25 °C, V_{CC} = 5 V

Table 2. Electrical Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High Level Input Voltage	V_{IH}	–	2.0	–	–	V
Low Level Input Voltage	V_{IL}	–	–	–	0.8	V
Input Current	I_i	V_i = V_{CC} or GND	–	–	±60	μA
High Level Output Voltage*	V_{OH}	I_O = 20 μA	4.4	–	–	V
Low Level Output Voltage*	V_{OL}	I_O = 20 μA	–	–	0.2	V

SIGNAL FUNCTION

Table 3. Interface Signal Function

Symbol	I/O	Function	(Remarks)
R7 to R0	I	8 bits red video signal[Note 1]	(R7: MSB, R0: LSB)
G7 to G0	I	8 bits green video signal[Note 1]	(G7: MSB, G0: LSB)
B7 to B0	I	8 bits blue video signal[Note 1]	(B7: MSB, B0: LSB)
ADCK	I	Clock signal which synchronizes to video signal	(positive edge)
HSYNC	I	Horizontal synchronous signal tw = 4 T_{ADCK} min	(negative pulse)
VSYNC	I	Vertical synchronous signal tw = 200 ns min.	(negative pulse)
M2 to M0	I	Video mode selection	(refer to the following list)
400H	I	Mode signal	(refer to the following list)
FS	I	Function selection[Note 2]	("L" in normal display mode)
FULH	I	Switch for "Full display mode" and "Normal display mode"	("H" in full display mode)
PSC3 to PSC0	I	4 bits PLE control signal (16 steps)	(PSC3: MSB, PSC0: LSB)
SVFLG	I	NEC internal test function mode	("L" in normal display mode)
BLKH	I	Video blanking and muting[Note 3]	("H" in muting)
SDATA	I	Serial data for display position adjustment	(total 16 bit: V-7 bit, H-9 bit)
LE	I	SDATA latch enable	(negative logic)
SCK	I	SDATA clock	(latch in positive edge)
PS3 to PS0	O	4 bits average brightness level signal (16 steps)	(PS3: MSB, PS0: LSB)
HW	O	H window display period indication signal	("H" in display period)
VW	O	V window display period indication signal	("H" in display period)
ALARM1	O	Alarm signal for panel broken and failure of internal power-source.[Note 4]	("L" in alarmed status)
ALARM2	O		

MSB : Most Significant Bit
LSB : Least Significant Bit

Notes 1. The RGB video signal should be compensated with Inverse γ circuit before input to the color plasma display module.

2. In case of normal display mode (aspect ratio = 4:3), gray level in right and left sides of no display areas can be set with M2-M0 (3 bits) data (While FS = "H" level, gray level is read into the module by VSYNC pulse).

3. When BLKH input is "H" level, all RGB data is read as "L" level (black color data).

4. When ALARM output turns to "L" level, high voltage power input (Sustain power supply: Vs, and Data power supply: Vd) should be switched off immediately. When glass panel is broken, high voltage may occur at the electrode section and cause electric shock. Failure of internal power-source cause over-power status and gives damage to the display panel and driver-circuits.

VIDEO SIGNAL INPUT AND SIGNAL TIMING

Table 4. Relation Between Input Video Signal and Module RGB Signal Input

	Video Signal						RGB Signal														
							Normal Display Mode (Aspect Ratio 4:3)									Full Display Mode (Aspect Ratio 16:9)						
	No.	Signal Name	Display Resolution (dot · line)	Vert Freq. (Hz)	Number of Lines In one Frame	Horiz. Freq. (kHz)	Recommended ratio between dot-clock freq. and horiz. freq. (Horiz. freq. : MHz)	Nominal data read start timing after sync. signal		Mode Signal						Recommended ratio between dot-clock freq. and horiz. freq. (Horiz. freq. : MHz)	Nominal data read start timing after sync. signal		Mode Signal				
								Dv	Dh	400H	FULH	M2	M1	M0			Dv	Dh	400H	FULH	M2	M1	M0
Vide mode	1	EUTV1	853 · 480	50.0	525	26.25	780 (20.48)	39	171	H	L	L	L	L	1040 (27.30)	39	228	H	H	L	L	L
	2	EUTV2	853 · 480	50.0	625	31.25	780 (24.38)	46	171	H	L	H	H	H	1040 (32.50)	46	228	H	H	H	H	H
	3	EDTV	853 · 480	59.94	525	31.47	780 (24.55)	35	116	L	L	L	L	L	1040 (32.73)	35	154	L	H	L	L	L
	4	HDTV	853 · 480	60	1125/2	33.75									1054 (35.57)	40	113	L	H	L	L	H
PC mode	5	NEC	640 · 400	56.4	440	24.83	848 (21.05)	33	149	H	L	L	H	L	1130 (28.06)	33	199	H	H	L	H	L
	6	NEC	640 · 400	70	449	31.47	800 (25.18)	36	143	H	L	L	H	H	1066 (33.55)	36	191	H	H	L	H	H
	7	IBM	640 · 400	70	449	31.47	800 (25.18)	36	146	H	L	L	H	H	1066 (33.55)	36	195	H	H	L	H	H
	8	VGA	640 · 480	59.94	525	31.47	800 (25.18)	35	144	L	L	L	H	H	1066 (33.55)	35	192	L	H	L	H	H
	9	IBM	640 · 480	59.94	525	31.47	800 (25.18)	27	136	L	L	L	H	H	1066 (33.55)	27	181	L	H	L	H	H
	10	NEC	640 · 480	59.94	525	31.47	800 (25.18)	39	145	L	L	L	H	H	1066 (33.55)	39	193	L	H	L	H	H
	11	MAC	640 · 480	66.66	525	35.00	864 (30.24)	42	160	L	L	H	L	L	1152 (40.32)	42	213	L	H	H	L	L
	12	VESA	640 · 480	72.8	520	37.86	832 (31.5)	31	168	L	L	H	L	H	1109 (42.00)	31	224	L	H	H	L	H
	13	VESA	640 · 480	75	500	37.5	840 (31.5)	19	184	L	L	H	H	L	1120 (42.00)	19	245	L	H	H	H	L
	14	IBM	640 · 480	75	525	39.38	800 (31.5)	34	144	L	L	H	H	L	1067 (42.00)	34	192	L	H	H	H	L

Notes 1. Frequency ranges of HSYNC signal in EUTV1 and EUTV 2 are as follows.
EUTV1: F-HSYNC < 28.9 kHz
EUTV2: F-HSYNC > 28.9 kHz

2. Maximum data clock (ADCK) frequency in MAC, VESA and IBM Full Display mode is 44 MHz.

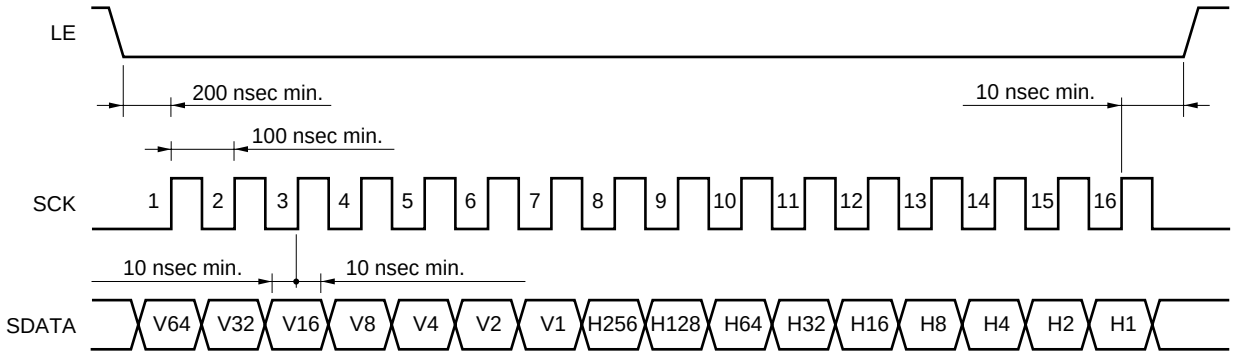
SIGNAL TIMING

Refer to the timing diagram on the following pages.

- Input video signal format is determined by Mode signal (refer to Table 4)
- "T_{ADCK}" shows 1 cycle period of ADCK.
- "t_{vs}" shows negative pulse width of VSYNC.
- "t_{hs}" shows negative pulse width of HSYNC.
- "1H" shows 1 cycle period of HSYNC (Horizontal Synchronous Signal).
- "1V" shows 1 cycle period of VSYNC (Vertical Synchronous Signal).
- "Dv" is a period between "leading-edge of the vertical synchronous pulse" and "valid RGB lines data read start timing"
- "Dh" is a period between "leading-edge of the horizontal synchronous pulse" and "valid RGB dots data read start timing"
- In case normal mode (640 dot mode) is selected, both sides are masked with gray patterns.
- In case 400 line is selected, upper 40 lines and lower 40 lines are masked with gray patterns.

SET-UP OF DISPLAY POSITION

Display start position is set by the value of Dv and Dh.



Dv can be set from 1 to 127 lines by V64 to V1 of 7 bits signal.

Dh can be set from 1 to 511 dots by H256 to H1 of 9 bits signal.

When Dv and Dh are set to the “Nominal data read start timing after sync. signal”, in Table 4, a picture is displayed on the center of the panel.

Note In 400 line mode and normal display mode, overlapped part of picture with blank area is not displayed.

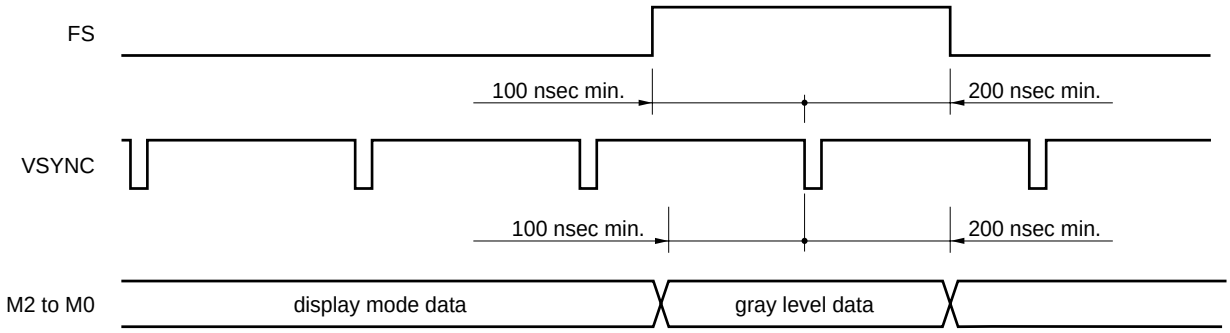
Set-up Sequence

1. Set LE to “L” level.
2. Put the display start position data into SDATA input, and latch into the module at the rising edge of SCK.
3. Set LE to “H” level.

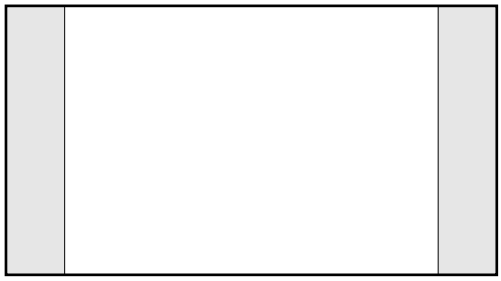
Note This display position data is kept in the module until V_{CC} is powered off.
When V_{CC} is powered on, display position should be set-up each time.

SET-UP OF GRAY LEVEL IN BLANK AREA

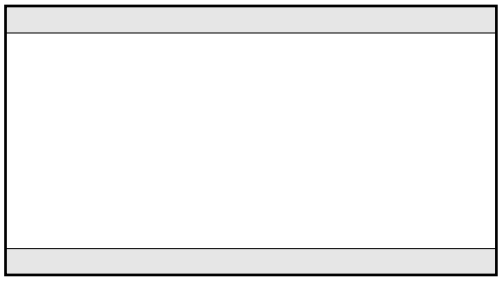
Brightness level of blank areas defined by normal mode and/or 400 line display mode can be set by M0-M2 signals with 8 steps of gray colors.



Blank Area



Left and right area
In normal display mode



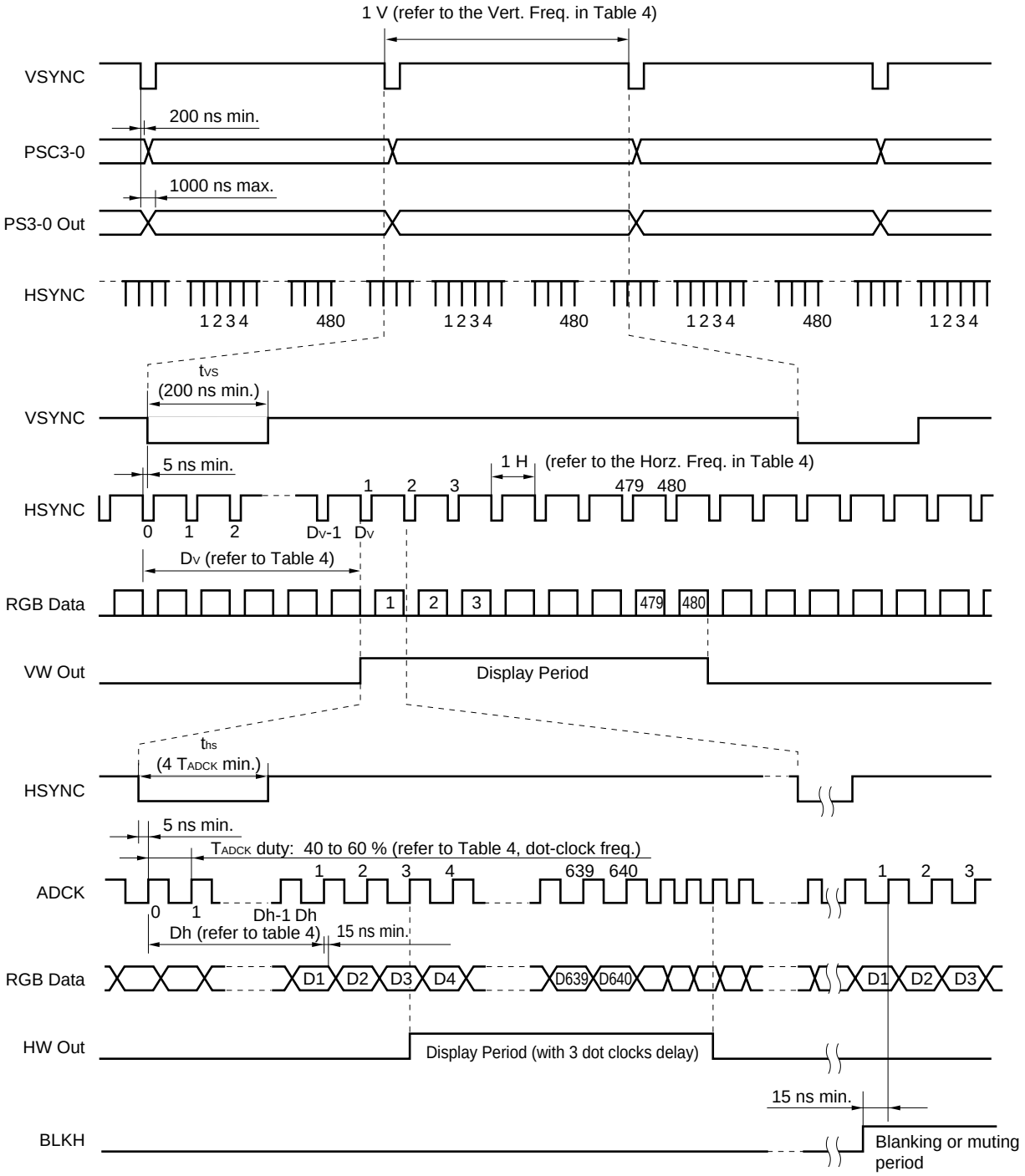
Upper and lower area
in 400 line display mode

Gray Level

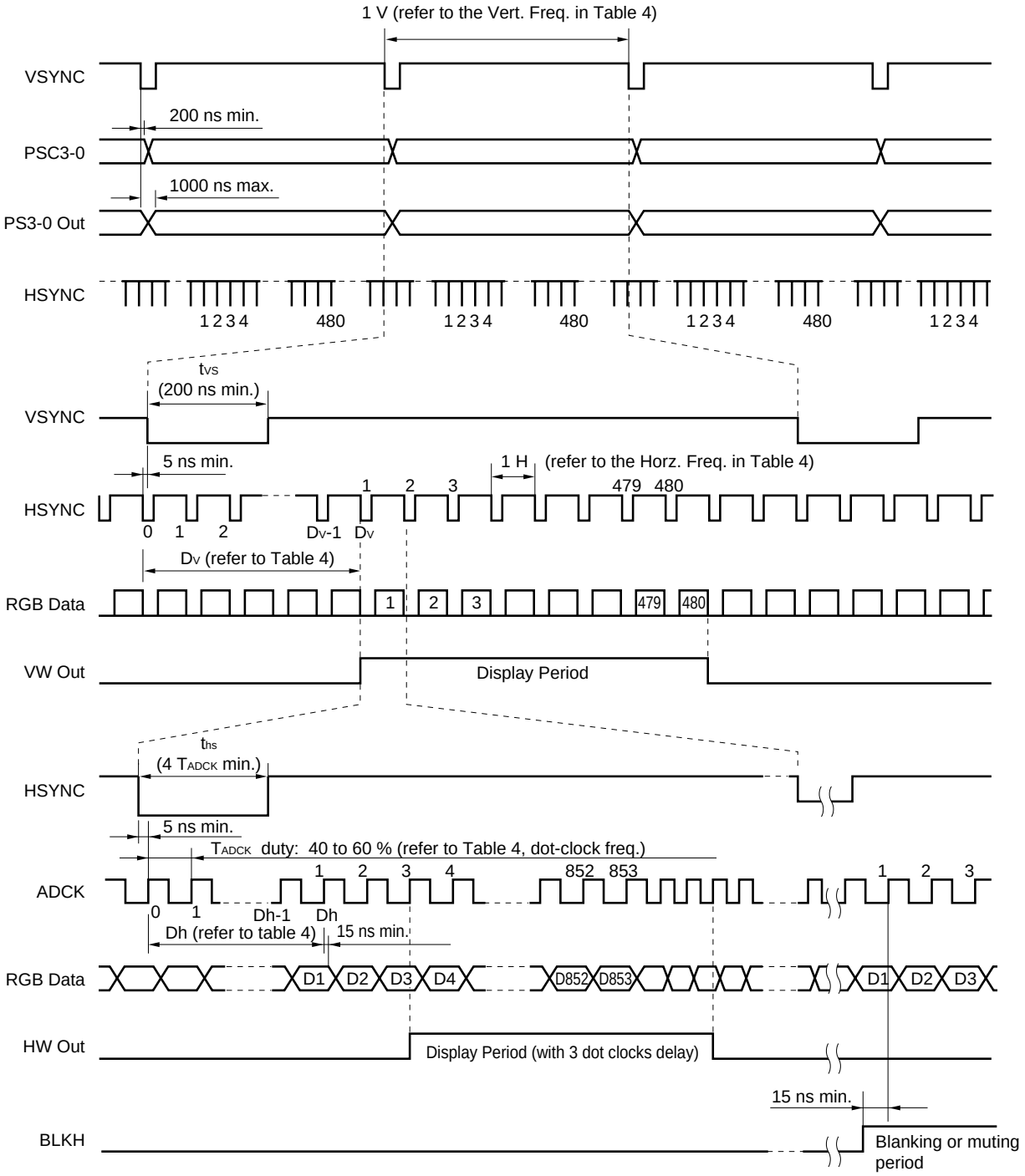
	M2	M1	M0	Brightness (white: 100 %)	
				Video Mode	PC Mode
BLACK	L	L	L	0	0
(darker)	L	L	H	2	1.5
↕	L	H	L	5	3
	L	H	H	9	6
	H	L	L	18	12
	H	L	H	23	16
	H	H	L	27	19
(brighter)	H	H	H	27	25

Note This gray level data is kept in the module until V_{CC} is powered-off.
When V_{CC} is powered on, gray level data should be set-up each time.

Timing Diagram (Normal Display Mode, 480 lines)



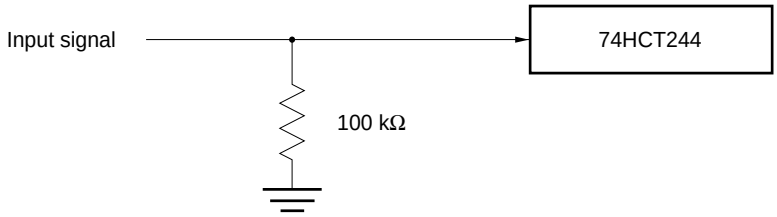
Timing Diagram (Full Display Mode, 480 Lines)



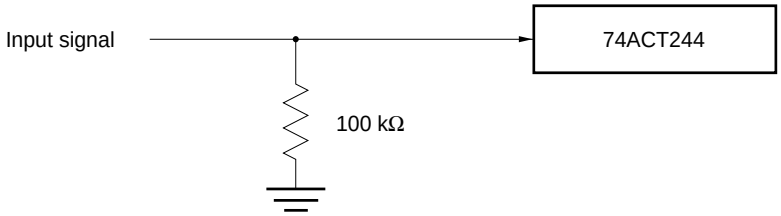
INPUT OUTPUT DRIVE CIRCUIT

Following are definitions of the input and output drive circuits for all interface signals and the PDP module.

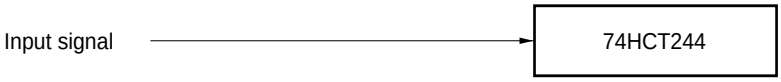
1) R7-R0, G7-G0, B7-B0, M2-M0, 400H



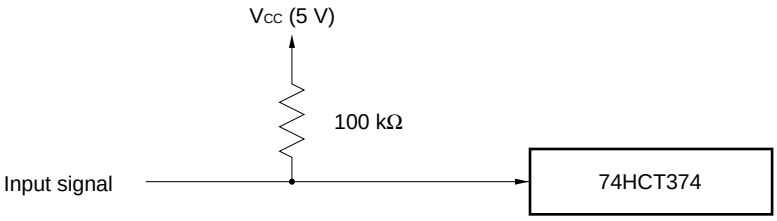
2) ADCK, HSYNC, VSYNC, FS, FULH, BLKH, LE, (SVFLG)



3) SCK, SDATA



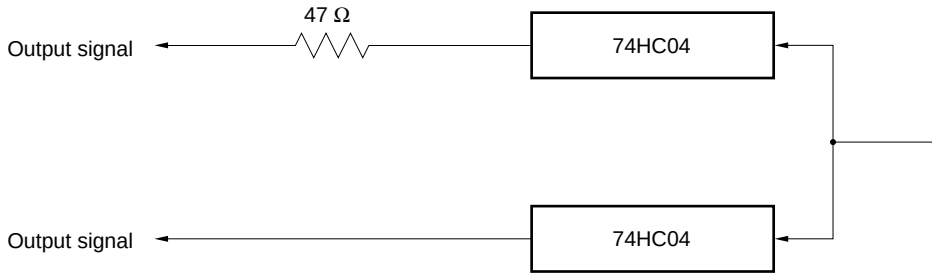
4) PSC3-PSC0



5) HW, VW, PS3-PS0

6) ALARM1

7) ALARM2



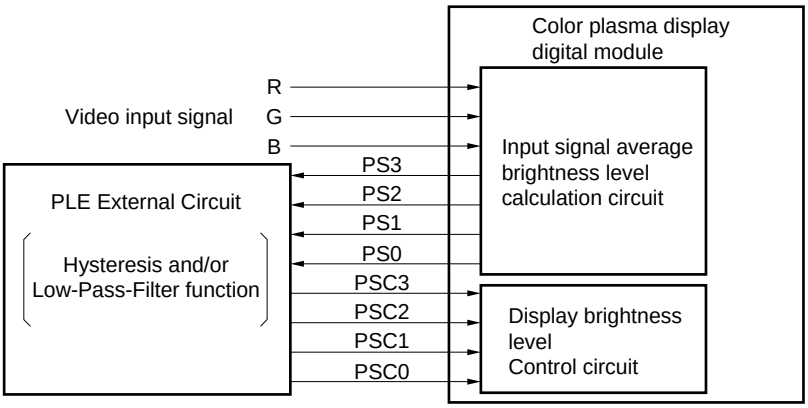
PLE (Peak Luminance Enhancement) FUNCTION

1) Basic function of PLE

The PLE function makes it possible to increase or decrease the average brightness level of the PDP display when the typical brightness level of the input video signal is lower or higher than the average brightness of the previous frame. This PLE function control reduces power consumption and results in a higher contrast level. External circuitry is required to take advantage of the PLE function.

The PLE control circuits can be constructed by connecting external hysteresis and/or low-pass filter circuits (PLE external circuit) between PSC3-0 (PLE control signal input) and PS3-0 (PLE control signal output).

The PLE brightness change response characteristic depends on the characteristics of the PLE external circuit.



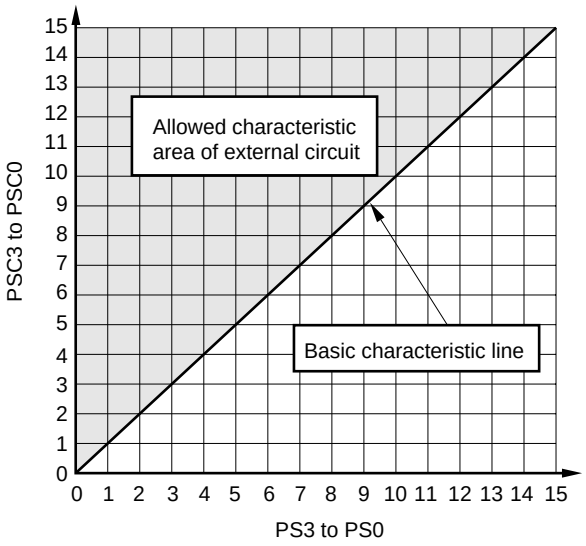
2) Characteristic of PLE external circuit

This digital module is designed subject to use PLE function, and input signal (PSC3-PSC0) should vary linearly to the output signal (PS3-PS0). (A short time of delayed response is allowed).

Right figure shows the basic characteristic line for module design and allowed characteristic area of the external circuit.

If PLE function is not used, PSC3-PSC0 inputs should be set to “H” level or be kept open. In this case the brightness level is set to a minimum level.

PS3-PS0 output signals are refreshed in every frame.



3) PLE response characteristic and variance of brightness and display (sustain) current

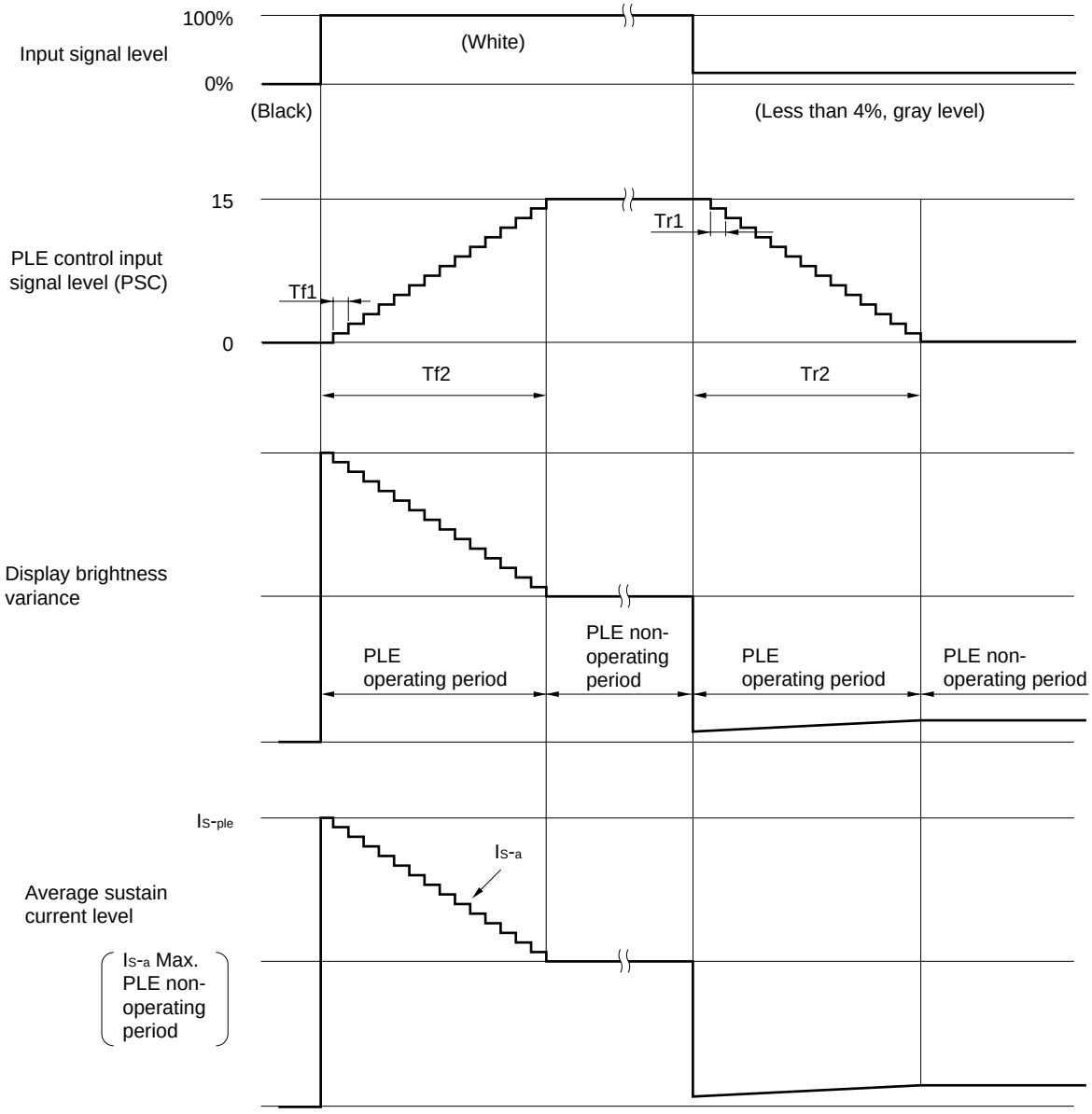
PLE response time is depend on the external circuit (Hysteresis and/or Low-Pass-Filter) which is connected to the module.

Generally these kind of external circuit have delayed response, and this delayed response occasionally make the module to flow large current while response period.

In order to avoid over power status, the PLE response is specified as follows.

Item	Symbol	Min.	Max.	Recommendation	Unit
1 step decrement time	Tf1	0	5	0.2 to 0.5	Sec
All steps decrement time	Tf2	0	75	3 to 7.5	Sec
1 step increment time	Tr1	0	----	0.2 to 0.5	Sec
All steps increment time	Tr2	0	----	3 to 7.5	Sec

Condition: Input signal jumps up and down with following sequence.



POWER INPUT AND OUTPUT

1) Sustain Power Supply

Table 5. Power Output

Item	Symbol	Condition and Remarks	Min.	Typ.	Max.	Unit
Absolute Maximum	----	--------	----	----	–200	V
Voltage	Vs	Dependent on the characteristics of each PDP[Note]	–160	----	–190	V
Voltage Stability	----	--------	----	----	±1.0	%
Average Current	Is-a	At PLE non-operation period	0.1	----	2.0	A
Maximum Average Current at PLE Operation	Is-ple	White input signal input and PSC3-0 = 0000	2.8	3.4	4.0	A
Peak Current	Is-peak	--------	----	----	15	A
Voltage Regulation	----	At peak current	----	----	5	V
Ripple and Noise	----	--------	----	----	500	mVp-p

Note Voltage should be set to a specified value, which is located on a label attached to the module.

2) Data Power Supply

Table 6. Data Power Supply (Vd)

Item	Symbol	Condition and Remarks	Min.	Typ.	Max.	Unit
Absolute Maximum	----	----	----	----	100	V
Voltage	Vd	Dependent on the characteristics of each PDP[Note]	60	----	90	V
Voltage Stability	----	----	----	----	±1.5	%
Average Current	Id-a	Varied correspondence to the Image	0.005	----	1.9	A
Ripple and Noise	----	----	----	----	300	mVp-p

Note Voltage should be set to a specified value, which is located on a label attached to the module.

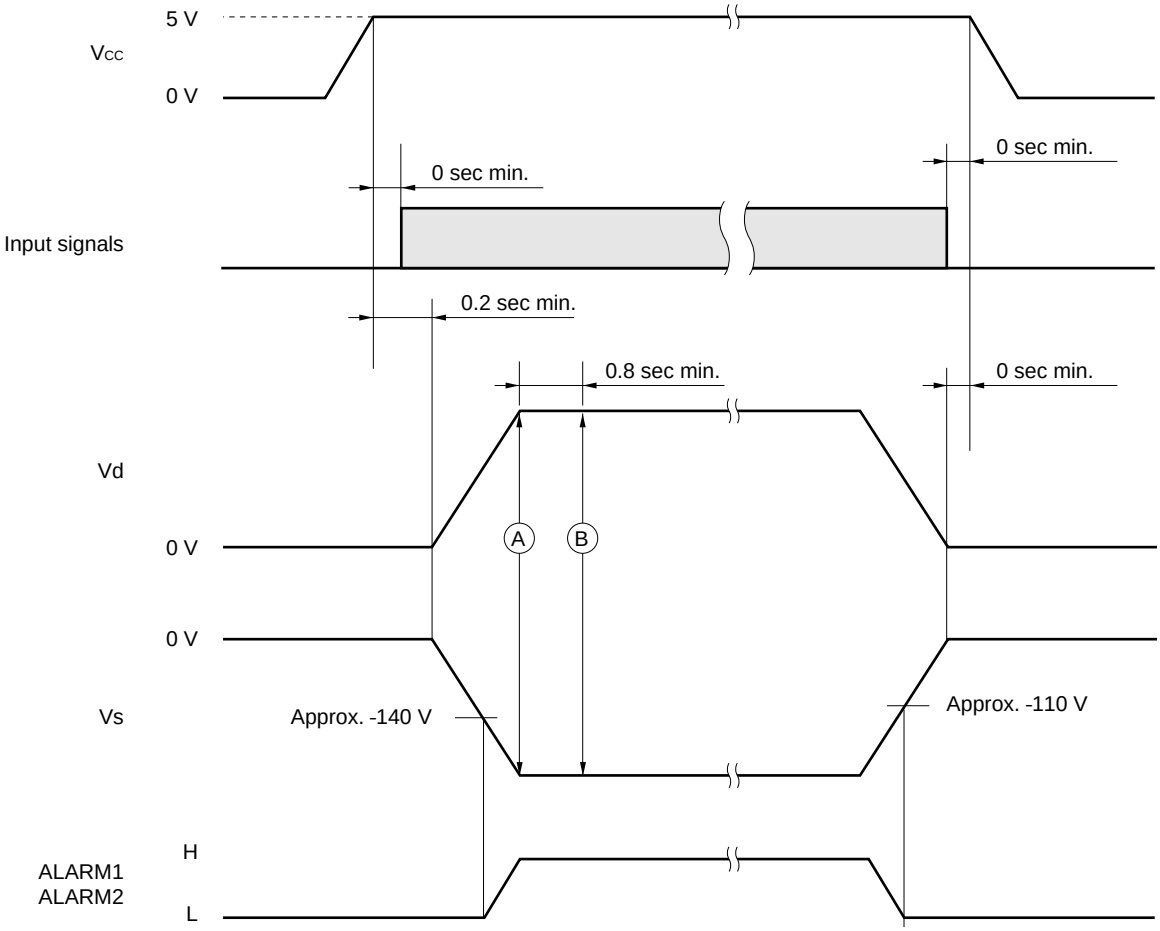
3) Logic Power Supply

Table 7. Logic Power Supply

Item	Symbol	Condition and Remarks	Min.	Typ.	Max.	Unit
Absolute Maximum	----	--------	----	----	6.00	V
Voltage Range	V_{CC}	---------	4.75	5.00	5.25	V
Current[Note]	I_{CC}	--------	2.7	4.5	6.0	A
Ripple	----	--------	----	----	30	mVp-p
Noise	----	--------	----	----	300	mVp-p

Note This module provides an automatic operation-stop function for internal malfunctions. When the module stops the operation, logic current may reduce to almost zero (0). Even if logic current becomes zero, applied voltage should be kept to less than 6.00 volts.

Supply Voltage and Signal Sequence



Notes 1. When high voltages are put into the module, a distorted image is displayed at point Ⓐ. In order to avoid this phenomenon, it is recommended to keep the RGB signal to “Black” or to keep BLKH signal to “H” (muting mode) until point Ⓑ.

2. Basically power source for Input signal circuit and Vcc can be switched on and off at the same time.

3. Sequence of Vd and Vs does not determined. It is recommended to switch on and off simultaneously.

4. When ALARM1 and ALARM2 is “L”, High voltage should be shut down. However, when Vcc is applied at first, “ALARM” signal keeps “L” until Vs is applied. In order to enable “High voltage power supply” operate, initial ALARM status “L” should be disregarded.

CONNECTORS PIN ASSIGNMENT

(for the connector position, please refer to the Rear View in the Outline Drawing)

1) SIGNAL INTERFACE CONNECTOR

Table 8. Connector CN101 Pin Assignment

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	R7	2	GND	41	B3	42	GND
3	R6	4	GND	43	B2	44	GND
5	R5	6	GND	45	B1	46	GND
7	R4	8	GND	47	B0	48	GND
9	R3	10	GND	49	ADCK	50	GND
11	R2	12	GND	51	HSYNC	52	GND
13	R1	14	GND	53	VSYNC	54	(N.C.)
15	R0	16	GND	55	M2	56	M1
17	G7	18	GND	57	M0	58	400H
19	G6	20	GND	59	FS	60	FULH
21	G5	22	GND	61	HW	62	GND
23	G4	24	GND	63	VW	64	PS3
25	G3	26	GND	65	PS2	66	PS1
27	G2	28	GND	67	PS0	68	GND
29	G1	30	GND	69	PSC3	70	PSC2
31	G0	32	GND	71	PSC1	72	PSC0
33	B7	34	GND	73	ALARM1	74	GND
35	B6	36	GND	75	SVFLG	76	BLKH
37	B5	38	GND	77	LE	78	SCK
39	B4	40	GND	79	SDATA	80	GND

(N.C.): non-connection pin

Module side connector: TX3-80P-D2ST-SN1

Mating connector : TX1-80S-D2P1-1D

Connector supplier : Japan Aviation Electronics Industry, Limited (JAE)

Fitting Cable : 80 conductors flat-cable, 0.635 mm pitch (equivalent to AWG#30)

2) POWER INPUT CONNECTORS

Table 9. Connector CN4 Pin Assignment	
Pin No.	Symbol
1	Internal use[Note]
2	Internal use[Note]
3	GND
4	ALARM2
5	GND
6	GND
7	Vd
8	(N.C.)
9	Vs
10	Vs

(N.C.): non-connection pin
Module side connector: B10P-VH
Mating connector : VHR-10N (housing)
BVH-21T-P1.1 or SVH-21T-P1.1 (contact)
Connector supplier : J.S.T TRADING COMPANY, LTD.
Fitting Cable : Equivalent to AWG#18

Note Since these terminals are allocated for internal connection, do not apply any signal or power source to these terminals.

Table 10. Connector CN9 Pin Assignment	
Pin No.	Symbol
1	V_{CC}
2	V_{CC}
3	GND
4	GND

Module side connector: B4P-VH
Mating connector : VHR-4N (housing)
BVH-21T-P1.1 or SVH-21T-P1.1 (contact)
Connector supplier : J.S.T TRADING COMPANY, LTD.
Fitting Cable : Equivalent to AWG#18

Note If using a long cable, applied voltage may be dropped because of its resistance.
Specified voltage should be applied correctly at the input of the Module side connector.

GENERAL CAUTION

(1) Caution for safety

- Because the Plasma Display Panel is made from fragile glass, shock and pressure to the Plasma Display module should be avoided.
  If the glass panel is broken, be careful to avoid injury from cracked glass.

(2) Caution when taking out the module

- Do not JOLT the glass panel when taking it out of the shipping package.

(3) Caution in handling the module

- The electrostatic discharge may break the Plasma Display module, if not handled with care.
- Do not pull the interface connectors in or out while the Plasma Display module is operating.
- The surface of the glass panel is easily scratched, do not rub or press the glass with hard material.
- When cleaning the glass surface, use a soft, dry, cloth, and wipe softly.
- Do not pour water or chemicals into the module, it causes the Plasma Display module to become damaged or will create defects.
- Handle connectors with care.

(4) Caution for operation

- Follow the supply voltage sequence. If the wrong sequence is applied, the module will be damaged.
- The Plasma Display module generators heat (about 380 W in all area white display) in narrow spaces, an appropriate air flow cooling system should be prepared.

(5) Caution for the atmosphere

- Dew-drop atmosphere should be avoided.
- Do not store and/or operate the Plasma Display module in a condition which exceeds the specified value.

(6) Cautions for module characteristics

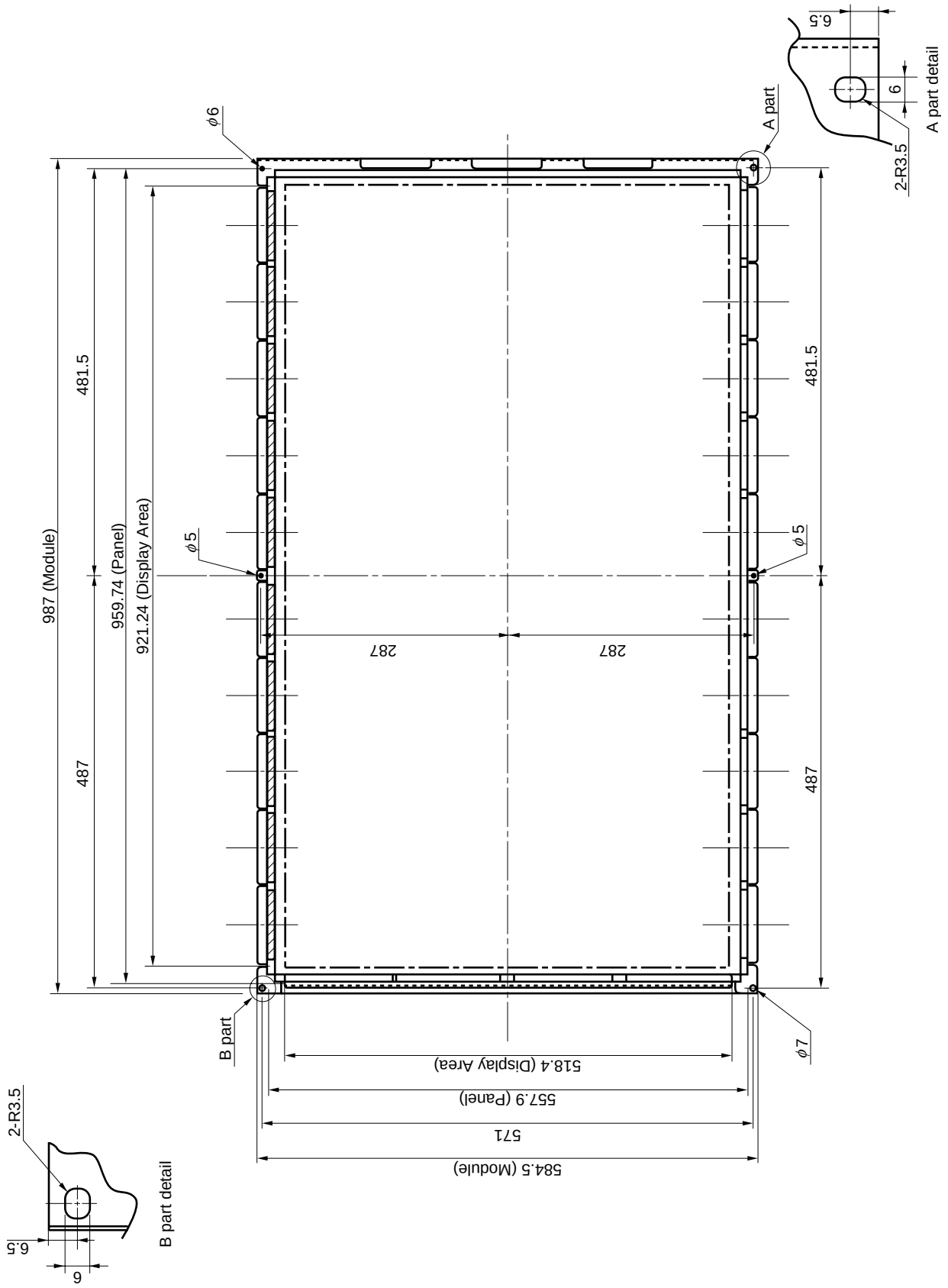
- Do not apply fixed pattern data signals to the Plasma Display module for long periods of time, doing so may cause image sticking.

(7) Other cautions

- Do not disassemble and re-assemble Plasma Display module.
- When returning the module for repair, please pack the module using original shipping packages.

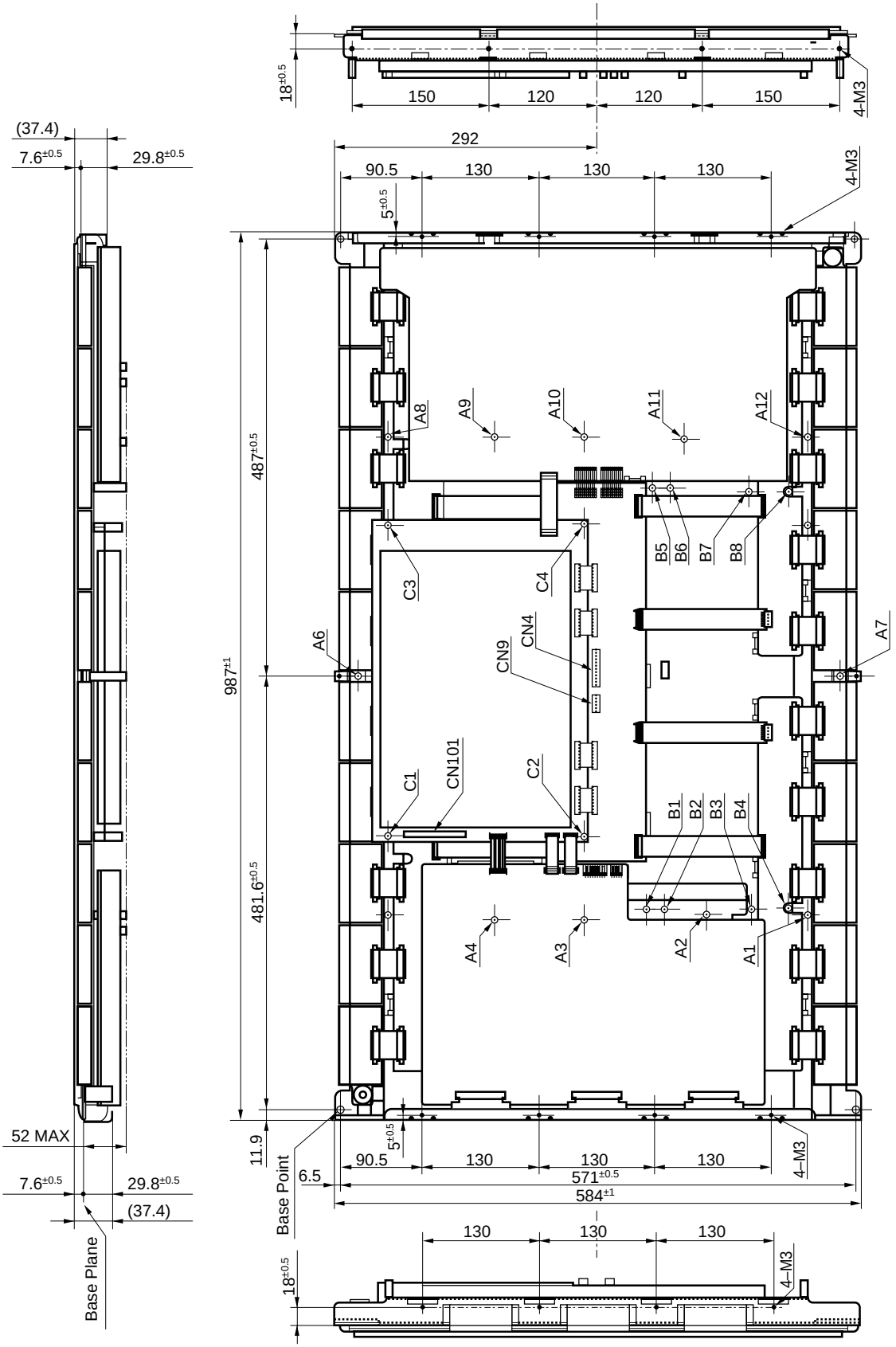
MECHANICAL DRAWING (Unit: mm)

FRONT VIEW



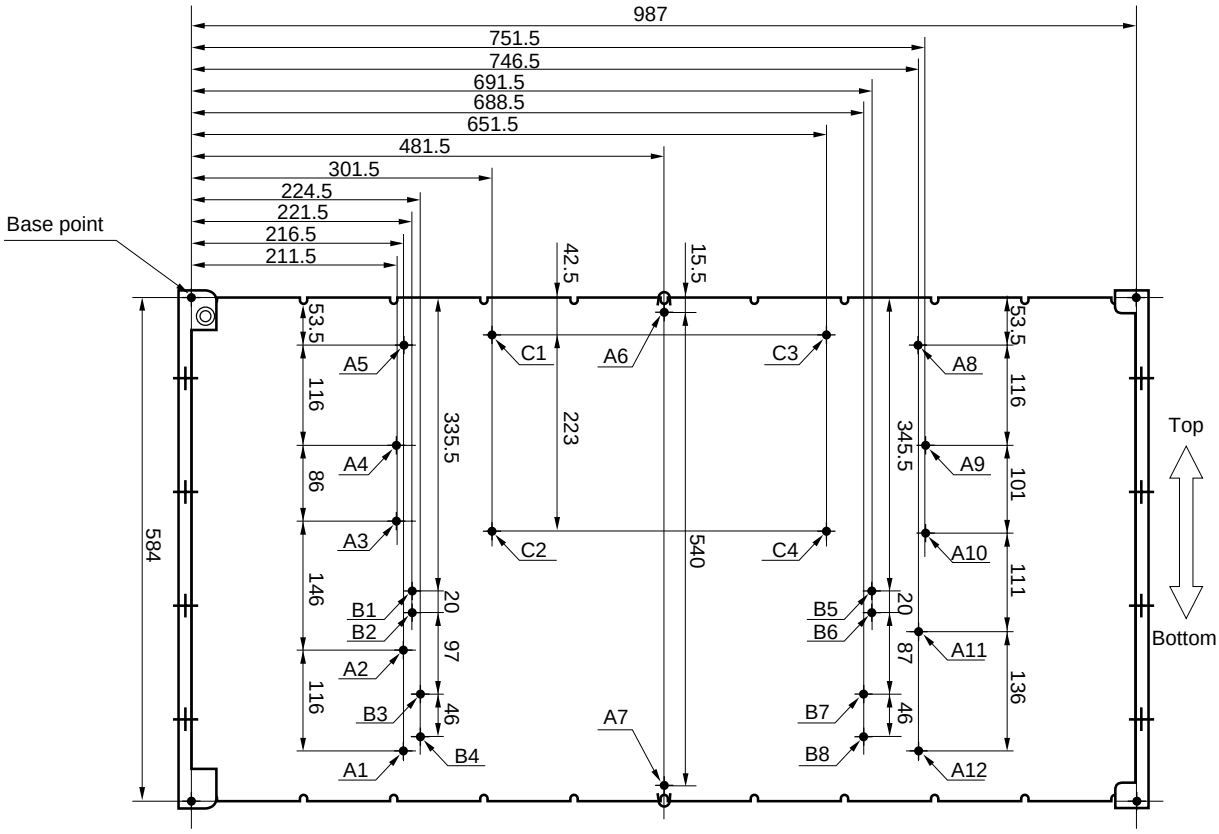
MECHANICAL DRAWING (Unit: mm)

REAR VIEW

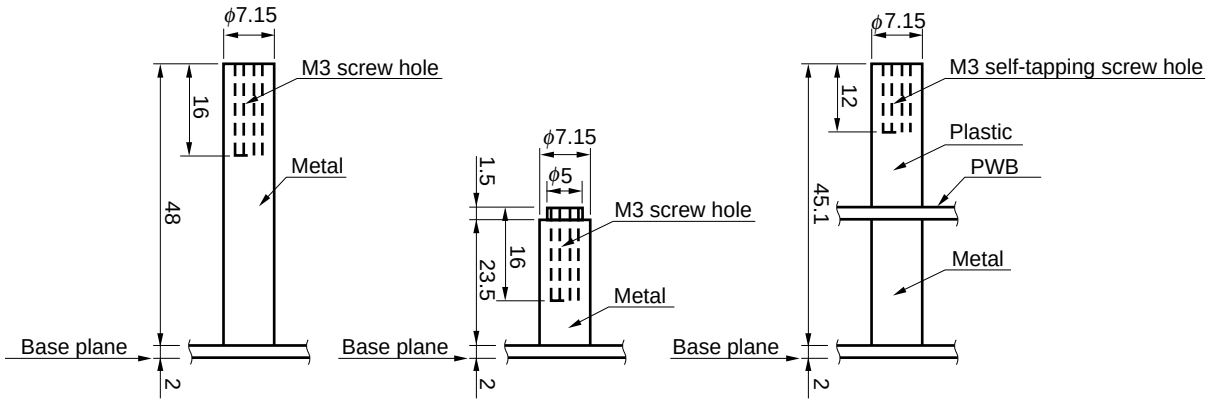


STUDS POSITION (Unit: mm)

REAR VIEW



SHAPE OF STUDS (Unit: mm)



Stud A **Stud B** **Stud C**

[MEMO]