NEC

# COLOR PDP MODULE
# NP4203MF02

## CosmoPlasma
**106 cm (42 inches), Wide Screen (853 × 480 Pixels), Digital Module**
**Digital 8-bit RGB Signal**

### DESCRIPTION

The NP4203MF02 is a 42-inch wide color PDP module with a resolution of 853 (H) x 480 (V) pixels. The display offers vibrant colors reproduced in a thin, low profile package. This device uses AC plasma technology developed by NEC and includes an 8-bit digital interface.

### FEATURES

- CCF (Applied Capsulated Color Filter) technology, developed at NEC, offers a high quality image match for CRT display. To offer remarkably pure colors, the color plasma display panel uses extremely clear, thin capsulated color filters to cut unnecessary light as the plasma discharges.
- Contrast ratio of 500:1 (typical value) is achieved through a new driving method, which offers improved black levels instead of toning down the white light emitted.
- The applied peak luminance enhancement (PLE) function enables the display to operate with ideal contrast. The PLE function makes it possible to adjust the average brightness level of the PDP display automatically in accordance with the average brightness level of an input video signal.

### APPLICATIONS

- Wide screen TV (aspect ratio 16:9)
- Public information displays
- Video conference systems
- Retail
- Education and training systems

**The information in this document is subject to change without notice.**

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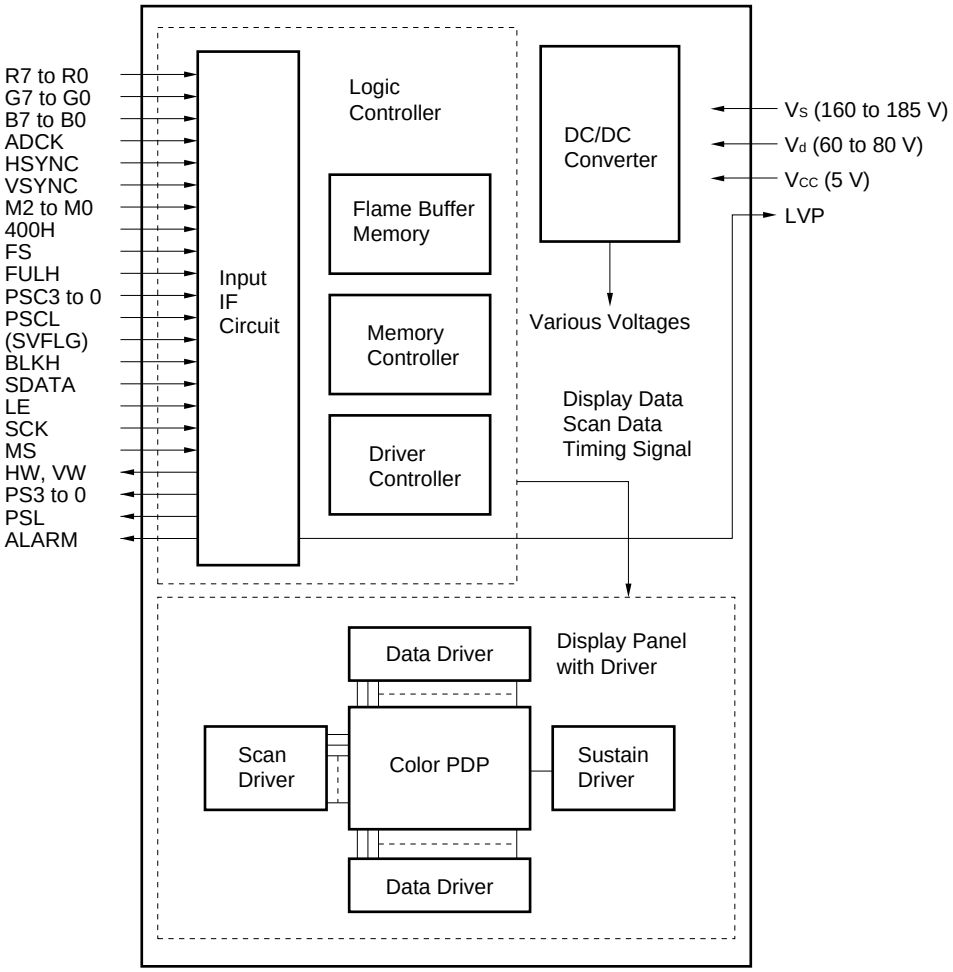
**STRUCTURE AND PRINCIPAL OPERATION OF PLASMA DISPLAY**

In a plasma display panel (PDP), row and column electrodes are placed between two glass substrates. A rare gas is then inserted between the substrates. When high voltage is applied to these electrodes, the gas is activated resulting in the radiation of ultraviolet light, similar to the operation of fluorescent lamps. These ultraviolet rays then activate the phosphor that coats the inside of the glass substrate, and visible light is emitted from the panel.

**ELECTRICAL INTERFACE OF PLASMA DISPLAY**

The NP4203MF02 requires 8 bits of digital video signals for each RGB color. In addition to the video signals, 12 kinds (14 bits) of digital control signals and 3 different DC voltages are required to operate the display. Five digital signals outputs and five digital inputs are provided for a “PLE” (peak luminance enhancement) function so that images can be displayed with the ideal contrast.

**BASIC CONFIGURATION**




**Note** SVFLG is used for NEC internal test mode.

## GENERAL SPECIFICATION

| | |
|---|---|
| **Display area** | 921 (H) × 518 (V) mm |
| **Outline dimensions** | 987 (W) × 584 (H) × 48 (D) mm |
| **Weight** | 17 kg |
| **Aspect ratio** | 16:9 |
| **Number of pixels** | 853 (H) × 480 (V) (1 pixel = 3 RGB cells) |
| **Pixel pitch** | 1.08 (H) × 1.08 (V) mm |
| **Color arrangement** | RGB vertical stripes |
| **Number of gradations** | 256 steps for PC RGB |
| **Peak brightness** | 400 cd/m$^2$ typical (VGA signal*****, 1/25 white window, PLE****** mode set to the maximum) |
| **Contrast ratio** | 500:1 (typ.) (VGA signal*****, 1/25 white window, PLE****** mode set to the maximum, measured in darkroom) |
| **Viewing angle** | 160 degrees (typical.) vertical and horizontal directions (angle at which brightness becomes half of front view brightness) |

***** Signal of fv = 59.94 Hz and fh = 31.47 kHz.

****** See the PLE (peak luminance enhancement) description.

## OPERATION ENVIRONMENTAL CONDITIONS

| | |
|---|---|
| **Temperature** | 0 to 50°C (with forced-air cooling) |
| **Humidity** | 20 to 80% RH (without condensation) |
| **Atmospheric pressure** | 800 to 1100 hPa |

## STORAGE ENVIRONMENTAL CONDITIONS

| | |
|---|---|
| **Temperature** | −20 to 60°C |
| **Humidity** | 10 to 90% RH (without condensation) |
| **Atmospheric pressure** | 700 to 1100 hPa |

## MECHANICAL TEST CONDITIONS

| | |
|---|---|
| **Vibration (operating)** | 0.5 G, 10 to 100 Hz, 3 directions, 10 minutes each |
| **Vibration (nonoperating)** | 0.5 G, 10 to 100 Hz, 3 directions, 2 hours each |

## LIFE EXPECTANCY

More than 10,000 hours of continuous operations

(Time when the brightness decreased to half to the initial)

## ELECTRICAL CHARACTERISTICS

### 1) Interface Signals; Absolute Ratings

Common conditions: Ta = 25°C, $V_{CC}$ = 5 V

**Table 1. Absolute Ratings**

| Item | | Parameter | Symbol | Ratings | Units |
|---|---|---|---|---|---|
| Input signals | R7 to R0, G7 to G0, B7 to B0, ADCK, HSYNC, VSYNC, M2 to M0, 400H, FS, FULH, PSC3 to PSC0, PSCL, BLKH, LE, SCK, SDATA, MS | Input voltage | Vi | −0.5 to 6.0 | V |
| | | Input current | Ii | ±20 | mA |
| Output signals | HW, VW, PS3 to PS0, PSL | Output voltage | Vo | −0.5 to 5.5 | V |
| | | Output current | Io | ±25 | mA |
| | ALARM, LVP | Output voltage | Vo | −0.5 to 5.5 | V |
| | | Output current | Io | ±25 | mA |

### 2) Interface Signals; Electrical Characteristics

Common conditions: Ta = 25°C, $V_{CC}$ = 5 V

**Table 2. Electrical Characteristics**

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| High level input voltage | $V_{IH}$ | – | 2.0 | – | – | V |
| Low level input voltage | $V_{IL}$ | – | – | – | 0.8 | V |
| Input current | $I_I$ | $V_I$ = $V_{CC}$ or GND | – | – | ±60 | μA |
| High level output voltage | $V_{OH}$ | $I_O$ = −20 μA | 4.4 | – | – | V |
| Low level output voltage | $V_{OL}$ | $I_O$ = 20 μA | – | – | 0.2 | V |

**SIGNAL FUNCTIONS**

**Table 3. Interface Signal Function**

| Symbol | I/O | Function | Remarks |
|---|---|---|---|
| R7 to R0 | I | 8 bits red video signal[Note 1] | (R7: MSB; R0: LSB) |
| G7 to G0 | I | 8 bits green video signal[Note 1] | (G7: MSB; G0: LSB) |
| B7 to B0 | I | 8 bits blue video signal[Note 1] | (B7: MSB; B0: LSB) |
| ADCK | I | Clock signal which synchronizes to video signal | |
| HSYNC | I | Horizontal synchronous signal tw = 4 $T_{ADCK}$ min. | (negative pulse) |
| VSYNC | I | Vertical synchronous signal tw = 200 ns min. | (negative pulse) |
| M2 to M0[Note 2] | I | These signal inputs are only used in a compatible operation with the previous model (NP4201MF02). | |
| 400H[Note 2] | I | | |
| FS[Note 2] | I | | |
| FULH[Note 2] | I | | |
| PSC3 to PSC0, PSCL | I | PLE control signal | (PSC3: MSB*; PSCL: LSB**) |
| SVFLG | I | NEC internal test function mode | (set to “L” level) |
| BLKH | I | Video blanking and muting[Note 3] | (“H” in muting) |
| SDATA | I | Serial data | (total 40 bit) |
| LE | I | SDATA latch enable | (negative logic) |
| SCK | I | SDATA clock | (latch in positive edge) |
| MS | I | Switch for parallel interface and serial interface mode | (set to “H” level) |
| PS3 to PS0, PSL | O | PLE average brightness level signal | (PS3: MSB, PS0: LSB) |
| HW | O | H window display period indication signal | (“H” in display period) |
| VW | O | V window display period indication signal | (“H” in display period) |
| ALARM | O | Alarm signal for broken panel or failure of internal power source.[Note 4] | (“L” in alarmed status) |
| LVP | O | Power supply shutdown signal upon alarm status[Note 4] | (“L” in alarmed status) |

*MSB : Most Significant Bit

**LSB : Least Significant Bit

**Notes 1.** The RGB video signal should be compensated by an Inverse $\gamma$ circuit before being input to the color plasma display module.

**2.** These signal inputs are used for parallel interface mode, which is compatible with the previous model (NP4201MF02), when the “MS” input is set to “L” level.

**3.** While BLKH input is at “H” level, the entire display area image turns to black color display.

**4.** When ALARM output turns to “L” level, high voltage power input (Sustain power supply: Vs; data power supply: Vd) should be switched off immediately. If the glass panel is broken, high voltage may occur at the electrode section and cause electric shock. Failure of the internal power source causes over-power status and damages the display panel and driver circuits.

**Table 4. Contents of SDATA (Serial imput data) in serial interface mode.**

| Data | Signal name | Function | Remarks |
|---|---|---|---|
| D0 | VIDEOH | Switch for “Video mode” and “PC mode” | H: Video mode; L: PC mode |
| D1 | LIFEH | Switch for PLE brightness control level | L: PLE normal operation<br>H: Low brightness level operation for longer life |
| D2 | ---- | Fix to “L” level | For NEC internal check use |
| D3 | SELFPLEH | Switch for “Internal PLE control” and “External PLE control” | H: Internal PLE control<br>L: External PLE control |
| D4 | TSELB | Switch for ADCK data latch timing | H: Falling edge L: Rising edge |
| D5 | FV2 | Vertical frequency selection | (Hz) 50 56-64 66 67-71 72-75<br>FV2 L L L L H<br>FV1 L L H H L<br>FV0 L H L H L |
| D6 | FV1 | | |
| D7 | FV0 | | |
| D8 | DISPLINE0 | Display line number | L: 400 line H: 480 lines |
| D9 | DISPDOT0 | Display pixel numbers/line | L: 640 pixels/line (Normal display mode)<br>H: 853 pixels/line (Full display mode) |
| D10 | VDELAY (Spare bit) | Fix to “L” level | |
| D11 | VDELAY256 | Vertical display start position<br>Refer to the “Dv” in Table 5 | Set the display start line number after the falling edge of VSYNC.<br>Range of setting line number: 0 to 511 |
| D12 | VDELAY128 | | |
| D13 | VDELAY64 | | |
| D14 | VDELAY32 | | |
| D15 | VDELAY16 | | |
| D16 | VDELAY8 | | |
| D17 | VDELAY4 | | |
| D18 | VDELAY2 | | |
| D19 | VDELAY1 | | |
| D20 | HDELAY (Spare bit) | Fix to “L” level | |
| D21 | HDELAY512 | Horizontal display start position<br>Refer to the “Dh” in Table 5 | Set the display start pixel number after the falling edge of HSYNC.<br>Range of setting pixel number: 0 to 1023 |
| D22 | HDELAY256 | | |
| D23 | HDELAY128 | | |
| D24 | HDELAY64 | | |
| D25 | HDELAY32 | | |
| D26 | HDELAY16 | | |
| D27 | HDELAY8 | | |
| D28 | HDELAY4 | | |
| D29 | HDELAY2 | | |
| D30 | HDELAY1 | | |
| D31 | HPOS3 | Setting of horizontal display position in normal mode (640 pixel/line display). Display position is adjustable by 2 pixel steps. | Position Left ---------- Center ---------- Right<br>HPOS3 L L L …… H …… H H H<br>HPOS2 L L L …… L …… H H H<br>HPOS1 L L H …… L …… L H H<br>HPOS0 L H L …… L …… H L H |
| D32 | HPOS2 | | |
| D33 | HPOS1 | | |
| D34 | HPOS0 | | |
| D35 | MASKLEVEL2 | Gray level in blank area<br>(Possible to set 0-24% of white level) | Level (%) 0 1.5 3 6 12 16 19 24<br>ML2 L L L L H H H H<br>ML1 L L H H L L H H<br>ML0 L H L H L H L H |
| D36 | MASKLEVEL1 | | |
| D37 | MASKLEVEL0 | | |
| D38 | Spare bit | Fix to “L” level | |
| D39 | Spare bit | Fix to “L” level | |

## VIDEO SIGNAL INPUT AND SIGNAL TIMING

**Table 5. Relation Between Input Video Signal and Module RGB Signal Input**

| | Video Signal | | | | | | RGB Signal | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Normal Display Mode (Aspect Ratio 4:3) | | | | | | | | | Full Display Mode (Aspect Ratio 16:9) | | | | | | | |
| | No. | Signal Name | Display Resolution (Dot · Line) | Vert. Freq. (Hz) | Number of Lines In One Frame | Horiz. Freq. (kHz) | Recommended ratio between dot-clock freq. and horiz. freq. (Horiz. freq. : MHz) | Nominal data read start timing after sync. signal | | Mode Signal | | | | | | Recommended ratio between dot-clock freq. and horiz. freq. (Horiz. freq. : MHz) | Nominal data read start timing after sync. signal | | Mode Signal | | | | |
| | | | | | | | | Dv | Dh | DL0 | DD0 | FV2 | FV1 | FV0 | | | Dv | Dh | DL0 | DD0 | FV2 | FV1 | FV0 |
| Vide mode | 1 | EUTV1 | 853 · 480 | 50.0 | 525 | 26.25 | 780 (24.38) | 46 | 171 | H | L | L | L | L | 1040 (32.50) | 46 | 228 | H | H | L | L | L |
| | 2 | EUTV2 | 853 · 480 | 59.94 | 525 | 31.47 | 780 (24.55) | 35 | 116 | H | L | L | L | H | 1040 (32.73) | 35 | 154 | H | H | L | L | H |
| | 3 | HDTV | 853 · 480 | 60 | 1125/2 | 33.75 | | | | | | | | | 1054 (35.57) | 40 | 113 | H | H | L | L | H |
| PC mode | 4 | NEC | 640 · 400 | 56.4 | 440 | 24.83 | 848 (21.05) | 33 | 149 | L | L | L | L | H | 1130 (28.06) | 33 | 199 | L | H | L | L | H |
| | 5 | NEC | 640 · 400 | 70 | 449 | 31.47 | 800 (25.18) | 36 | 143 | L | L | L | H | H | 1066 (33.55) | 36 | 191 | L | H | L | H | H |
| | 6 | IBM | 640 · 400 | 70 | 449 | 31.47 | 800 (25.18) | 36 | 146 | L | L | L | H | H | 1066 (33.55) | 36 | 195 | L | H | L | H | H |
| | 7 | VGA | 640 · 480 | 59.94 | 525 | 31.47 | 800 (25.18) | 35 | 144 | H | L | L | L | H | 1066 (33.55) | 35 | 192 | H | H | L | L | H |
| | 8 | IBM | 640 · 480 | 59.94 | 525 | 31.47 | 800 (25.18) | 27 | 136 | H | L | L | L | H | 1066 (33.55) | 27 | 181 | H | H | L | L | H |
| | 9 | NEC | 640 · 480 | 59.94 | 525 | 31.47 | 800 (25.18) | 39 | 145 | H | L | L | L | H | 1066 (33.55) | 39 | 193 | H | H | L | L | H |
| | 10 | MAC | 640 · 480 | 66.66 | 525 | 35.00 | 864 (30.24) | 42 | 160 | H | L | L | H | L | 1152 (40.32) | 42 | 213 | H | H | L | H | L |
| | 11 | VESA | 640 · 480 | 72.8 | 520 | 37.86 | 832 (31.5) | 31 | 168 | H | L | H | L | L | 1109 (42.00) | 31 | 224 | H | H | H | L | L |
| | 12 | VESA | 640 · 480 | 75 | 500 | 37.5 | 840 (31.5) | 19 | 184 | H | L | H | L | L | 1120 (42.00) | 19 | 245 | H | H | H | L | L |
| | 13 | IBM | 640 · 480 | 75 | 525 | 39.38 | 800 (31.5) | 34 | 144 | H | L | H | L | L | 1067 (42.00) | 34 | 192 | H | H | H | L | L |

**Notes 1.** Maximum data clock (ADCK) frequency is 50 MHz.

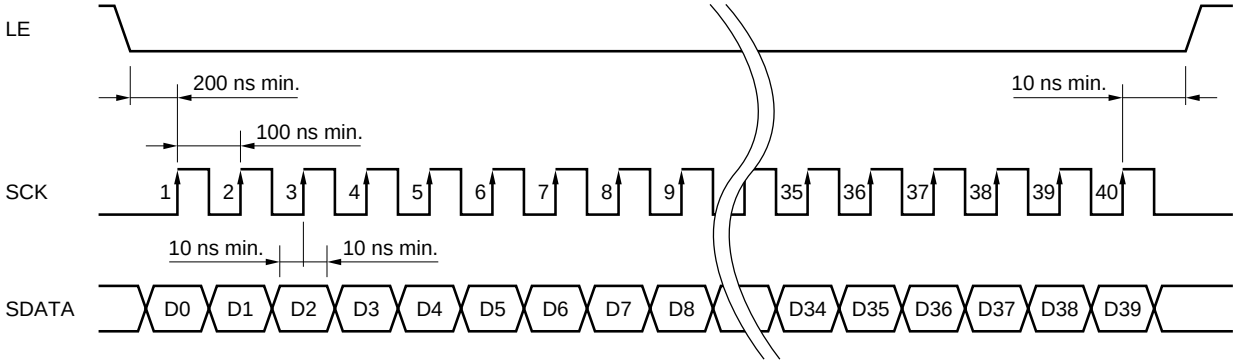
**2.** Maximum horizontal frequency in Video mode is 47 kHz.

**3.** Maximum horizontal frequency in PC mode is 70 kHz.

**4.** Vertical frequency range is 50 Hz to 75 Hz.

**5.** D8 (DISPLINEO) and D9 (DISPDOTO) of serial input data should be set correctly according to the display data. If they are not correct, the PLE function will not operate correctly.

**Setup of control mode signals and display position**




Setup Sequence:

1. Set LE to “L” level.
2. Enter the 40 bits of SDATA into the module synchronizing to the serial clock signal (SCK)
3. Set LE to “H” level.

**Notes: 1.** Serial input data should be refreshed at least in every 5 or 6 seconds or less.

**2.** Serial input data (SDATA) is latched into the module at the trailing edge of the VSYNC signal after the “LE” signal is returned to “H” level. When VSYNC is overlapped with the “LE” signal’s “L” period, the serial data is latched with the next VSYNC timing.

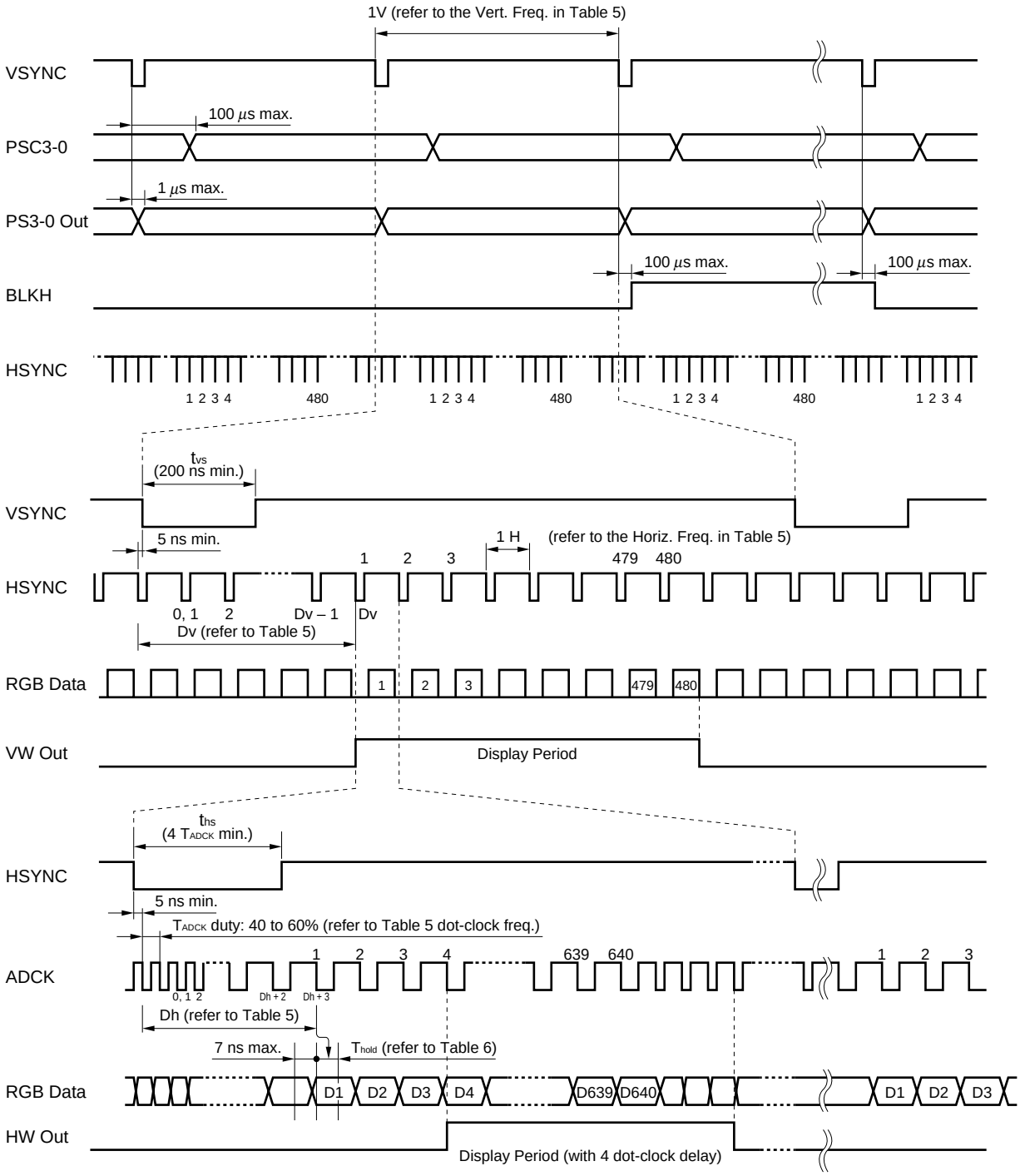
**3.** When power is supplied to the module, serial data in the module has vague status. Therefore, serial data should be refreshed after power on.

**SIGNAL TIMING**

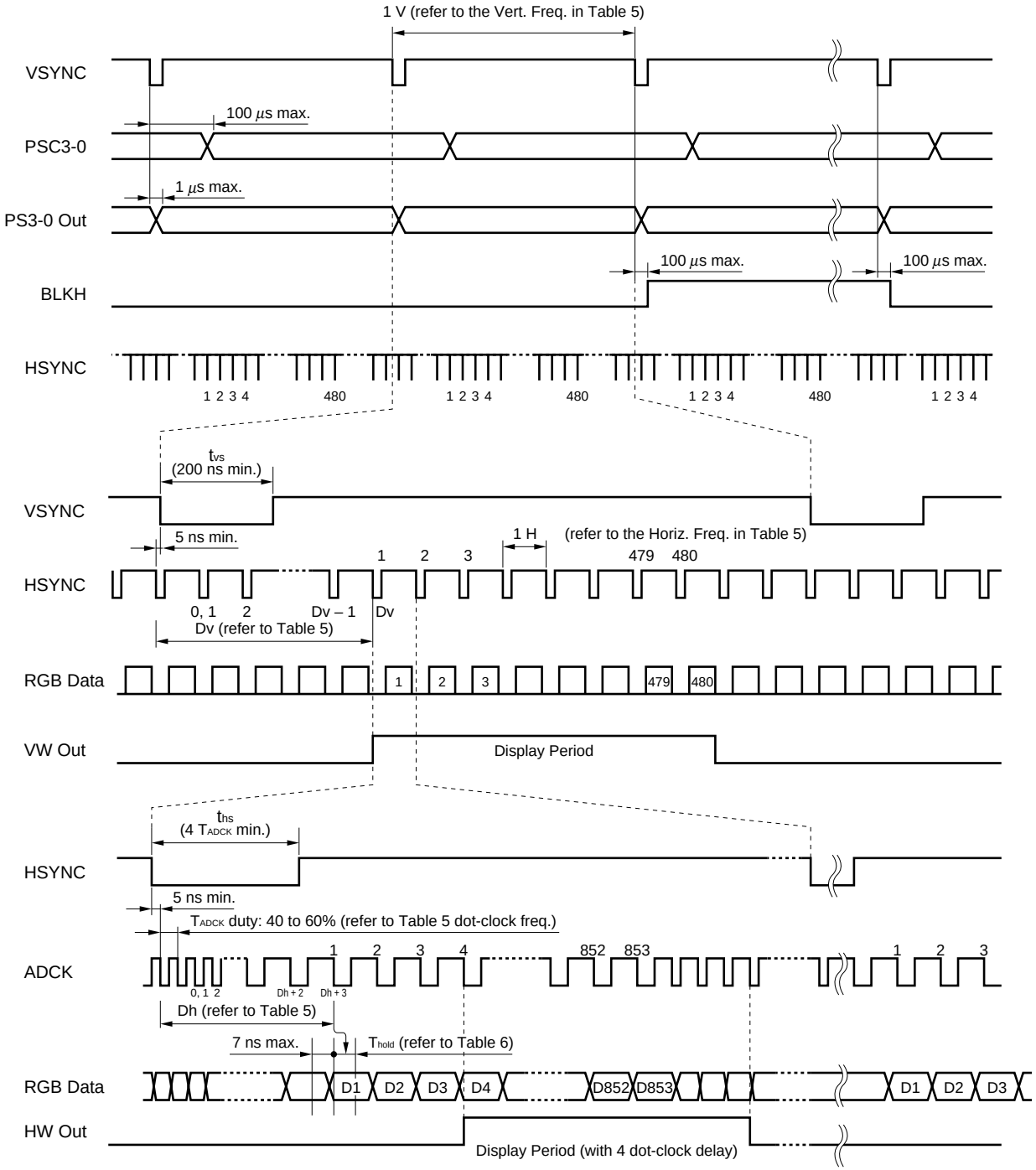
Refer to the timing diagram on the following pages.

- Input video signal format is determined by the mode signal (refer to Table 5).
- “TADCK” shows 1 cycle period of ADCK.
- “$t_{vs}$” shows negative pulse width of VSYNC.
- “$t_{vh}$” shows negative pulse width of HSYNC.
- “1H” shows 1 cycle period of HSYNC (horizontal synchronous signal).
- “1V” shows 1 cycle period of VSYNC (vertical synchronous signal).
- “Dv” is a period between “leading edge of the vertical synchronous pulses” and “valid RGB lines data read start timing.”
- “Dh” is a period between “leading edge of the horizontal synchronous pulse” and “valid RGB dots data read start timing.”
- When normal mode (640-dot mode) is selected, both sides are masked with gray patterns.
- When 400 lines are selected, the upper 40 lines and lower 40 lines are masked with gray patterns.

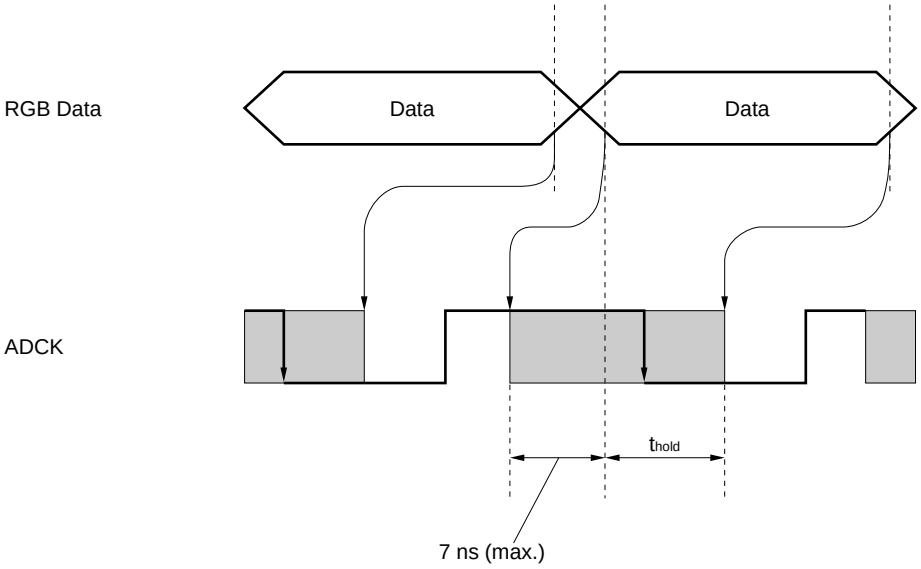
**Timing Diagram (Normal Display Mode, 480 Lines)**



**Timing Diagram (Full Display Mode, 480 Lines)**



**RGB Data Read Timing by ADCK**

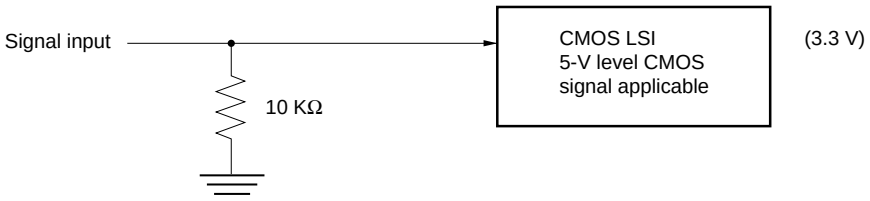



| ADCK (Data Cycle Time) | | $t_{hold}$ (ns) |
|---|---|---|
| Frequency (MHz) | Cycle time (ns) | |
| 20 to 25 | 50 to 40 | 17 |
| 26 to 30 | 39 to 33 | 12 |
| 31 to 35 | 32 to 28 | 7 |
| 36 to 42 | 27 to 23 | 3 |

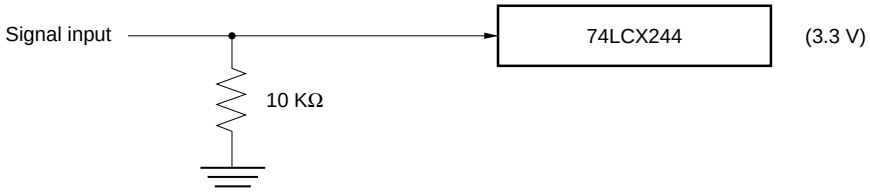
**INPUT AND OUTPUT DRIVE CIRCUITS**

Following are definitions of the input and output drive circuits for all interface signals and the PDP module.

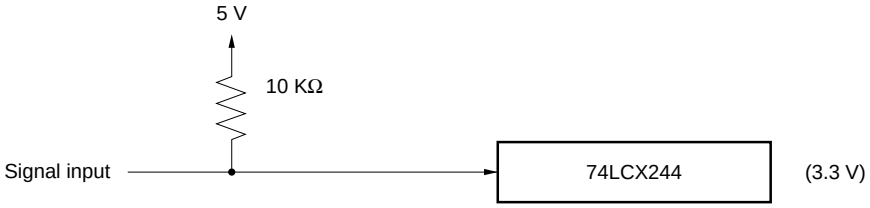
**(1) R7-R0, G7-G0, B7-B0. M2-M0, 400H, ADCK, HSYNC, VSYNC, FS, FULH, BLKH (SVFLG)**




**(2) SCK, SDATA, LE**



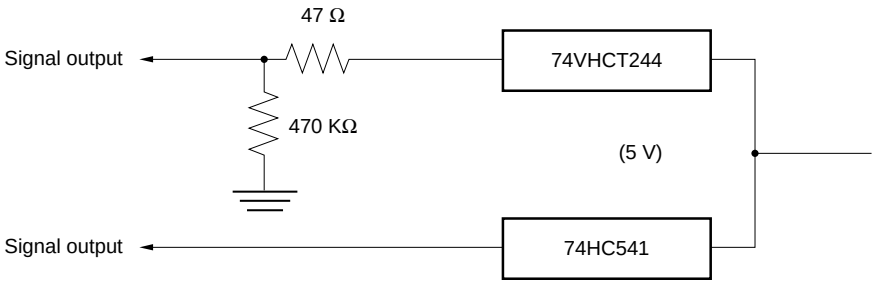

**(3) PSC3-PSC0, PSCL**



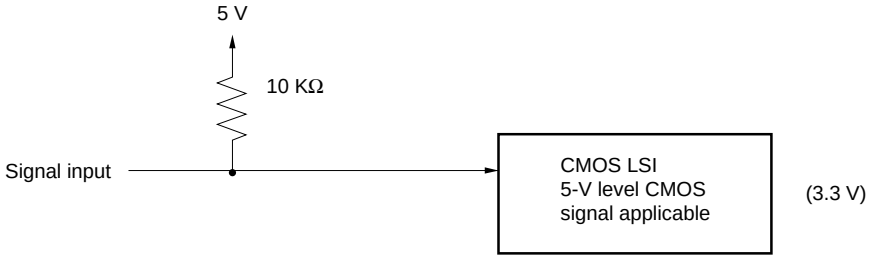

**(4) HW, VW, PS3-PSO, PSL**


**(5) ALARM**

**(6) LVP**




**(7) MS**



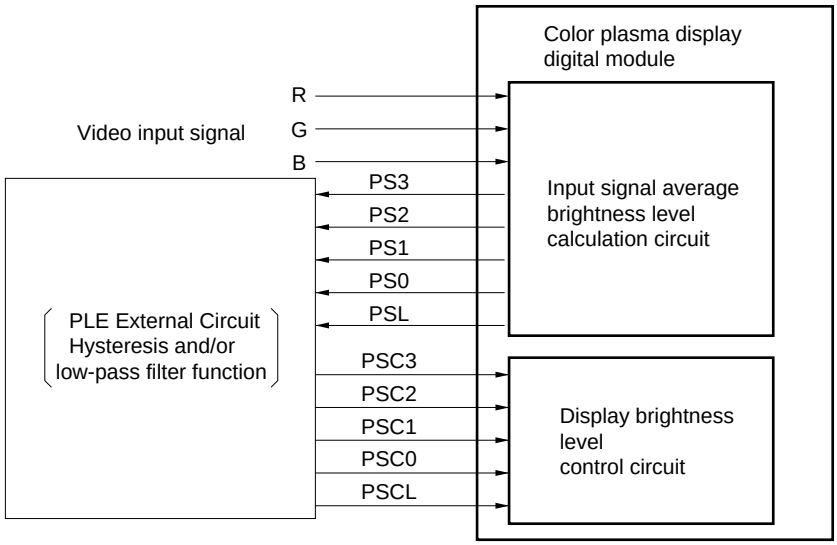
## PLE (PEAK LUMINANCE ENHANCEMENT) FUNCTION

### 1) Basic Function of the PLE

The PLE function makes it possible to increase or decrease the average brightness level of the PDP display when the typical brightness level of the input video signal is lower or higher than the average brightness of the previous frame. This PLE function control reduces power consumption and results in a higher contrast level. External circuitry is required to take advantage of the PLE function.

The PLE control circuits can be constructed by connecting external hysteresis and/or low-pass filter circuits (PLE external circuit) between PSC3-0, PSCL (PLE control signal input) and PS3-0, PSL (PLE control signal output).

The PLE brightness change response characteristic depends on the characteristics of the PLE external circuit.



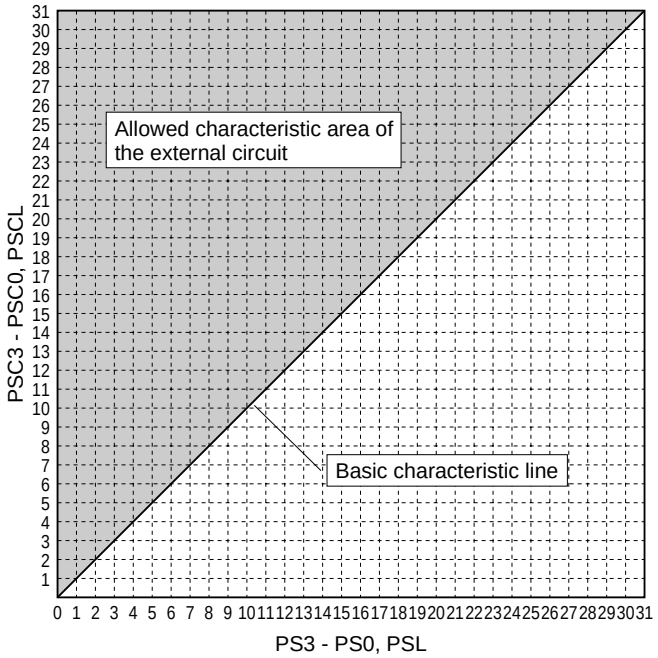

### 2) Characteristics of the PLE external circuit

This digital module is designed to use the PLE function, and input signals (PSC3 - PSC0 and PSCL) should vary linearly to the output signals (PS3 - PS0 and PSL). (A short time of delayed response is allowed.)

The figure at right shows the basic characteristic line for module design and the allowed characteristic area of the external circuit.

If the PLE function is not used, PSC3-PSC0 and PSCL inputs should be set to “H” level or be kept open. In this case, the brightness level is set to a minimum.

PS3 - PS0 and PSL output signals are refreshed in every frame.



**3) PLE Response Characteristic and Variance of Brightness and Display (Sustain) Current**

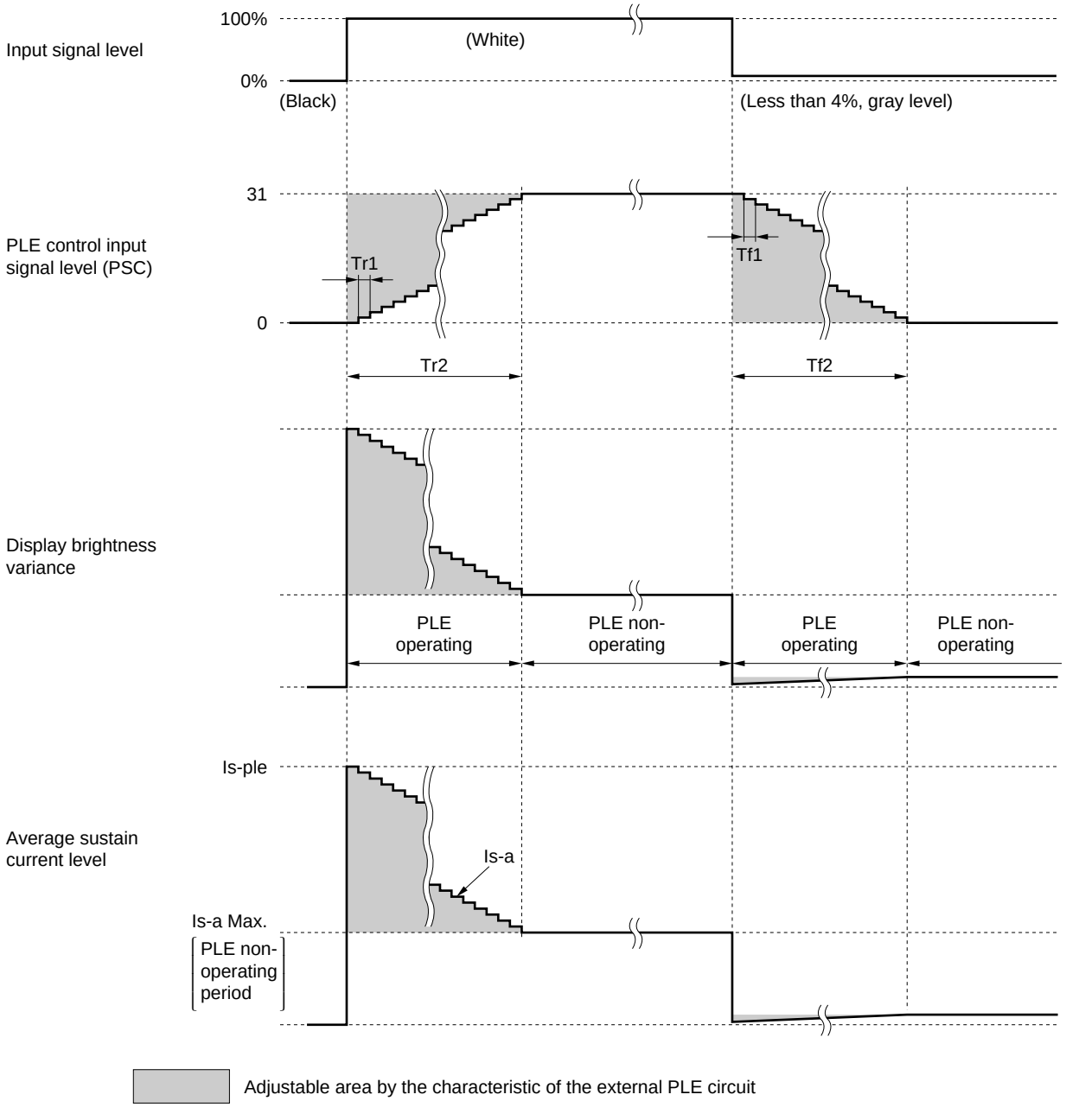
PLE response time depends on the external circuit (hysteresis and/or low-pass filter) that is connected to the module.

Generally, these kinds of external circuits have a delayed response, which occasionally intreases the current during the response period.

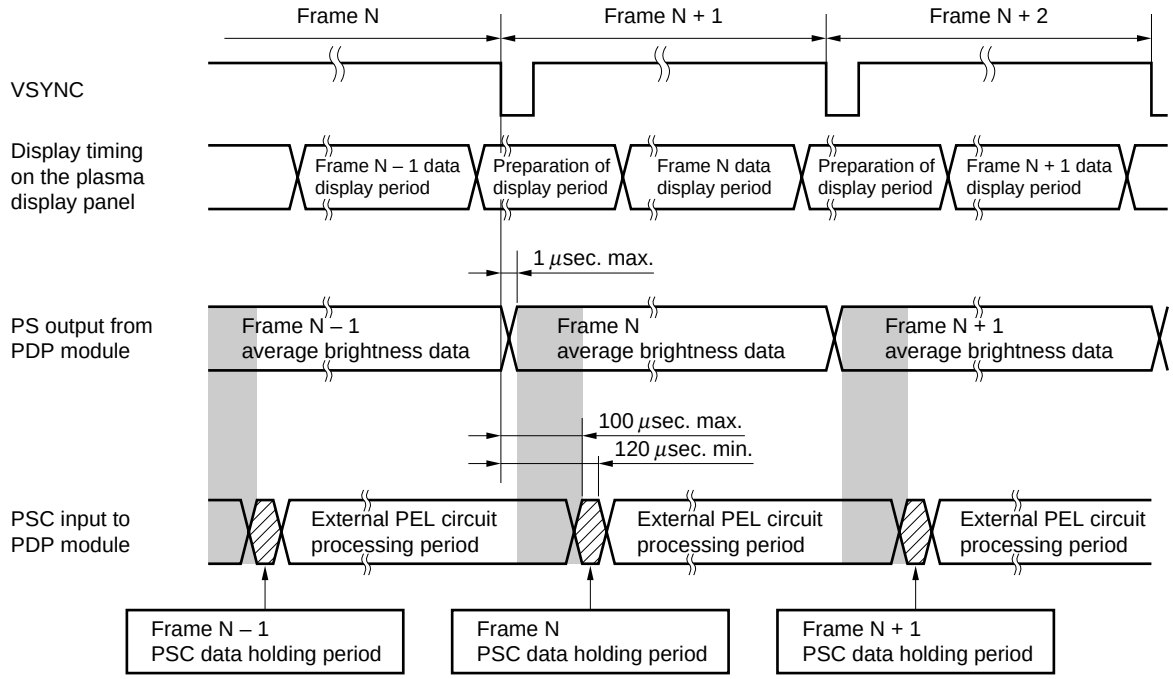
In order to avoid overpower status, the PLE response is specified as follows.

| Item | Symbol | Min. | Max. | Recommendation | Unit |
|---|---|---|---|---|---|
| 1 step increment response time | Tr1 | 0 | 2.5 | 0 to 0.25 | Sec |
| All steps increment response time | Tr2 | 0 | 75 | 0 to 7.5 | Sec |
| 1 step decrement response time | Tf1 | 0 | ---- | 0.1 to 0.25 | Sec |
| All steps decrement response time | Tf2 | 0 | ---- | 3 to 7.5 | Sec |

Condition: Input signal jumps up and down in the following sequence.



**PLE SIGNAL TIMING**




**Note:** If PS data is read out from the module and PSC data is put into the module within the same period, display brightness can be controlled with the average brightness of same frame.

When PSC data is put into the module after the “PSC data holding period,” brightness is controlled with a 1-frame delayed response.

**POWER INPUT AND OUTPUT**

**1) Sustain Power Supply**

**Table 6. Power Supply**

| Item | Symbol | Condition and Remarks | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Absolute Maximum | ---- | -------- | ---- | ---- | 200 | V |
| Voltage | Vs | Dependent on the characteristics of each PDP[Note] | 160 | ---- | 185 | V |
| Voltage Stability | ---- | -------- | ---- | ---- | ±1.0 | % |
| Average Current | Is-a | At PLE nonoperation period | 0.1 | ---- | 2.0 | A |
| Average Current at PLE Operation | Is-ple | When input signal is changed from all-black level (00000) to all-white level (11111) | ---- | ---- | 5.5 | A |
| Peak Current | Is-peak | -------- | ---- | ---- | 15 | A |
| Voltage Regulation | ---- | At peak current | ---- | ---- | 5 | V |
| Ripple and Noise | ---- | -------- | ---- | ---- | 500 | mV p-p |

**Note:** Voltage should be set to a specified value, which is located on a label attached to the module.

**2) Data Power Supply**

**Table 7. Data Power Supply**

| Item | Symbol | Condition and Remarks | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Absolute Maximum | ---- | ---- | ---- | ---- | 90 | V |
| Voltage | Vd | Dependent on the characteristics of each PDP[Note] | 60 | ---- | 80 | V |
| Voltage Stability | ---- | ---- | ---- | ---- | ±1.5 | % |
| Average Current | Id-a | Varied correspondence to the Image | 0.005 | ---- | 2.0 | A |
| Ripple and Noise | ---- | ---- | ---- | ---- | 300 | mV p-p |

**Note:** Voltage should be set to a specified value, which is located on a label attached to the module.

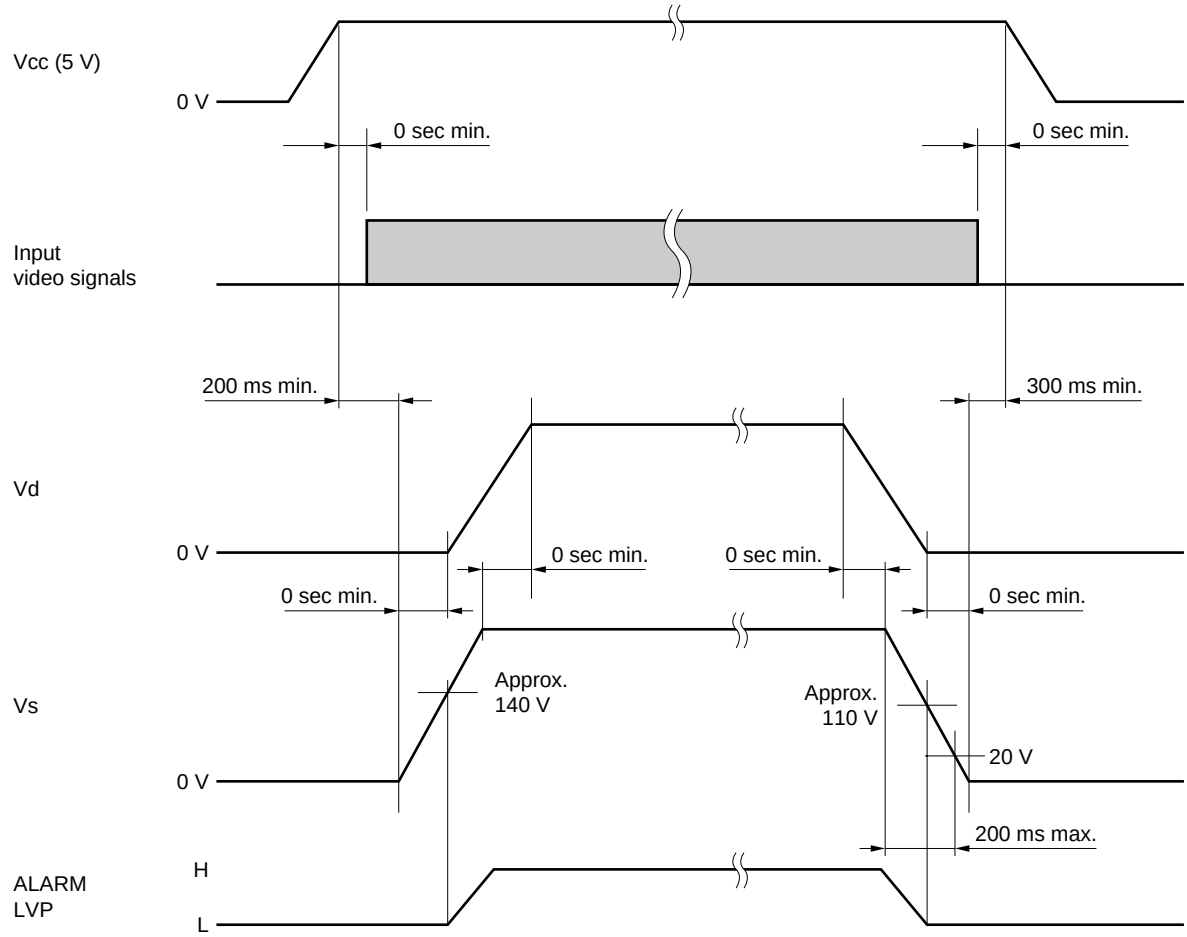
**3) Logic Power Supply**

**Table 8. Logic Power Supply**

| Item | Symbol | Condition and Remarks | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Absolute Maximum | ---- | -------- | ---- | ---- | 6.00 | V |
| Voltage Range | $V_{CC}$ | --------- | 4.75 | 5.00 | 5.25 | V |
| Current[Note] | $I_{CC}$ | -------- | 1.2 | 2.0 | 3.0 | A |
| Ripple | ---- | -------- | ---- | ---- | 30 | mV p-p |
| Noise | ---- | -------- | ---- | ---- | 300 | mV p-p |

**Note:** This module provides an automatic operation-stop function for internal malfunctions. When the module stops the operation, logic current may decrease to almost zero (0). Even if logic current becomes zero, applied voltage should be kept to less than 6.0 volts.

**Supply Voltage and Signal Sequence**




**Notes: 1.** The power ON/OFF sequence is as follows (refer to the above sequence diagram):
Power ON sequence : Vcc → Vs → Vd
Power OFF sequence: Vd → Vs → Vcc

**2.** The power source for the Input signal circuit and Vcc can be switched on and off at the same time.

**3.** When the ALARM and LVP signals are “L,” High voltage should be shut down. However, when Vcc is applied at first, ALARM and LVP signals are kept “L” until Vs is applied. In order to enable “high-voltage power supply” operation, the initial ALARM and LVP signals’ status “L” should be disregarded.

**CONNECTOR PIN ASSIGNMENT**

(for the connector position, please refer to the Rear View in the Outline Drawing)

**1) Signal Interface Connector**

**Table 9. Connector CN101 Pin Assignment**

| Pin No. | Symbol | Pin No. | Symbol | Pin No. | Symbol | Pin No. | Symbol |
|---|---|---|---|---|---|---|---|
| 1 | R7 | 2 | GND | 41 | B3 | 42 | GND |
| 3 | R6 | 4 | GND | 43 | B2 | 44 | GND |
| 5 | R5 | 6 | GND | 45 | B1 | 46 | GND |
| 7 | R4 | 8 | GND | 47 | B0 | 48 | GND |
| 9 | R3 | 10 | GND | 49 | ADCK | 50 | GND |
| 11 | R2 | 12 | GND | 51 | HSYNC | 52 | GND |
| 13 | R1 | 14 | GND | 53 | VSYNC | 54 | PSL |
| 15 | R0 | 16 | GND | 55 | M2 | 56 | M1 |
| 17 | G7 | 18 | GND | 57 | M0 | 58 | 400H |
| 19 | G6 | 20 | GND | 59 | FS | 60 | FULH |
| 21 | G5 | 22 | GND | 61 | HW | 62 | GND |
| 23 | G4 | 24 | GND | 63 | VW | 64 | PS3 |
| 25 | G3 | 26 | GND | 65 | PS2 | 66 | PS1 |
| 27 | G2 | 28 | GND | 67 | PS0 | 68 | MS |
| 29 | G1 | 30 | GND | 69 | PSC3 | 70 | PSC2 |
| 31 | G0 | 32 | GND | 71 | PSC1 | 72 | PSC0 |
| 33 | B7 | 34 | GND | 73 | ALARM | 74 | PSCL |
| 35 | B6 | 36 | GND | 75 | SVFLG | 76 | BLKH |
| 37 | B5 | 38 | GND | 77 | LE | 78 | SCK |
| 39 | B4 | 40 | GND | 79 | SDATA | 80 | GND |

N.C.: nonconnection pin

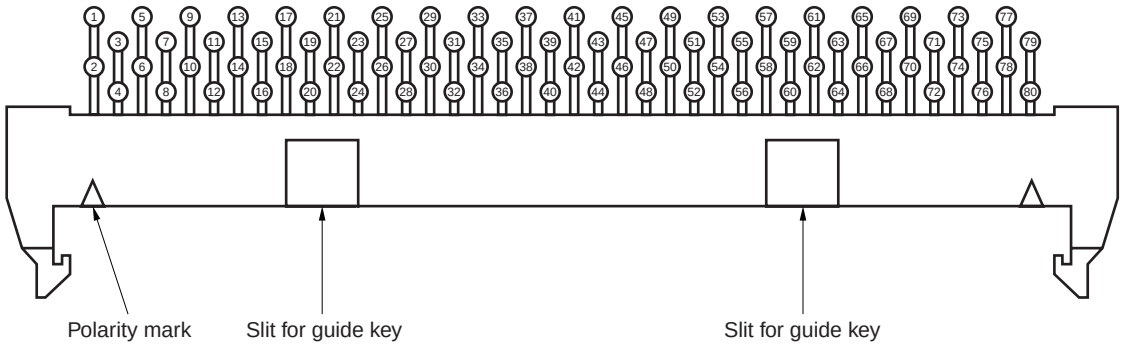
Module side connector: TX3-80P-D2ST-SN1

Mating connector : TX1-80S-D2P1-1D

Connector supplier : Japan Aviation Electronics Industry, Limited (JAE)

Fitting cable : 80-conductor flat cable, 0.635 mm pitch (equivalent to AWG#30)

**TX3-80P-D2ST-SN1 pin numbers (Top view)**

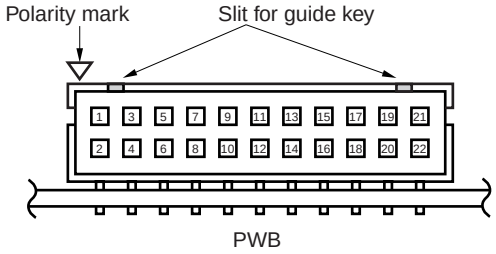


**2) Power Input Connector**

**Table 10. Connector CN104 Pin Assignment**

| Pin No. | Symbol | Pin No. | Symbol |
|---|---|---|---|
| 1 | LVP | 2 | N.C. |
| 3 | GND | 4 | GND |
| 5 | GND | 6 | GND |
| 7 | $V_{CC}$ (+5 V) | 8 | $V_{CC}$ (+5 V) |
| 9 | GND | 10 | GND |
| 11 | GND | 12 | GND |
| 13 | N.C. | 14 | N.C. |
| 15 | Vd | 16 | Vd |
| 17 | N.C. | 18 | N.C. |
| 19 | Vs | 20 | Vs |
| 21 | Vs | 22 | Vs |

**DF1B-22DP-2.5DS pin numbers**
**(View from the pin connection side)**

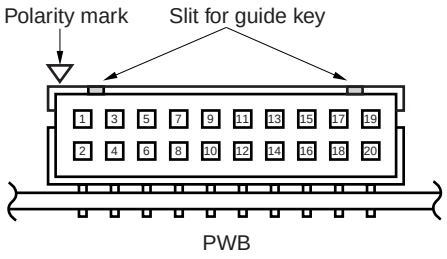



N.C.: Nonconnection pin
Module side connector: DF1B-22DP-2.5DS
Mating connector : DF1B-22DS-2.5RC (housing),
DF1B-2022SC or DF1B-2022SCF (contact)
Connector supplier : HIROSE Electric Co., Ltd.
Fitting cable : Equivalent to AWG#20

**Table 11. Connector CN105 Pin Assignment**

| Pin No. | Symbol | Pin No. | Symbol |
|---|---|---|---|
| 1 | Vs | 2 | Vs |
| 3 | Vs | 4 | Vs |
| 5 | N.C. | 6 | N.C. |
| 7 | Vd | 8 | Vd |
| 9 | N.C. | 10 | N.C. |
| 11 | GND | 12 | GND |
| 13 | GND | 14 | GND |
| 15 | $V_{CC}$ (+5 V) | 16 | $V_{CC}$ (+5 V) |
| 17 | GND | 18 | GND |
| 19 | GND | 20 | N.C. |

**DF1B-20DP-2.5DS pin numbers**
**(View from the pin connection side)**




N.C.: Nonconnection pin
Module side connector: DF1B-20DP-2.5DS
Mating connector : DF1B-20DS-2.5RC (housing),
DF1B-2022SC or DF1B-2022SCF (contact)
Connector supplier : HIROSE Electric Co., Ltd.
Fitting cable : Equivalent to AWG#20

**Note:** If using a long cable, applied voltage may be dropped because of its resistance.
Specified voltage should be applied correctly at the input of the module side connector.

## 1. Warnings and Cautions

Warning: Indicates a hazard that can lead to death or injury if the warning is ignored and the product is handled incorrectly.

Caution : Indicates a hazard that can lead to injury or damage to property if the caution is ignored and the product is handled incorrectly.

**[Warning]**

(1) This product uses a high voltage (350 V MAX.). Do not touch the circuitry of this product with your hands when power is supplied to the product or immediately after turning off the power. Be sure to confirm that the voltage has dropped to a sufficiently low level.

(2) Do not supply a voltage higher than that specified to this product. This can damage the product and may cause a fire.

(3) Do not use this product in locations where the humidity is extremely high, where it may be splashed with water, or where it is surrounded by flammable materials. Do not install or use the product in a location that does not satisfy the specified environmental conditions. This can damage the product and may cause a fire.

(4) If a foreign substance (such as water, metal, or liquid) gets inside the product, immediately turn off the power. Continuing to use the product as it is may cause fire or electric shock.

(5) If the product emits smoke, an abnormal smell, or makes an abnormal sound, immediately turn off the power. If nothing is displayed or if the display goes out during use, immediately turn off the power. Continuing to use the product as it is may cause fire or electric shock.

(6) Do not disconnect or connect the connector while power to the product is on. It takes some time for the voltage to drop to a sufficiently low level after the power has been turned off. Confirm that the voltage has dropped to a safe level before disconnecting or connecting the connector. Otherwise, this may cause fire, electric shock, or malfunctioning.

(7) Do not pull out or insert the power cable from/to an outlet with wet hands. Doing so may cause electric shock.

(8) Do not damage or modify the power cable. Doing so may cause fire or electric shock.

(9) If the power cable is damaged, or if the connector is loose, do not use the product; otherwise, this can lead to fire or electric shock.

(10) If the power connector or the connector of the power cable becomes dirty or dusty, wipe it with a dry cloth. Otherwise, this can lead to fire.

**[Caution]**

(1) Do not place this product in a location that is subject to heavy vibration, or on an unstable surface such as an inclined surface. The product may fall off or fall over, causing injuries.

(2) When moving the product, be sure to turn off the power and disconnect all the cables. While moving the product, watch your step. The product may be dropped or fall, leading to injuries or electric shock.

(3) Before disconnecting cables from the product, be sure to turn off the power. Be sure to hold the connector when disconnecting cables. Pulling a cable with excessive force may cause the core of the cable to be exposed or break the cable, and this can lead to fire or electric shock.

(4) This product should be moved by two or more persons. If one person attempts to carry this product alone, he/she may be injured.

(5) This product contains glass. The glass may break, causing injuries, if shock, vibration, heat, or distortion is applied to the product.

(6) The temperature of the glass surface of the display may rise to 50 °C or more depending on the conditions of use. If you touch the glass inadvertently, you may be burned.

(7) Do not poke or strike the glass surface of the display with a hard object. The glass may break or be scratched. If the glass breaks, you may be injured.

(8) If the glass surface of the display breaks or is scratched, do not touch the broken pieces or the scratches with bare hands. You may be injured.

(10) Do not place an object on the glass surface of the display. The glass may break or be scratched.

**2. Cautions on Design**

(1) This product may be damaged if it is subject to excessive stresses (such as excessive voltage, current, or temperature). The absolute maximum ratings specify the limits of these stresses, and system design must ensure that none of the absolute maximum ratings are exceeded.

(2) The recommended operating conditions are conditions in which the normal operation of this product is guaranteed. All the rated values of the electrical specifications are guaranteed within these conditions. Always use the product within the range of the recommended operating conditions. Otherwise, the reliability of the product may be degraded. Use of the product with a combination of parameters, conditions, or logic not specified in the specifications of this product is not guaranteed. If intending to use the product in such a way, be sure to consult NEC in advance.

(3) This product emits near infrared rays (800 to 1000 nm) that may cause the remote controllers of other electric products to malfunction. To avoid this, use an infrared absorption filter and thoroughly evaluate the system and environment.

(4) This product uses high-voltage switching and a high-speed clock. A system using this product should be designed so that it does not affect the other systems, and should be thoroughly evaluated.

(5) This product has a glass display surface. Design your system so that excessive shock and load are not applied to the glass. Exercise care that the vent at the corner of the glass panel is not damaged. If the glass panel or vent is damaged, the product is inoperable.

(6) There are some exposed components on the rear panel of this product. Touching these components may cause an electric shock.

(7) This product uses a high voltage. Design your system so that any residual voltage in this product is dissipated quickly when power is turned off, observing the specifications.

(8) This product uses heat-emitting components. Take the heat emitted by these components into consideration when designing your system. If the product is used outside the specified temperature range, it may malfunction.

(9) This product uses a high voltage and, because of its compact design, components are densely mounted on the circuit boards. If dust collects on these components, it can cause short-circuiting between the pins of the components and moisture can cause the insulation between the components to break down, causing the product to malfunction.

(10) Regulations and standards on safety and electromagnetic interference differ depending on the country. Design your system in compliance with the regulations and standards of the country for which your system is intended.

(11) To obtain approval under certain safety standards (such as UL and EN), a filter that passes a shock test must be fitted over the glass surface of the finished product. In addition, it must be confirmed that the level of UV emissions is within the range specified by such standards.

(12) If this product is used as a display board to display a static image, image “burn-in” occurs. This means that the luminance of areas of the display that remain lit for a long time drops compared with the luminance of areas that are lit for a shorter time, causing uneven luminance across the display. The degree to which this occurs is in proportion to the luminance at which the display is used. To prevent this phenomenon, therefore, avoid static images as much as possible and design your system so that it is used at a low luminance, by setting PLE to the maximum level (PSC = 31).

(13) Within the guarantee period, general faults that occur due to defects in components such as ICs will be rectified by NEC without charge. However, faults due to “burn-in” are not included because such faults can be avoided by using the product correctly. Repairs due to the other faults may be charged for depending on responsibility for the faults.

(14) This product is designed to NEC’s “Standard” quality grade. If you wish to use the product for applications outside the scope of the “Standard” grade, be sure to consult NEC in advance to assess the technological feasibility before starting to design your system.

### 3. Cautions on Use

(1) Because this product uses a high voltage, connecting or disconnecting the connectors while power is supplied to the product may cause malfunctioning. Never connect or disconnect the connectors while the power is on. Immediately after power has been turned off, a residual voltage remains in the product. Be sure to confirm that the voltage has dropped to a sufficiently low level.
(2) Watching the display for a long time can tire the eyes. Take a break at appropriate intervals.
(3) Do not cover or wrap the product with a cloth or other covering while power is supplied to the product.
(4) Before turning on power to the product, check the wiring of the product and confirm that the supply voltage is within the rated voltage range. If the wiring is wrong or if a voltage outside the rated range is applied, the product may malfunction or be damaged.
(5) Do not store this product in a location where temperature and humidity are high. This may cause the product to malfunction. Because this product uses a discharge phenomenon, it may take time to light (operation may be delayed) when the product is used after it has been stored for a long time. In this case, it is recommended to light all cells for about 2 hours (aging).
(6) If the glass surface of the display becomes dirty, wipe it with a soft cloth moistened with a neutral detergent. Do not use acidic or alkaline liquids, or organic solvents.
(7) This product is made from various materials such as glass, metal, and plastic. When discarding it, be sure to contact a professional waste disposal operator.

### 4. REPAIR AND MAINTENANCE

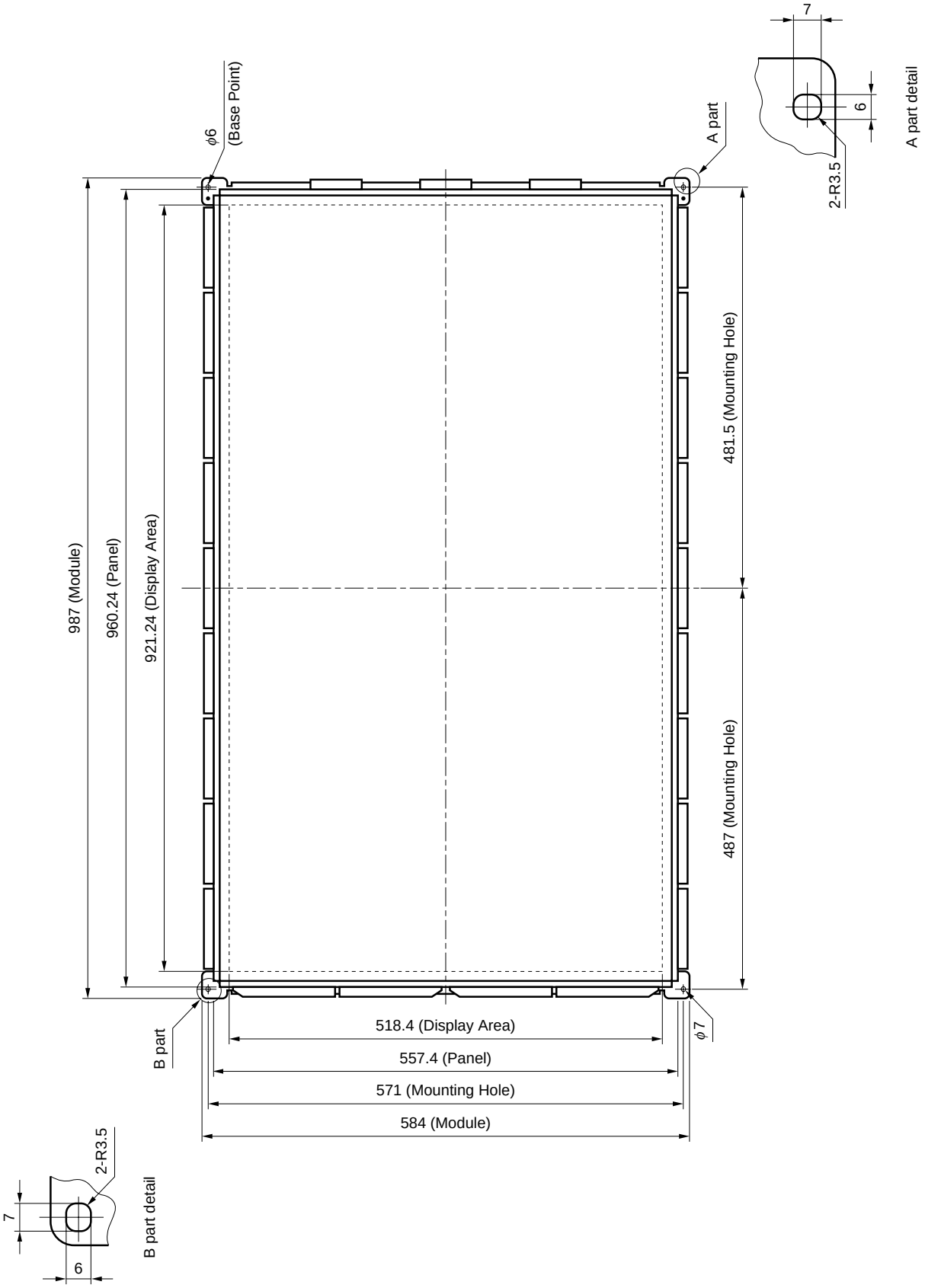
Because this product combines the display panel and driver circuits in a single module, it cannot be repaired or maintained at users' office or plant. Arrangements for maintenance and repair will be determined later.

### 5. OTHERS

(1) If your system requires the user to observe any particular precautions, in addition to the above warnings and cautions, include such caution and warning statements in the manual for your system.
(2) If you have any questions concerning design, such as on housing, storage, or operating environment, consult NEC in advance.

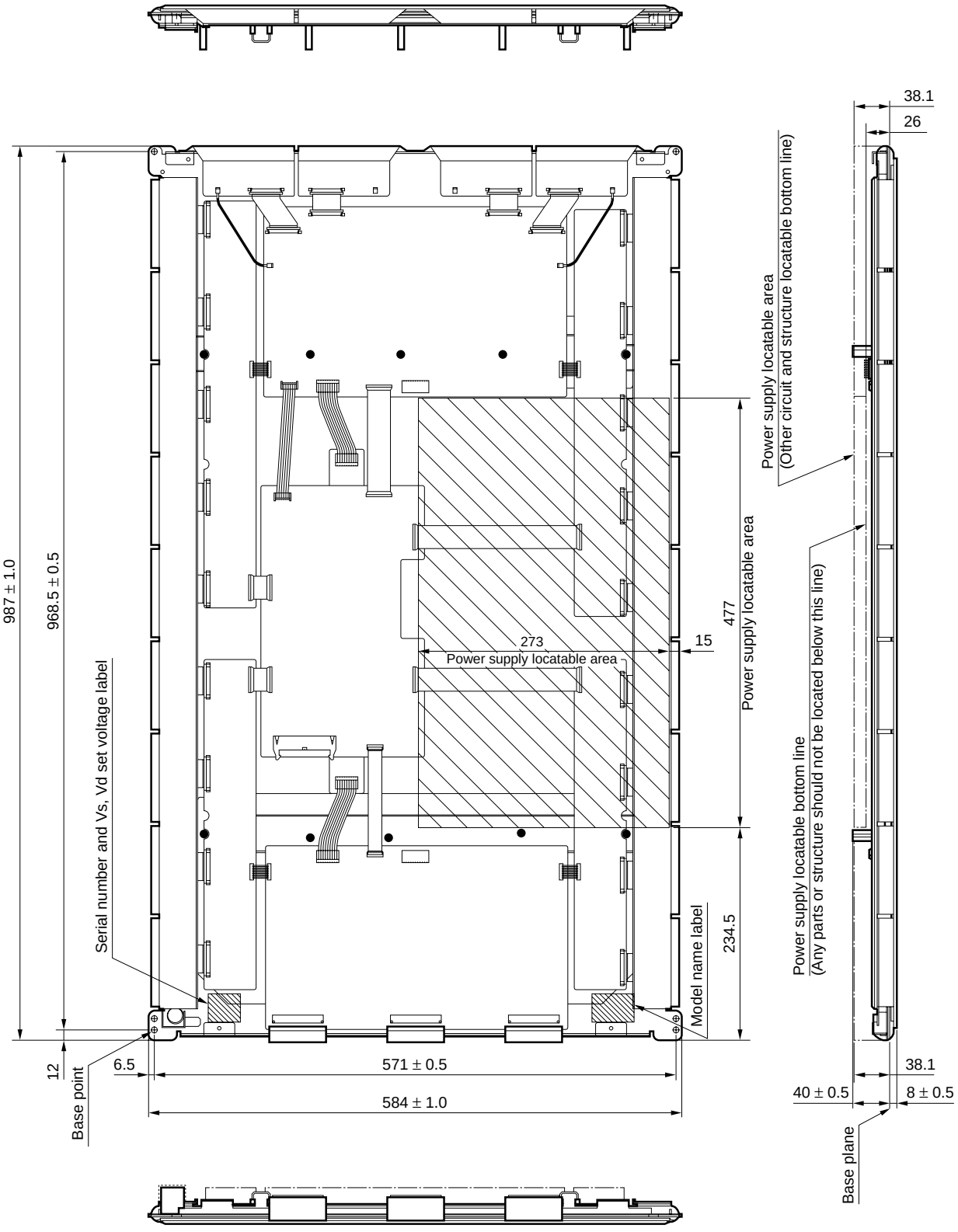
**MECHANICAL DRAWING (Unit: mm)**

**FRONT VIEW**



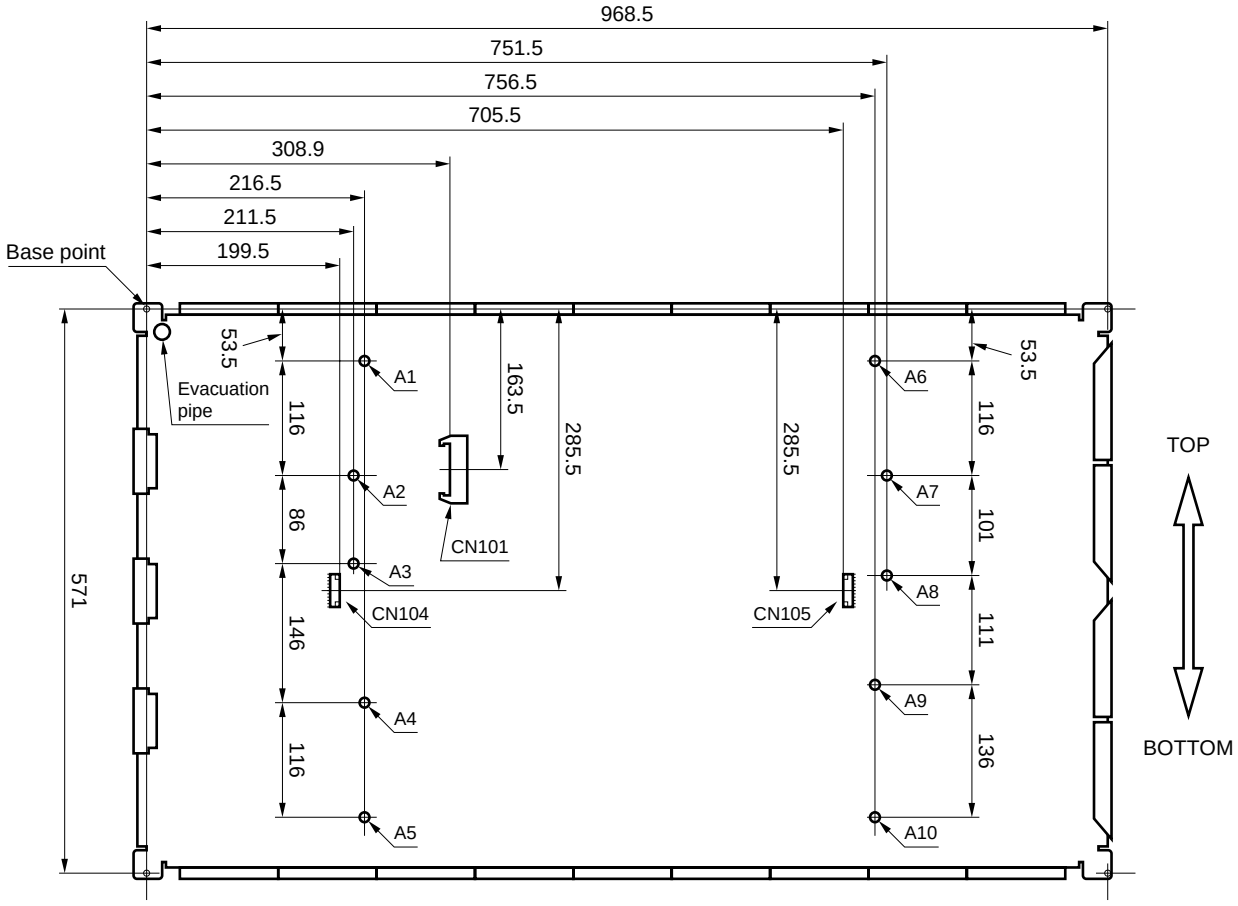
**MECHANICAL DRAWING (Unit: mm)**

**REAR VIEW**

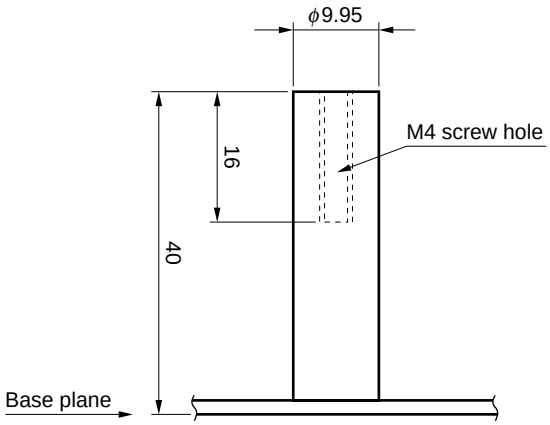


**STUDS POSITION (Unit: mm)**

**REAR VIEW**




**SHAPE OF STUDS A1 - A10 (Unit: mm)**



**[MEMO]**