NEC

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NP42B1MF03 Data Sheet

106 cm (42 type), Wide screen (853 x 480 Pixels), Digital Module
Digital RGB signal, 8bits signal each

DESCRIPTION

The NP42B1MF03 is a 42-inch wide color plasma display module with a resolution of 853(H)x480(V) pixels. The display offers vibrant colors we reproduced in a thin and low profile package. This device uses AC plasma technology by NEC and includes an 8-bit of digital video signal interface for each RGB color.

FEATURES

- O Applied Capsulated Color Filter (CCF) technology, developed at NEC, which offers a high quality image match for CRT display. To offer remarkably pure colors, the color plasma display panel uses extremely clear, thin capsulated color filters to cut unnecessary light as the plasma discharges.
- O Peak luminance of 500cd/m^2 (typical value) is achieved through a new driving method, which offers extremely vivid image with good contrast.
- O Applied Peak Luminance Enhancement (PLE) function that enables the display to operate with the ideal contrast. The PLE function makes it possible to adjust the average luminance level of the PDP display automatically in accordance with the average luminance level of an input video signal.

APPLICATIONS

- O Wide Screen TV (aspect ratio 16:9)
- O Public Information Display
- O Video Conference Systems
- O Retail
- O Education and Training Systems

The information in this document is subject to change without notice.

STRUCTURE AND PRINCIPLE OPERATION OF PLASMA DISPLAY

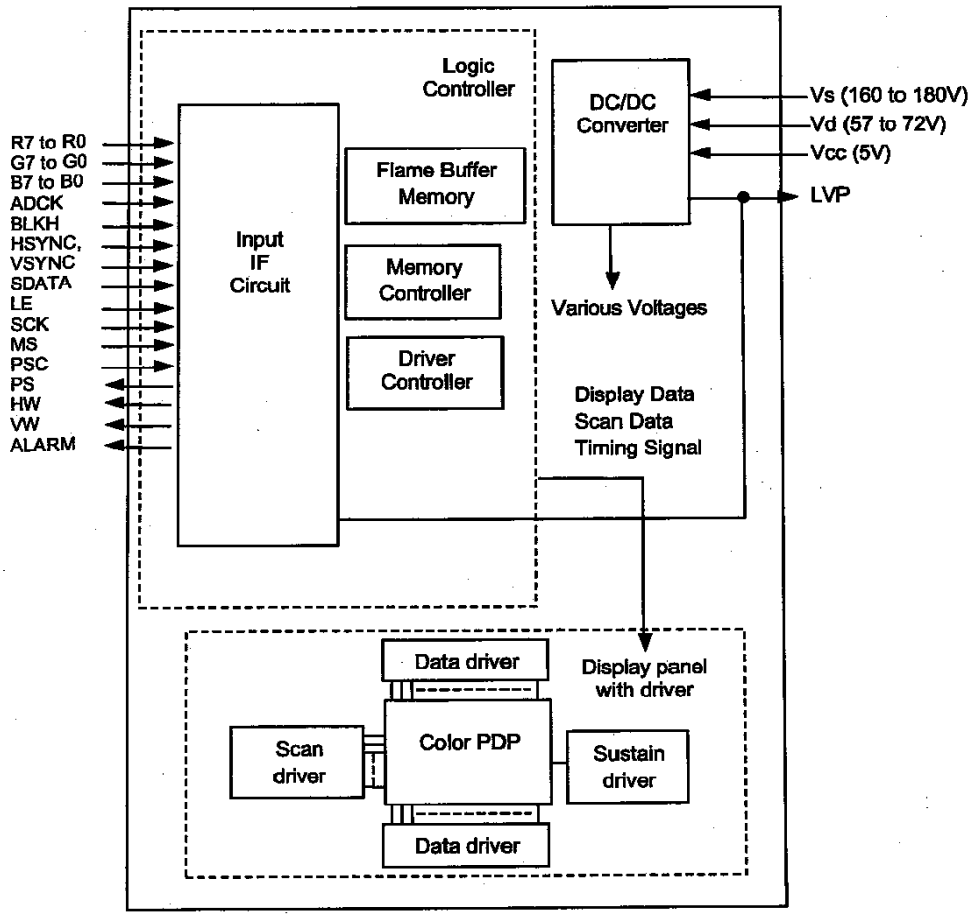
In a Plasma Display Panel, Row and Column electrodes are placed between two glass substrates. A rare gas is then filled between each substrate. When a high voltage is applied to these electrodes, the gas is activated resulting in the radiation of ultraviolet light, similar to the operation in fluorescent lamps. These ultraviolet rays then activate phosphor that has been coated on the inside of the glass substrate, and visible light is emitted from the panel.

ELECTRICAL INTERFACE OF PLASMA DISPLAY

NP42B1MF03 requires 8 bits of digital video signals for each RGB color. For the signal inputs, parallel interface (semi-compatible with NP4203MF02) is prepared in the module. In addition to the video signals, synchronous signals, mode control signals and 3 different DC voltages are required to operate the display.

This plasma display module has a "PLE" (Peak Luminance Enhancement) function that adjusts the luminance and contrast to the suitable value in accordance with the input video signal level variance, so that images can be displayed with the ideal luminance and contrast.

BASIC CONFIGURATION



GENERAL SPECIFICATION

Display area	921(H) x 518(V) mm
Outline dimensions	987(W) x 584(H) x 48(D) mm
Weight	15 kg
Aspect ratio	16:9
Number of pixels	853(H) x 480(V) (1pixel = 3 RGB cells)
Pixel pitch	1.08 (H) x 1.08(V) mm
Color arrangement	RGB vertical stripes
Number of gradations	256 steps for each RGB
Peak luminance	500cd/m^2 typical (Video signal*, 1/25 white window, PLE** mode set to the maximum)

* Signal of EUTV , fv = 59.94 Hz and fh = 31.47 kHz
** See PLE (Peak Luminance Enhancement) description.

OPERATION ENVIRONMENTAL CONDITIONS

Temperature	0 to 50 °C (with forced-air cooling)
Humidity	20 to 80% RH (without condensation)
Atmospheric pressure	800 to 1100 hPa

STRAGE ENVIRONMENTAL CONDITIONS

Temperature	-20 to 60 °C
Humidity	10 to 90% RH (without condensation)
Atmospheric pressure	700 to 1100 hPa

MECHANICAL TEST CONDITIONS

Vibration (operating)	4.9m/s^2 (0.5 G), 10 to 100 Hz, 3 directions, 10 minutes each
Vibration (non-operating)	4.9m/s^2 (0.5 G), 10 to 100 Hz, 3 directions, 2 hours each

LIFE EXPECTANCY

More than 10,000 hours of continuous operations
(Time when the luminance decreased to half to the initial)

POWER INPUT AND OUTPUT

1) Sustain Power Supply

Table 1. Power Output

Item	Symbol	Condition and Remarks	Min.	Typ.	Max.	Unit
Absolute Maximum	----	--------	----	----	200	V
Voltage	Vs	Dependent on the characteristics of each PDP (Note1)	160	----	180	V
Voltage Stability	----	--------	----	----	±1.0	%
Average Current (Note2)	Is-a	Under normal PLE operation	0.1	----	2.0	A
Average current at inhibited PLE operation (Note 2)	Is-ple	(Reference value) (Note3)	----	----	10	A
Peak Current	Is-peak	--------	----	----	15	A
Voltage Regulation	----	At peak current	----	----	5	V
Ripple and Noise	----	--------	----	----	500	mVp-p

Note1: Voltage should be set to a specified value, which is located on a label attached to the module.
Note2: Average of rippled current.
Note3: See PLE (Peak Luminance Enhancement) description.
Current when PLE is set to maximum luminance level with full white image, or when PLE has a delayed response and image is changed from full black to full white.

2) Data Power Supply

Table 2. Data Power Supply

Item	Symbol	Condition and Remarks	Min.	Typ.	Max.	Unit
Absolute Maximum	----	----	----	----	90	V
Voltage	Vd	Dependent on the characteristics of each PDP (Note1)	57	----	72	V
Voltage Stability	----	----	----	----	±1.5	%
Average Current (Note2)	Id-a	Varied correspondence to the Image	0.005	----	2.0	A
Peak Current	Id-peak	----	----	----	5	A
Ripple and Noise	----	----	----	----	300	mVp-p

Note1: Voltage should be set to a specified value, which is located on a label attached to the module.
Note2: Average of rippled current.

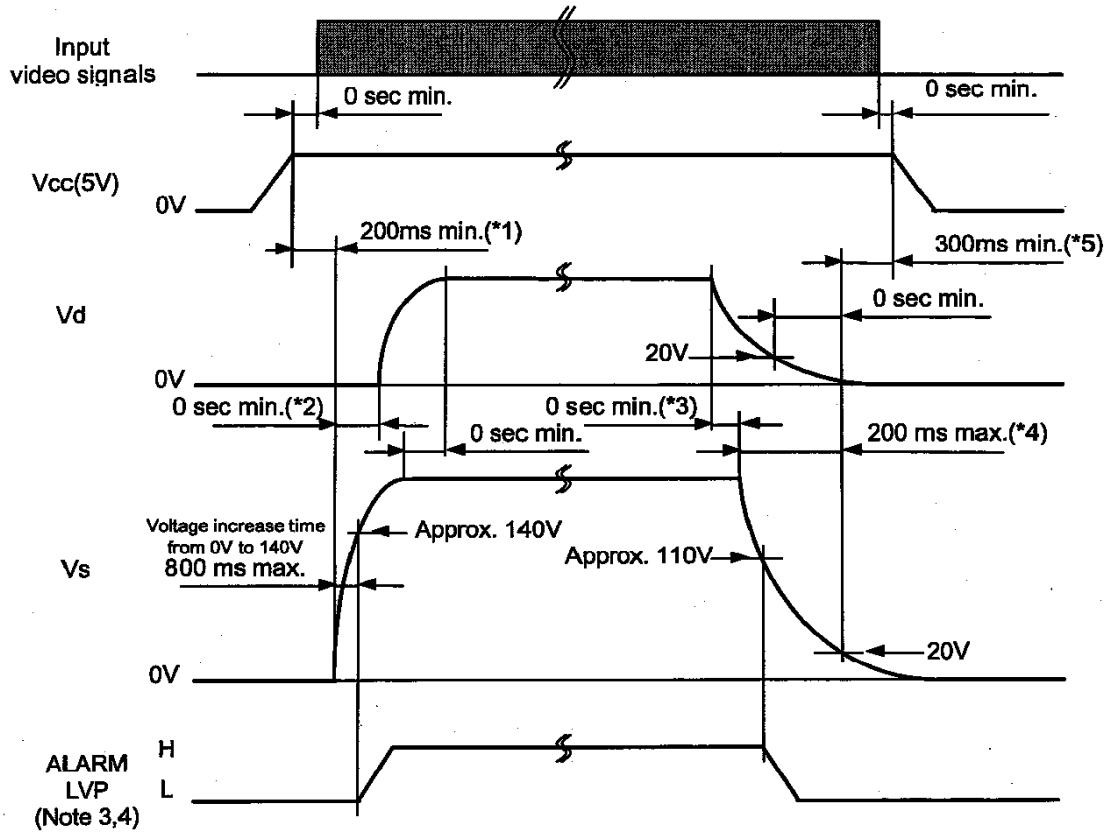
3) Logic Power Supply

Table 3. Logic Power Supply

Item	Symbol	Condition and Remarks	Min.	Typ.	Max.	Unit
Absolute Maximum	—	———	4.5	----	6.0	V
Voltage Range	Vcc	———	4.75	5.0	5.25	V
Current (Note1)	Icc	———	1.0	2.5	3.2	A
Peak Current	Icc-peak	———	—	—	(TBD)	A
Ripple	—	———	—	—	30	mVp-p
Noise	—	———	—	—	300	mVp-p

Note1: Average of rippled current.
This module provides an automatic operation-stop function for internal malfunctions. When the module stops the operation, logic current may reduce to almost zero (0). Even if logic current becomes zero, applied voltage should be kept to less than 6.0 volts.

Supply Voltage and Signal Sequence



Note 1: Power ON/OFF sequence is as follows (refer to the above sequence diagram):
Power ON sequence:
Vcc ON→ 200ms min.(*1) → Vs ON → 0sec min.(*2) → Vd ON
Power OFF sequence:
Vd OFF→ 0sec min. (*3) → Vs OFF → 200ms max.(*4) → 300ms min.(*5) → Vcc OFF
(Caution)
If power sequence does not meet to above sequence diagram, PDP drivers may have a permanent damage.
In order to decrease Vs and Vd voltages quickly to satisfy above sequence diagram, forced discharge circuits are essential in the power supply.

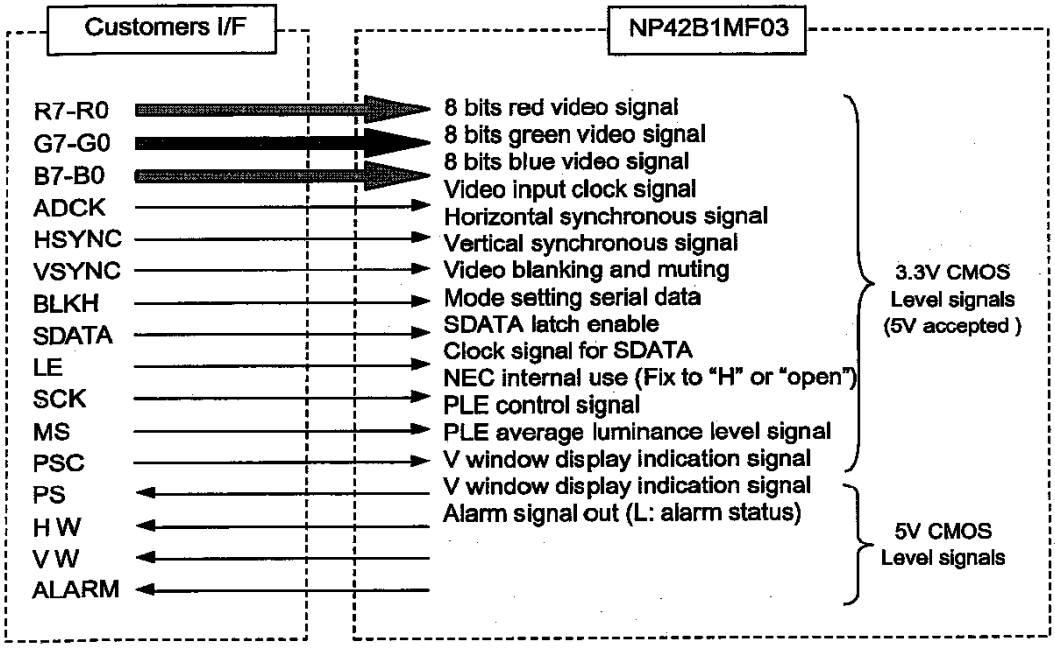
Note 2: The power source for the Input signal circuit and Vcc can be switched on and off at the same time.

Note 3: LVP is the power supply shutdown output signal when the panel is broken and/or failure of internal power source in the PDP module.

Note 4: When the ALARM and LVP signals are "L" High voltage should be shut down. However, when Vcc is applied at first, ALARM and LVP signals are kept "L" until Vs is applied. In order to enable "high voltage power supply" operation, the initial ALARM and LVP signals' status "L" should be disregarded.

INTERFACE SIGNAL

PARALLEL INTERFACE CONFIGURATION



ELECTRICAL CHARACTERISTICS

1) Interface Signals; Absolute Ratings

Common conditions: Ta=25°C, Vcc=5V

Table 4. Absolute Ratings

Item		Parameter	Symbol	Ratings	Unit
Input Signals	R7 to R0, G7 to G0, B7 to B0, ADCK, HSYNC, VSYNC, PSC3 to PSC0, PSCL, BLKH, LE, SCK, SDATA, PSCLL, PSC3L, PSC4L	Input Voltage	V_i	-0.5 to 6.0	V
		Input current	I_i	±20	mA
Output Signals	HW, VW, PS3 to PS0, PSL, ALARM, LVP, PSLL, PS3L, PS4L	Output Voltage	V_o	-0.5 to 5.5	V
		Output current	I_o	±25	mA

2) Interface Signals; Electrical Characteristics

Common conditions: Ta=25°C, Vcc=5V

Table 5. Electrical Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High Level Input Voltage	V_{IH}	----	2.0	----	----	V
Low Level Input Voltage	V_{IL}	----	----	----	0.8	V
Input Current	I_i	V_i=V_{cc} or GND	----	----	±60	μA
High Level Output Voltage	V_{OH}	I_o= -20μA	4.4	----	----	V
Low Level Output Voltage	V_{OL}	I_o=20μA	----	----	0.2	V

SIGNAL FUNCTION

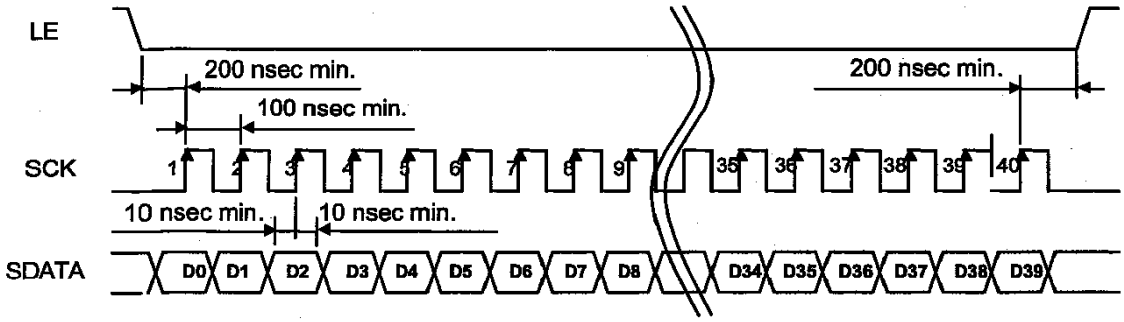
Table 6. Interface Signal Function

Symbol	I/O	Function	(Remarks)
R7 to R0	I	8 bits red video signal (Note 1)	(R7:MSB*, R0: LSB**)
G7 to G0	I	8 bits green video signal (Note 1)	(G7:MSB*, G0:LSB**)
B7 to B0	I	8 bits blue video signal (Note 1)	(B7:MSB*, B0:LSB**)
ADCK	I	Clock for video signal	
HSYNC	I	Horizontal synchronous signal tw=4TADCK min.	(negative pulse)
VSYNC	I	Vertical synchronous signal tw=200ns min.	(negative pulse)
BLKH	I	Video blanking and/or muting (Note 2)	("H" in blanking, muting)
SDATA	I	Mode setting serial data	(total 40bits)
LE	I	SDATA latch enable	(negative logic)
SCK	I	SDATA clock	(latch in positive edge)
PSC3 to PSC0, PSCL	I	PLE control signal	(PSC3:MSB*, PSCL: LSB**)
PSCLL	I	LSB+2 of PSC signal in 256-step PLE operation (LSB of PSC signal in 64-step)	
PS3 to PS0, PSL	O	PLE average luminance level signal	(PS3:MSB*, PSL:LSB**)
PSLL	O	LSB+2 of PS signal in 256-step PLE operation (LSB of PS signal in 64-step)	
PSC3L	I	LSB+1 of PSC signal in 256-step PLE operation	
PSC4L	I	LSB of PSC signal in 256-step PLE operation	
PS3L	O	LSB+1 of PS signal in 256-step PLE operation	
PS4L	O	LSB of PS signal in 256-step PLE operation	
HW	O	H window display period indication signal	("H" in display period)
VW	O	V window display period indication signal	("H" in display period)
ALARM	O	Alarm signal for panel broken and failure of internal power-source. (Note 3)	("L" in alarmed status)

* MSB: Most Significant Bit
** LSB: Least Significant Bit

Note 1: The RGB video signal should be compensated with Inverse?circuit before input to the color plasma display module.
Note 2: While BLKH input is "H" level, all display area image turns to black color display.
Note 3: When ALARM output turns to "L" level, high voltage power input (Sustain power supply: Vs, and Data power supply: Vd) should be switched off immediately. When glass panel is broken, high voltage may occur at the electrode section and cause electric shock. Failure of internal power-source cause over-power status and gives damage to the display panel and driver-circuits.

Set-up of control mode signals and display position



Set-up Sequence:

1. Set LE to "L" level.
2. Enter the 40 bits of SDATA into the module synchronizing to the serial clock signal (SCK)
3. Set LE to "H" level.

Note 1: SCK clock rate: 1MHz max.

Note 2: Serial input data should be refreshed at least in every 5 or 6 seconds or less.

Note 3: Serial input data (SDATA) is latched into the module at the falling edge of the VSYNC signal after "LE" signal is returned back to "H" level. When VSYNC is overlapped with the "LE" signal's "L" period, the serial data is latched with the next VSYNC timing.

Note 4: When only 40 SCK clocks are entered while LE is "L" level period, SDATA become enable. If SCK clocks number is not 40, SDATA is not refreshed.

Note 5: When powers are supplied to the module, serial data in the module has vague status. Therefore serial data should be refreshed after powered on.

Mode setting signal

Table 7. Contents of SDATA (Mode setting parallel input data)

Data	Signal name	Function	
D0	VIDEOH	Switch for "Video mode" and "PC mode"	H: Video mode, L: PC mode
D1	LIFEH	Switch for PLE luminance control level	L: PLE normal operation H: Fix PLE to low luminance level for longer life operation.
D2	---	NEC internal use	Fix to "L" level
D3	SELFPLEH	Switch for "Internal PLE control" and "External PLE control"	H: Internal PLE control. L: External PLE control
D4	TSELB	Switch for ADCK data latch timing	H: Falling edge, L: Rising edge
D5	FV2	Vertical frequency selection	(Hz) 50 56-64 66 67-71 72-75 FV2 L L L L H FV1 L L H H L FV0 L H L H L
D6	FV1		
D7	FV0		
D8	DISPLINE0	Display lines number	L: 400 lines, H: 480 lines
D9	DISPDOT0	Display Pixel numbers/line	L: 640 pixels/line (Normal display mode), H: 853 pixels/line (Full display mode)
D10	VDELAY (Spare bit)	Fix to "L" level	
D11	VDELAY256	Vertical display start position Refer to the "Dv" in the table 8	Set the display start line number after falling edge of VSYNC. Range of setting line number: 0 to 511
D12	VDELAY128		
D13	VDELAY64		
D14	VDELAY32		
D15	VDELAY16		
D16	VDELAY8		
D17	VDELAY4		
D18	VDELAY2		
D19	VDELAY1		
D20	HDELAY (Spare bit)	Fix to "L" level	
D21	HDELAY512	Horizontal display start position Rerer to the "Dh" in the table 8	Set the display start pixel number after falling edge of HSYNC. Range of setting pixels number: 0 to 1023
D22	HDELAY256		
D23	HDELAY128		
D24	HDELAY64		
D25	HDELAY32		
D26	HDELAY16		
D27	HDELAY8		
D28	HDELAY4		
D29	HDELAY2		
D30	HDELAY1		
D31	HPOS3	Setting of horizontal display position in normal mode (640 pixel/line display). Display position is adjustable by 2 pixels step.	Position Left ——— Center ——— Right HPOS3 L L L ..... H..... H H H HPOS2 L L L ..... L ..... H H H HPOS1 L L H ..... L ..... L H H HPOS0 L H L ..... L ..... H L H
D32	HPOS2		
D33	HPOS1		
D34	HPOS0		
D35	MASKLEVEL2	Gray level in blank area (Possible to set 0-24% of white level)	Level(%) 0 1.5 3 6 12 16 19 24 ML2 L L L L H H H H ML1 L L H H L L H H ML0 L H L H L H L H
D36	MASKLEVEL1		
D37	MASKLEVEL0		
D38	Spare bit	Fix to "L" level	
D39	Spare bit	Fix to "L" level	

Example of video signal input and signal timing

Table 8. Relation Between Input Video Signal and Module RGB Signal Input

	Video Signal						RGB Signal													
							Mode Signal			Normal Display Mode (Aspect Ratio 4:3)					Full Display Mode (Aspect Ratio 16:9)					
							Vertical frequency			Recommended dot-clock numbers in one horizontal synchronous signal period (Horiz. freq.: MHz)	Nominal data read start timing after sync. signal		Pixel & line numbers		Recommended dot-clock numbers in one horizontal synchronous signal period (Horiz. freq.: MHz)	Nominal data read start timing after sync. signal		Pixel & line numbers	
	No	Signal Name	Display Resolution (dot line)	Vert Freq. (Hz)	Number of Lines In one Frame	Horiz. Freq. (kHz)	FV2	FV1	FV0		Dv	Dh	DL0	DD0		Dv	Dh	DL0	DD0
Video mode	1	EUTV	853x480	50.0	525	26.25	L	L	L	780 (20.48)	38	128	H	L	1040 (27.3)	38	171	H	H
	2	EDTV	853x480	59.94	525	31.47	L	L	H	780 (24.55)	35	116	H	L	1040 (32.73)	35	154	H	H
	3	HDTV	853x480	60	1125/2	33.75	L	L	H						1054 (35.57)	40	113	H	H
PC mode	4	NEC	640x400	56.4	440	24.83	L	L	H	848 (21.05)	33	149	L	L	1130 (28.06)	33	199	L	H
	5	NEC	640x400	70	449	31.47	L	H	H	800 (25.18)	36	143	L	L	1066 (33.55)	36	191	L	H
	6	IBM	640x400	70	449	31.47	L	H	H	800 (25.18)	36	146	L	L	1066 (33.55)	36	195	L	H
	7	VGA	640x480	59.94	525	31.47	L	L	H	800 (25.18)	35	144	H	L	1066 (33.55)	35	192	H	H
	8	IBM	640x480	59.94	525	31.47	L	L	H	800 (25.18)	27	136	H	L	1066 (33.55)	27	181	H	H
	9	NEC	640x480	59.94	525	31.47	L	L	H	800 (25.18)	39	145	H	L	1066 (33.55)	39	193	H	H
	10	MAC	640x480	66.66	525	35.00	L	H	L	864 (30.24)	42	160	H	L	1152 (40.32)	42	213	H	H
	11	VESA	640x480	72.8	520	37.86	H	L	L	832 (31.5)	31	168	H	L	1109 (42.00)	31	224	H	H
	12	VESA	640x480	75	500	37.5	H	L	L	840 (31.5)	19	184	H	L	1120 (42.00)	19	245	H	H
	13	IBM	640x480	75	525	39.38	H	L	L	800 (31.5)	34	144	H	L	1067 (42.00)	34	192	H	H

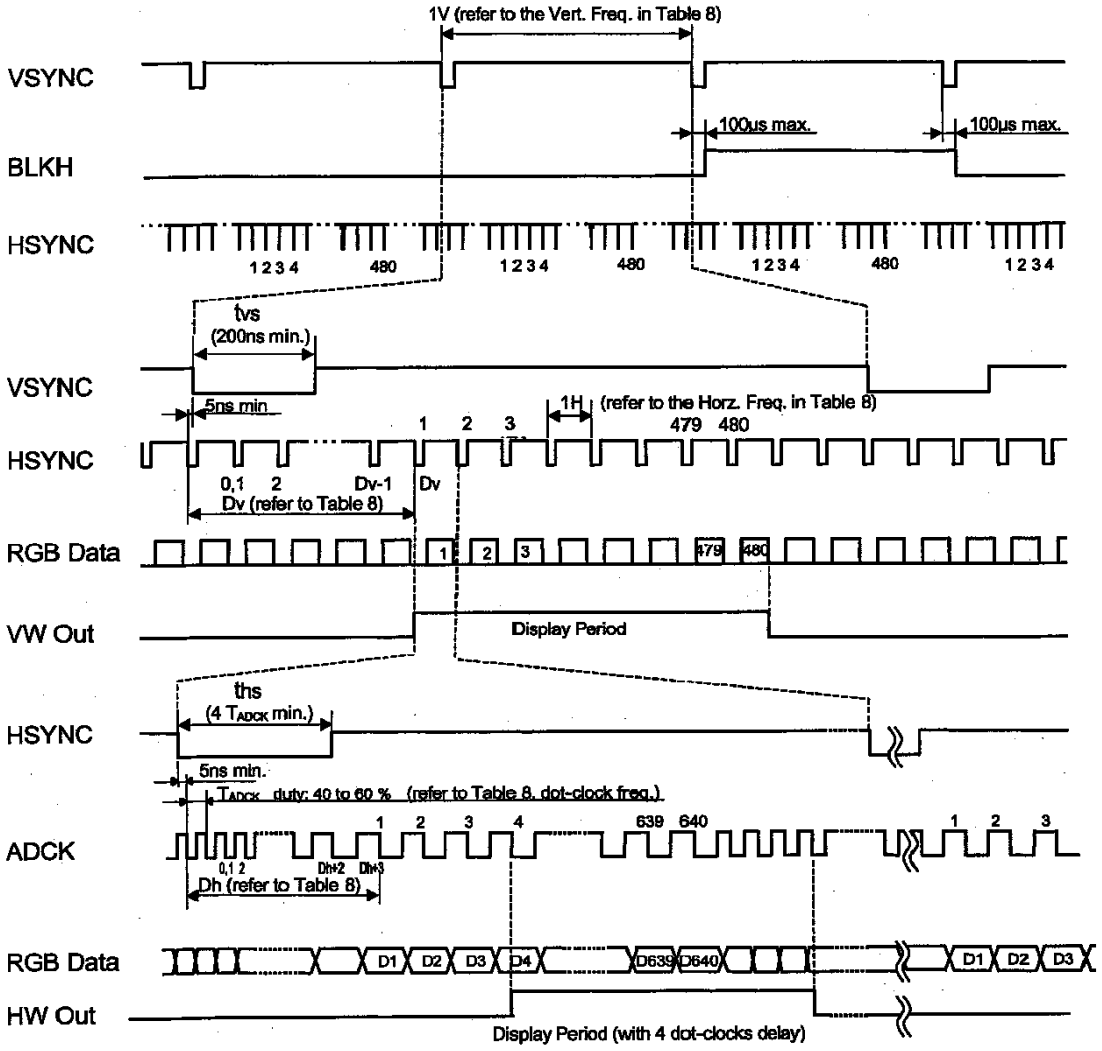
Note 1: Maximum data clock (ADCK) frequency is 50MHz.
Note 2: Maximum horizontal frequency in Video mode is 47 kHz
Note 3: Maximum horizontal frequency in PC mode is 70 kHz
Note 4: Vertical frequency range is 50Hz to 75Hz.
Note 5: D8 (DISPLINE0) and D9 (DISPDOT0) of serial input data should be set correctly according to the display data. If do not correct, PLE function is not operated correctly.
Note 6: When one horizontal signal period is divided equally with the value of above "Recommended dot clock numbers in one horizontal period", the effective display width of the video signal becomes equal with the width of the screen width. When over-scan is required, this value should be adjusted to smaller value.
Note 7: When one horizontal signal period is divided equally with the value of above "Recommended dot clock numbers in one horizontal period", Dv and Dh values in the same row gives the display image position at almost the center of the screen.

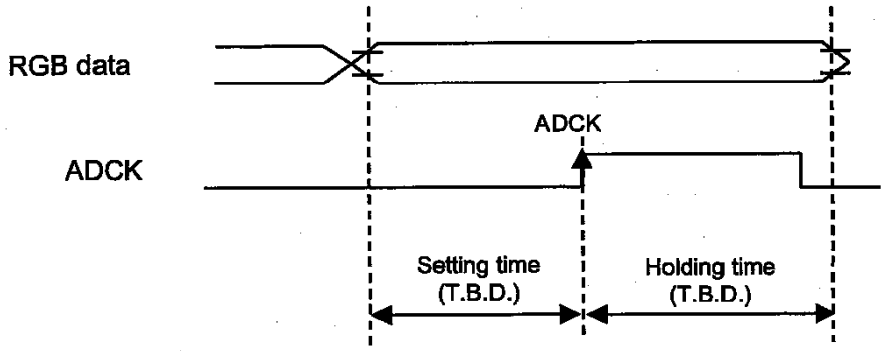
SIGNAL TIMING

Refer to the timing diagram on the following pages.

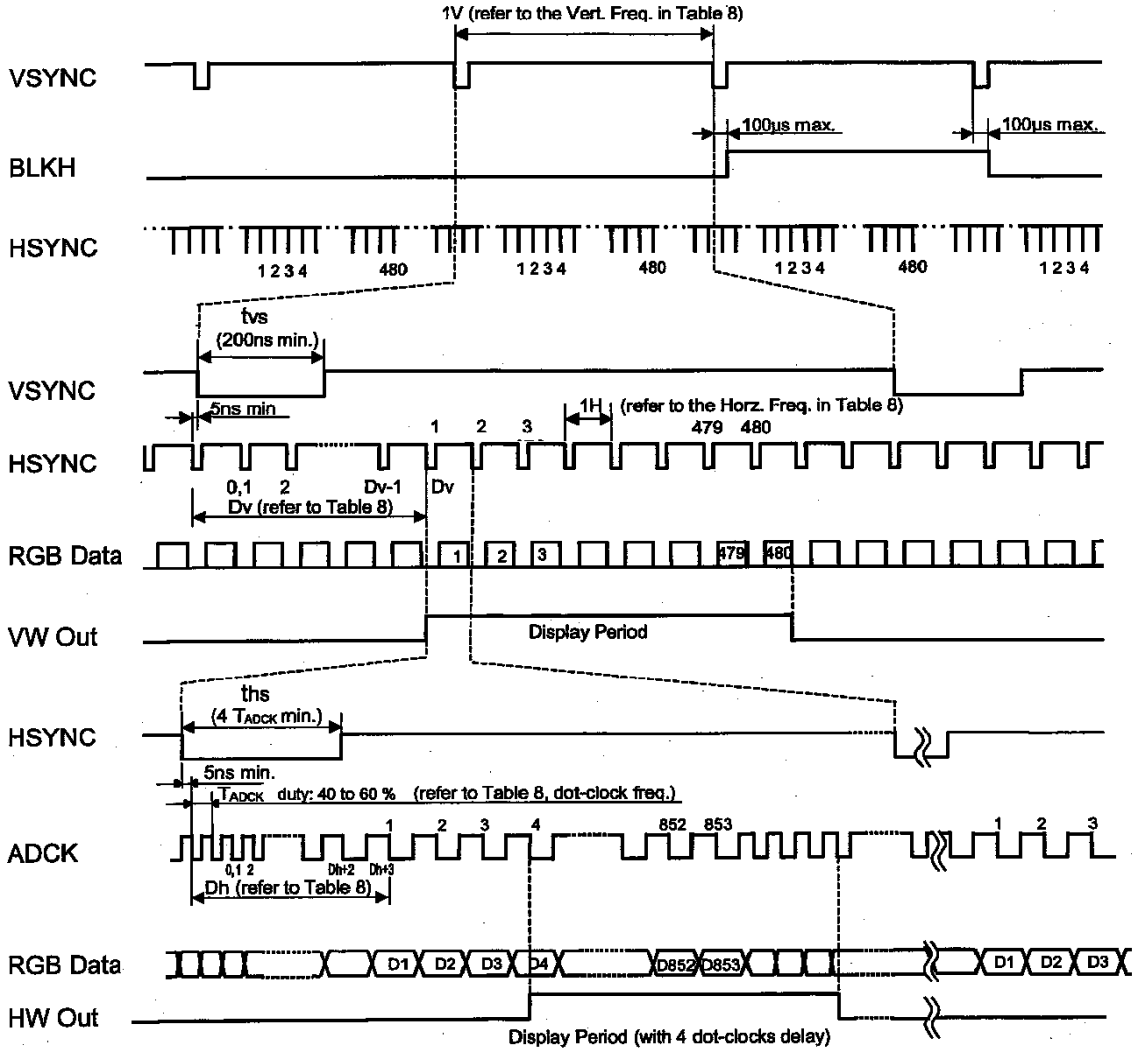
- Input video signal format is determined by Mode signal (refer to Table 8)
- "T_{ADCK}" shows 1 cycle period of ADCK.
- "tvs" shows negative pulse width of VSYNC.
- "tvh" shows negative pulse width of HSYNC.
- "1H" shows 1 cycle period of HSYNC (Horizontal Synchronous Signal).
- "1V" shows 1 cycle period of VSYNC (Vertical Synchronous Signal).
- "Dv" is a period between "leading-edge of the vertical synchronous pulses" and " valid RGB lines data read start timing "
- "Dh" is a period between "leading-edge of the horizontal synchronous pulse" and " valid RGB dots data read start timing "
- In case normal mode (640 dot mode) is selected, both sides are masked with gray patterns.
- In case 400 line is selected, upper 40 lines and lower 40 lines are masked with gray patterns.

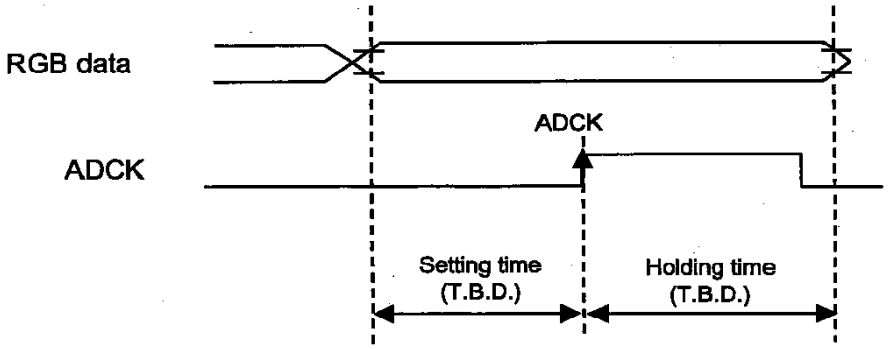
Timing Diagram (Normal Display Mode, 480 lines)





Timing Diagram (Full Display Mode, 480 Lines)

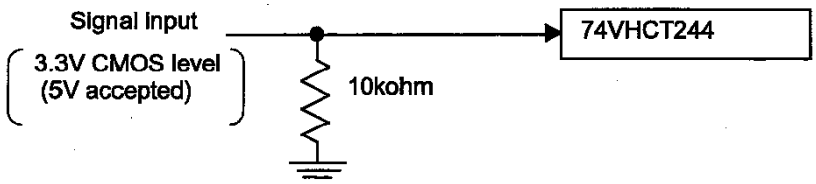




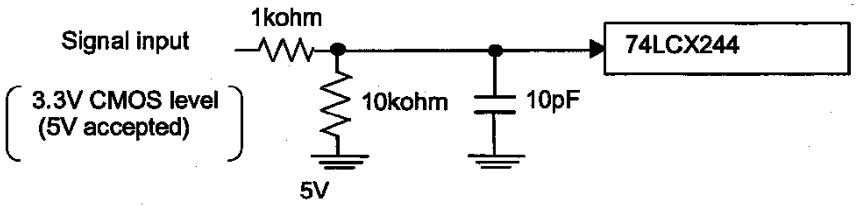
INPUT OUTPUT DRIVE CIRCUIT

Following are definitions of the input and output drive circuits for all interface signals and the PDP module.

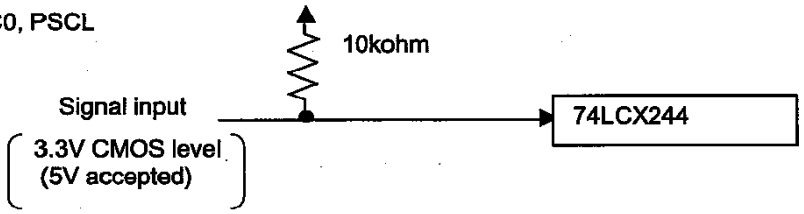
(1) R7-R0, G7-G0, B7-B0, ADCK, HSYNC, VSYNC, BLKH



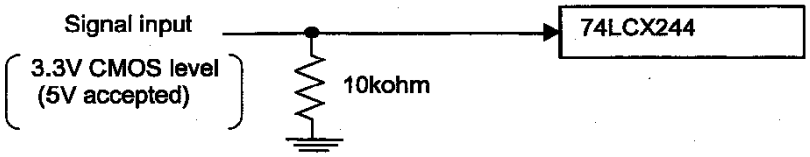
(2) SCK, SDATA, LE



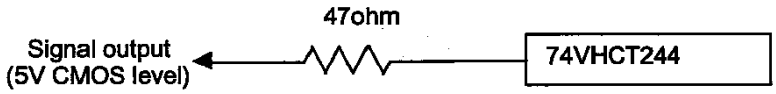
(3) PSC3-PSC0, PSCL



(4) PSCLL
PSC3L
PSC4L

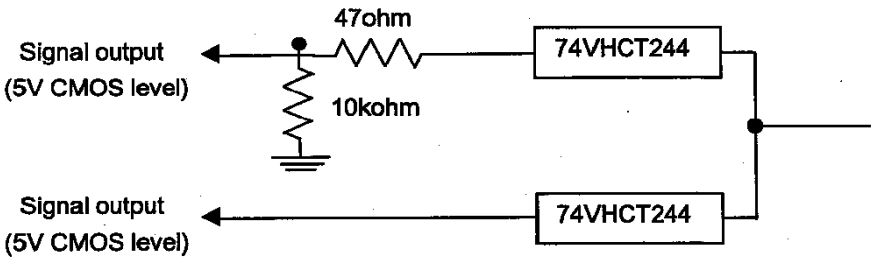


(5) HW ,VW, PS3-PSO, PSL, PSLL
PS3L,PS4L



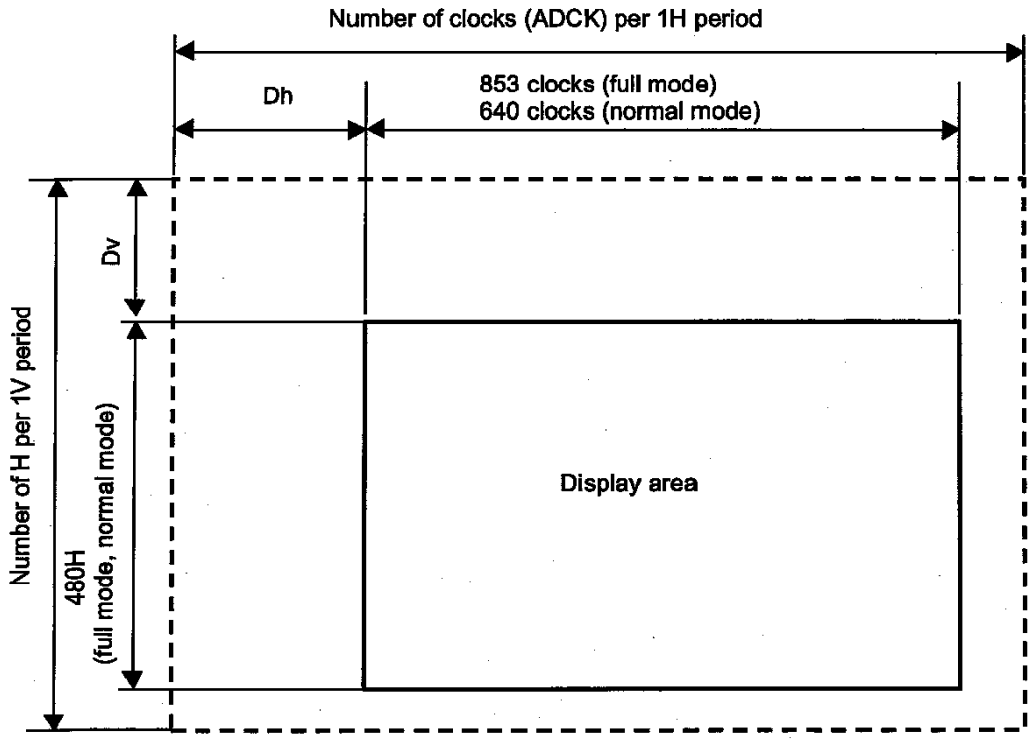
(6) ALARM

(7) LVP



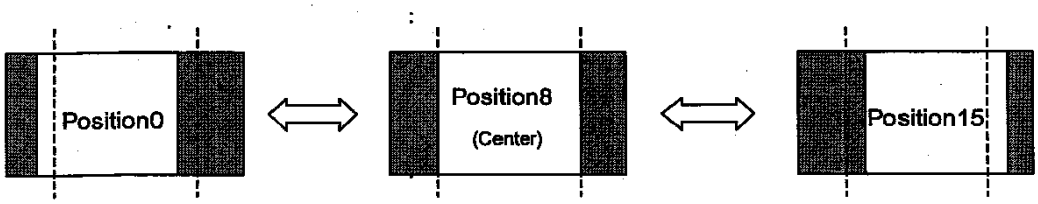
Display position

The relation among Dv, Dh, and the display position is as shown below.



1) Setting range of Dv and Dh
   Dv: 9bit 0-511 line (HSYNC)
   Dh: 10bit 0-1023 dot (ADCK)
2) Limitation of number of clocks per 1H period
   normal mode: (Dh)+2+640 Number of clocks per 1H period 11bit+10bit = 3071
   full mode: (Dh) +2+853 Number of clocks per 1H period 11bit+10bit = 3071
3) Limitation of number of HSYNC pulses per 1V period
   (Dv) +2+480 Number of HSYNC pulses per 1V period 2047 (HSYNC)

Display position setting in normal modes (aspect ratio 4:3)

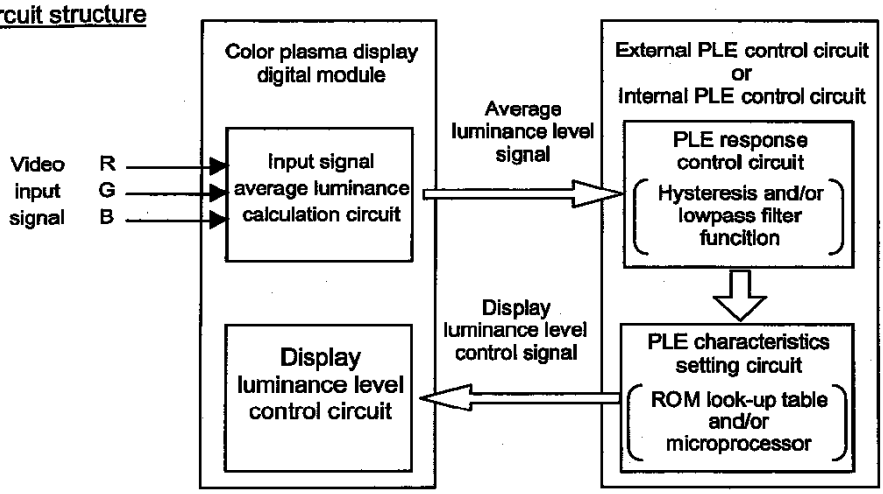


16 positions can be set by 2-pixel pitch through "Mode setting serial data".

PLE (Peak Luminance Enhancement) FUNCTION

The PLE function makes it possible to increase the luminance level of the PDP display when the average luminance level of the input video signal is low. This PLE function reduces the maximum power by absorbing the luminance when the high-power-load-image is displayed, and results in a higher contrast level.

PLE circuit structure



This plasma display module has following two modes. These two modes can be selected by the mode control signal.

1. "Internal PLE" mode --- Built-in PLE function in the PDP module itself. This PLE mode realizes one of the best PLE characteristics without any additional circuit. Therefore this mode is very convenient, and it is recommend to utilize this function actively.

2. "External PLE" mode --- Externally controlled PLE function from the customer's interface circuit. External PLE mode enables to make customer's original characteristics within the limitation range. The PLE characteristics is strongly related not only the luminance characteristics of plasma display module but also the power consumption and the generated heat, therefore it is required to obtain the acknowledgement of NEC concerning the external PLE characteristics to be set at the customer.

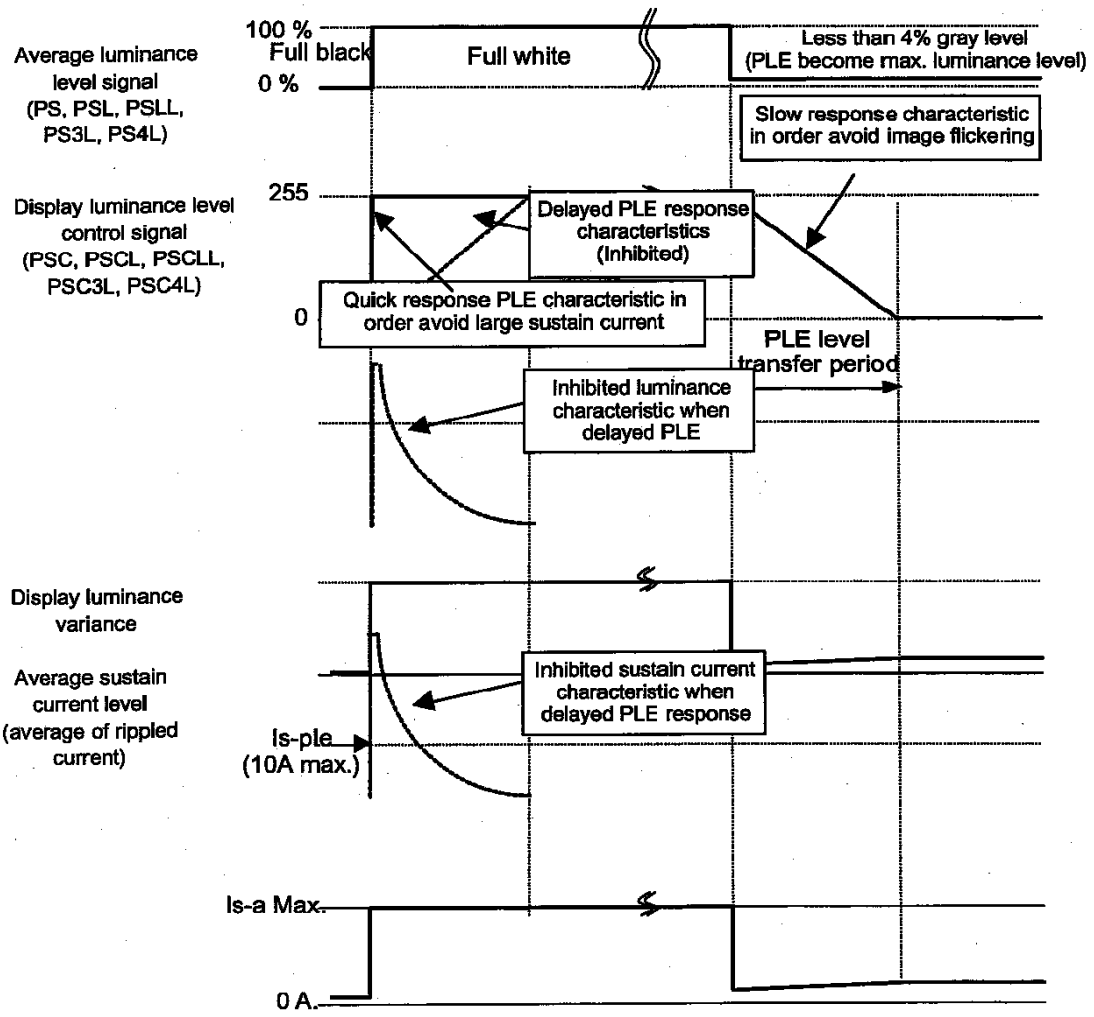
(Caution)
When use the external PLE function, please use within the limitation range. If external PLE characteristic is set outside of the limitation range, plasma display module may have damage. Any trouble caused by this incorrect operation is not included in the warranty

Power consumption and generated heat of plasma display module varies depending on the setting values of PLE characteristic. Therefore the temperature investigation and optimization of cooling design should be done in the state mounted in the plasma display set.

Characteristics of Internal PLE

When PDP module displays full white with maximum luminance, or when PLE characteristic has some delayed response and display image is changed from full black to full white, large sustain current (Is-peak: 10A max.) flows, and plasma display becomes over power status.

In the internal PLE function, when the "Average luminance level" increases, in order to avoid large sustain current flow and over power status, the "Display luminance level" is immediately reduced to the setting level with quick response. And when display load decreases, in order to avoid image flickering caused by the short term average luminance level's fluctuations, the "Display luminance level" is gradually move to the setting level with a slow response characteristic.
(Refer to the following figures)



CONNECTORS PIN ASSIGNMENT
(For the connector position, please refer to the Rear View in the Outline Drawing)

1. POWER INPUT CONNECTORS

Table 9. Connector CN104 Pin Assignment			
Pin No.	Symbol	Pin No.	Symbol
1	LVP	2	GND
3	GND	4	Vcc
5	GND	6	GND
7	Vd	8	N.C.
9	Vs	10	Vs

N.C.: non-connection pin.

Module side connector: B10PS-VH
Mating connector: VHR-10N (housing),
SVH-21T-P1.1(contact)
Connector supplier: J.S.T. TRADING COMPANY., LTD.
Fitting Cable: Equivalent to AWG#20

Table 10. Connector CN105 Pin Assignment			
Pin No.	Symbol	Pin No.	Symbol
1	Vs	2	Vs
3	N.C.	4	Vd
5	GND	6	GND
7	Vcc	8	GND
9	GND	---	---

N.C.: non-connection pin.

Module side connector: B9PS-VH
Mating connector: VHR-9N (housing),
SVH-21T-P1.1 (contact)
Connector supplier: J.S.T. TRADING COMPANY, LTD.
Fitting Cable: Equivalent to AWG#20

(Note): If using a long cable, applied voltage may be dropped because of its resistance.
Specified voltage should be applied correctly at the input of the module side connector.

2. SIGNAL INTERFACE CONNECTOR

80-PIN CONNECTOR

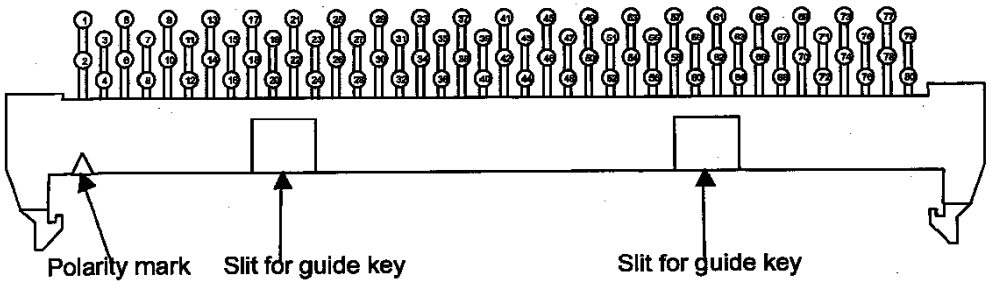
Table 11. Connector CN101 Pin Assignment

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	R7	2	GND	41	B3	42	GND
3	R6	4	GND	43	B2	44	GND
5	R5	6	GND	45	B1	46	GND
7	R4	8	GND	47	B0	48	GND
9	R3	10	GND	49	ADCK	50	GND
11	R2	12	GND	51	HSYNC	52	INV
13	R1	14	GND	53	VSYNC	54	PSL
15	R0	16	GND	55	(Note)	56	(Note)
17	G7	18	GND	57	(Note)	58	(Note)
19	G6	20	GND	59	(Note)	60	(Note)
21	G5	22	GND	61	HW	62	GND
23	G4	24	GND	63	VW	64	PS3
25	G3	26	GND	65	PS2	66	PS1
27	G2	28	GND	67	PS0	68	(Note)
29	G1	30	GND	69	PSC3	70	PSC2
31	G0	32	GND	71	PSC1	72	PSC0
33	B7	34	GND	73	ALARM	74	PSCL
35	B6	36	GND	75	(Note)	76	BLKH
37	B5	38	GND	77	LE	78	SCK
39	B4	40	GND	79	SDATA	80	GND

Note: This terminal must be kept open.

Module side connector: TX3-80P-D2LT-SN1
Mating connector: TX1-80S-D2P1-1D
Connector supplier: Japan Aviation Electronics Industry, Limited (JAE)
Fitting Cable: 80 conductors flat-cable, 0.635mm pitch (equivalent to AWG#30)

TX3-80P-D2LT-SN1 pin numbers (Top view)



ADDITIONAL CONNECTOR FOR 64 STEP PLE

Table12.Connector CN102 Pin Assignment		
Pin No.	Symbol	Function
1	PSLL	LSB of PS signal in 64-step PLE operation
2	PSCLL	LSB of PSC signal in 64-step PLE operation
3	GND	---

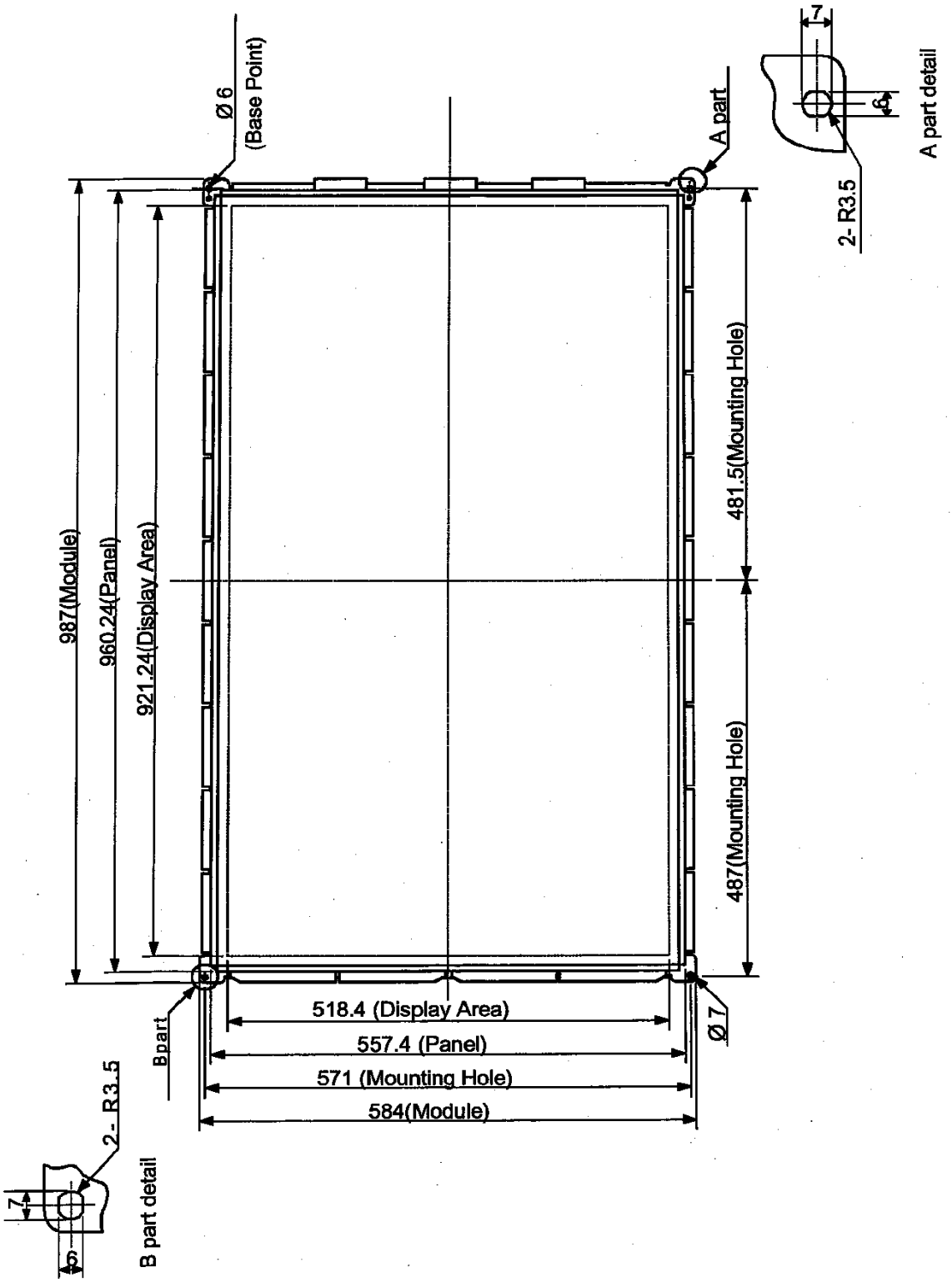
Module side connector : B3B-EH
Mating connector : EHR-3 (housing)
SEH-001T-P0.6 (contact)
Connector supplier : J.S.T. TRADING COMPANY, LTD.
Fitting cable : Equivalent to AWG#22

ADDITIONAL CONNECTOR FOR 256 STEP PLE

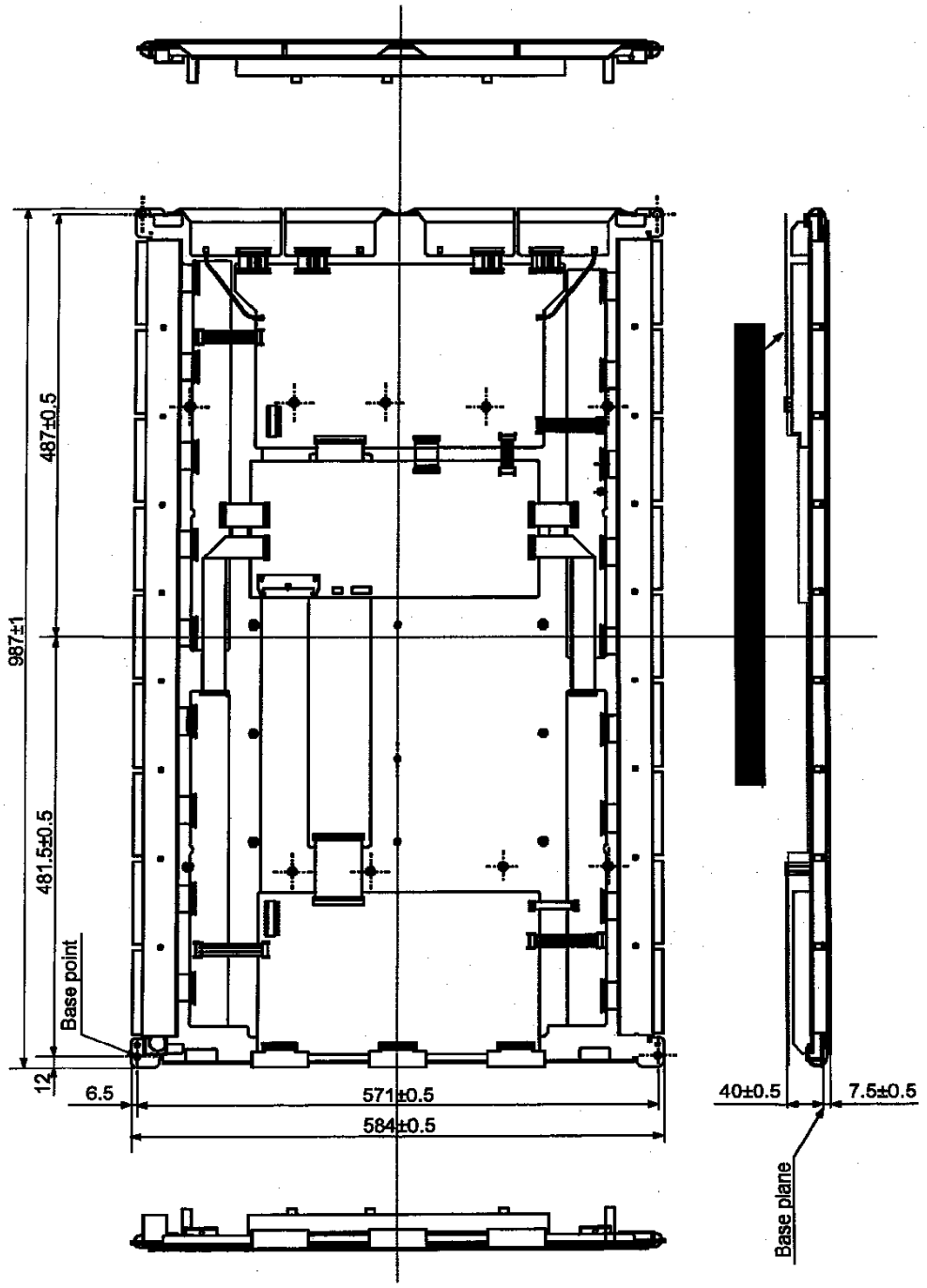
Table13.Connector CN103 Pin Assignment		
Pin No.	Symbol	Function
1	PSLL	LSB+2 of PS signal in 256-step PLE operation
2	PS3L	LSB+1 of PS signal in 256-step PLE operation
3	PS4L	LSB of PS signal in 256-step PLE operation
4	PSCLL	LSB+2 of PSC signal in 256-step PLE operation
5	PSC3L	LSB+1 of PSC signal in 256-step PLE operation
6	PSC4L	LSB of PSC signal in 256-step PLE operation
7	GND	---

Module side connector : B7B-EH
Mating connector : EHR-7 (housing)
SEH-001T-P0.6 (contact)
Connector supplier : J.S.T. TRADING COMPANY, LTD.
Fitting cable : Equivalent to AWG#22

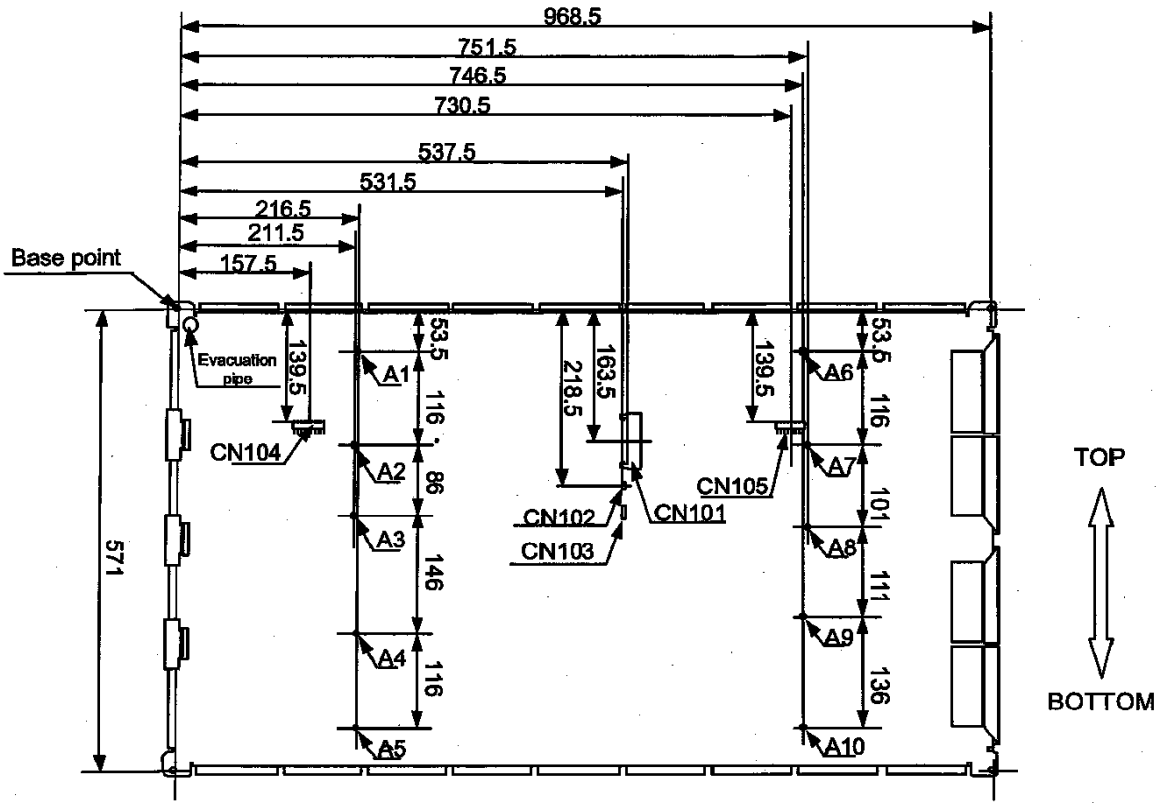
MECHANICAL DRAWING (Unit: mm)
FRONT VIEW



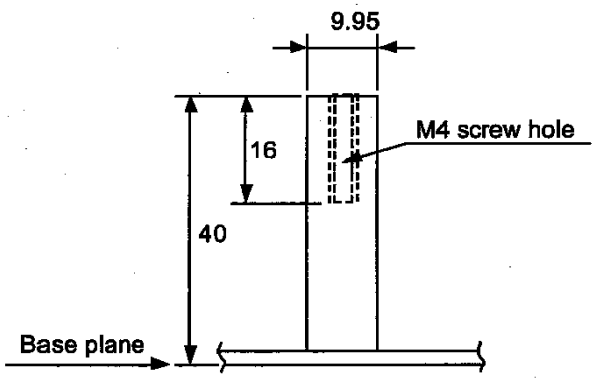
MECHANICAL DRAWING (Unit: mm)
REAR VIEW



STUDS AND CONNECTORS POSITION
REAR VIEW (Unit: mm)



SHAPE OF STUD (Unit: mm)



Locatable position of other parts or structures adjacent to the PDP module
Rear view (Unit: mm)

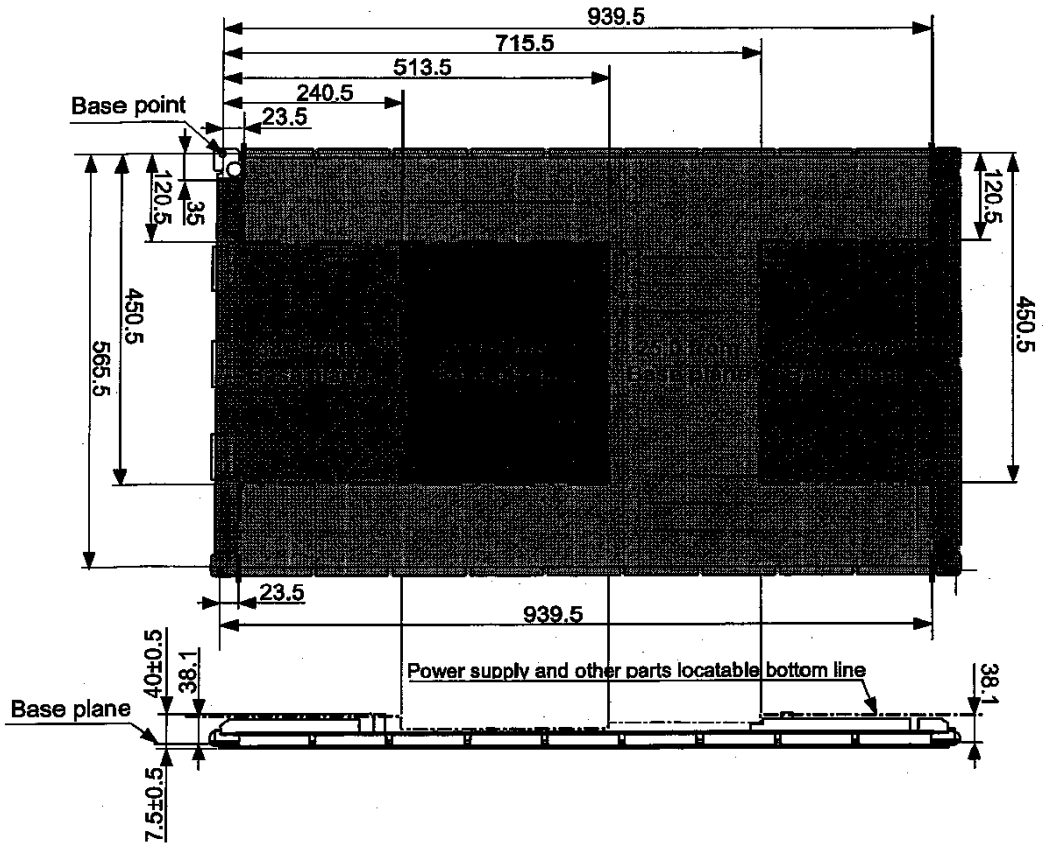


IMAGE STICKING CHARACTERISTICS

1) Image sticking

The fluorescent substance used in the plasma module loses its luminance with the lapse of lighting time.
This deterioration in luminance appears to be a difference in luminance in relation to the surroundings, and comes to be recognized as image sticking.

In other words, the image sticking is defined as follows: when the same pattern (of the fixed display) is displayed for a long time, a difference in luminance is caused around the lighting area and non-lighting area due to deterioration in the fluorescent substance.
When the present pattern is changed over to another one, the boundary comes to be seen between the lighting area and non-lighting area due to difference in luminance in the pattern shown shortly before changeover. If this condition is accumulated, the boundary or image sticking comes to be seen with the naked eyes.

2) Secular change in luminance

The life of luminance, defined as the reduction to half the initial level, is more than 10 thousand hours on average.
Conditions: All white (100% white) input at an ambient temperature of 25 °C.
However, this life time is not a guarantee value for life and luminance. It should be recognized simply as the data for reference.

3) Warranty

Image sticking and faults in luminance and picture elements are excluded from the warranty objects.

4) Cause of deterioration in luminance

A major possible cause of deterioration in luminance is damage in the fluorescent substance due to impact caused by ions generated at the time of plasma discharges.

5) Practical value for Image sticking

The relationship between integrated lighting time and luminance in this plasma module is described in the attached material. In particular, the deterioration in luminance tends to be accelerated up to 100 hours in the initial period. In the initial period, the fixed display of patterns particularly tends to cause image sticking.
The practical value for image sticking is difficult to define in concrete numerals. As described below, you are advised to take proper measures to make the occurrence of image sticking as slow as possible.

6) Proposed measures taken to relieve image sticking

So long as there is the reduction of luminance in the fluorescent substance, it is impossible to avoid the occurrence of image sticking. Therefore, to relieve image sticking, we offer you a method of entering an image input that may ensure reluctance to the generation of the difference in luminance reduction among the displayed dots.

The images from TV broadcasting involve a high rate of motion picture displays.
Therefore, there is less chance of being a cause of difference in luminance reduction among the cells. Even when the fixed patterns are displayed, they generally last for a few minutes.

Since the same pattern is less liable to be displayed, there is almost no influence toward image sticking.

If the fixed patterns tend to be displayed for a long time, however, there occurs a substantial imbalance between the lighting and non-lighting areas, thus causing a difference in luminance as a result. In this document, we offer you some proposals of installation, paying attentions to the two points: the reduction of difference in luminance achieved by integrated lighting time leveling and the method of edge smearing to make image sticking hard to be discerned.

The result from these proposals can, however, greatly depend on the contents of images and the operating environment. Therefore, we consider that it is essential to take the suitable measures in consideration of the customer's operating environment.

Example of Proposal 1: The display position is moved while the fixed display pattern is changed over, or it is scrolled during the display.

Example of Proposal 2: If possible, a pattern of complementary color is incorporated (for integrated time leveling).

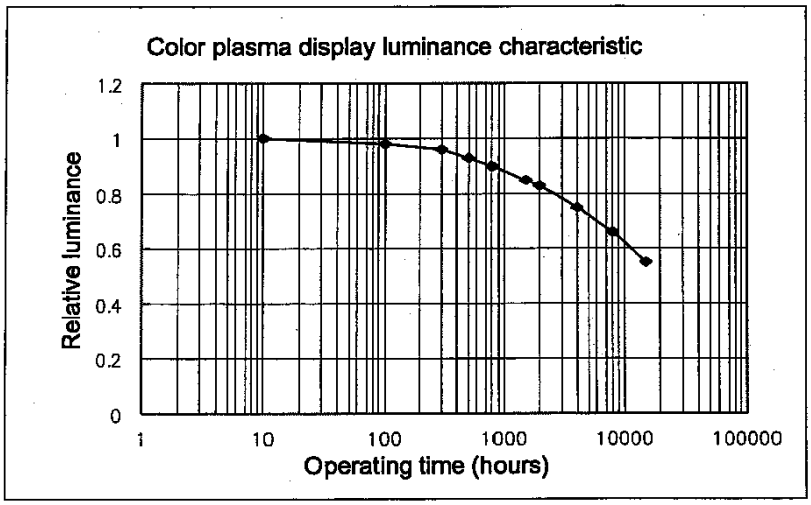
Example of Proposal 3: The fixed pattern and the motion picture display are reciprocally exchanged, in order to minimize the display period of the fixed pattern.

Example of Proposal 4: During operation, the luminance of screen is suppressed as low as possible. For the display patterns, characters are indicated not on the black ground (non-picture area) but on the colored ground (mixture of R, G, B recommended).

7) Proposed countermeasures for the plasma module

Since the PDP is a display that uses a fluorescent substance like the CRT, it is a fundamental phenomenon that image sticking occurs. Unlike the CRT, the PDP gives rise to deterioration in the fluorescent substance due to impact caused by ions generated during plasma display.

As a result of the above-mentioned improvements, it is possible to extend the PDP lifetime and relieve the effect of burning, but is impossible to realize the complete elimination of burning so far as a fixed pattern is displayed for a long time.



1. Warning and Cautions

Warning: Indicates a hazard that can lead to death or injury if the warning is ignored and the product is handled incorrectly.

Caution: Indicates a hazard that can lead to injury or damage to property if the caution is ignored and the product is handled incorrectly

[Warning]

(1) This product uses a high voltage (420V max.). Do not touch the circuitry of this product with your hands when power is supplied to the product or immediately after turning off the power. Be sure to confirm that the voltage has dropped to a sufficiently low level.
(2) Do not supply a voltage higher than that specified to this product. This can damage the product and may cause a fire.
(3) Do not use this product in locations where the humidity is extremely high, where it may be splashed with water, or where it is surrounded by flammable materials. Do not install or use the product in a location that does not satisfy the specified environmental conditions. This can damage the product and may cause a fire.
(4) If a foreign substance (such as water, metal, or liquid) gets inside the product, immediately turn off the power. Continuing to use the product as it is may cause fire or electric shock.
(5) If the product emits smoke, an abnormal smell, or makes an abnormal sound, immediately turn off the power. If nothing is displayed or if the display goes out during use, immediately turn off the power. Continuing to use the product as it is may cause fire or electric shock.
(6) Do not disconnect or connect the connector while power to the product is on. It takes some time for the voltage to drop to a sufficiently low level after the power has been turned off. Confirm that the voltage has dropped to a safe level before disconnecting or connecting the connector. Otherwise, this may cause fire, electric shock, or malfunctioning.
(7) Do not pull out or insert the power cable from/to an outlet with wet hands. Doing so may cause electric shock.
(8) Do not damage or modify the power cable. Doing so it may cause fire or electric shock.
(9) If the power cable is damaged, or if the connector is loose, do not use the product; otherwise, this can lead to fire or electric shock.
(10) If the power connector or the connector of the power cable becomes dirty or dusty, wipe it with a dry cloth. Otherwise, this can lead to fire.

[Caution]

(1) Do not place this product in a location that is subject to heavy vibration, or on an unstable surface such as an inclined surface. The product may fall off or fall over, causing injuries.
(2) When moving the product, be sure to turn off the power and disconnect all the cables. While moving the product, watch your step. The product may be dropped or fall, leading to injuries or electric shock.
(3) Before disconnecting cables from the product, be sure to turn off the power. Be sure to hold the connector when disconnecting cables. Pulling a cable with excessive force may cause the core of the cable to be exposed or break the cable, and this can lead to fire or electric shock.
(4) This product should be moved by two or more persons. If one person attempts to carry this product alone, he/she may be injured.
(5) This product contains glass. The glass may break, causing injuries, if shock, vibration, heat, or distortion is applied to the product.
(6) The temperature of the glass surface of the display may rise to 80°C or more depending on the conditions of use. If you touch the glass inadvertently, you may be burned.
(7) Do not poke or strike the glass surface of the display with a hard object. The glass may break or be scratched. If the glass breaks, you may be injured.
(8) If the glass surface of the display breaks or is scratched, do not touch the broken pieces or the scratches with bare hands. You may be injured.
(9) Do not place an object on the glass surface of the display. The glass may break or be scratched.

2. Cautions on Design

(1) This product may be damaged if it is subject to excessive stresses (such as excessive voltage, current, or temperature). The absolute maximum ratings specify the limits of these stresses, and system design must ensure that none of the absolute maximum ratings are exceeded.

(2) The recommended operating conditions are conditions in which the normal operation of this product is guaranteed. All the rated values of the electrical specifications are guaranteed within these conditions. Always use the product within the range of the recommended operating conditions. Otherwise, the reliability of the product may be degraded. Use of the product with a combination of parameters, conditions, or logic not specified in the specifications of this product is not guaranteed. If intending to use the product in such a way, be sure to consult NEC in advance.

(3) This product emits near infrared rays (700 to 1100 nm) that may cause the remote controllers of other electric products to malfunction. To avoid this, use an infrared absorption filter and thoroughly evaluate the system and environment.

(4) This product uses high-voltage switching and a high-speed clock. A system using this product should be designed so that it does not affect the other systems, and should be thoroughly evaluated.

(5) This product has a glass display surface. Design your system so that excessive shock and load are not applied to the glass. Exercise care that the vent at the corner of the glass panel is not damaged. If the glass panel or vent is damaged, the product is inoperable.

(6) There are some exposed components on the rear panel of this product. Touching these components may cause an electric shock.

(7) This product uses a high voltage. Design your system so that any residual voltage in this product is dissipated quickly when power is turned off, observing the specifications.

(8) This product uses heat-emitting components. Take the heat emitted by these components into consideration when designing your system. If the product is used outside the specified temperature range, it may malfunction.

(9) This product uses a high voltage and, because of its compact design, components are densely mounted on the circuit boards. If dust collects on these components, it can cause short-circuiting between the pins of the components and moisture can cause the insulation between the components to break down, causing the product to malfunction.

(10) Regulations and standards on safety and electromagnetic interference differ depending on the country. Design your system in compliance with the regulations and standards of the country for which your system is intended.

(11) To obtain approval under certain safety standards (such as UL and EN), a filter that passes a shock test must be fitted over the glass surface of the finished product. In addition, it must be confirmed that the level of UV emissions is within the range specified by such standards.

(12) If this product is used as a display board to display a static image, "image sticking" occurs. This means that the luminance of areas of the display that remain lit for a long time drops compared with the luminance of areas that are lit for a shorter time, causing uneven luminance across the display. The degree to which this occurs is in proportion to the luminance at which the display is used. To prevent this phenomenon, therefore, avoid static images as much as possible and design your system so that it is used at a low luminance, by setting PLE to the maximum level.

(13) Within the warranty period, general faults that occur due to defects in components such as ICs will be rectified by NEC without charge. **However, IMAGE STICKING is not included in the warranty.** Repairs due to the other faults may be charged for depending on responsibility for the faults.

(14) This product is designed to NEC's "Standard" quality grade. If you wish to use the product for applications outside the scope of the "Standard" grade, be sure to consult NEC in advance to assess the technological feasibility before starting to design your system.

3. Cautions on Use

(1) Because this product uses a high voltage, connecting or disconnecting the connectors while power is supplied to the product may cause malfunctioning. Never connect or disconnect the connectors while the power is on. Immediately after power has been turned off, a residual voltage remains in the product. Be sure to confirm that the voltage has dropped to a sufficiently low level.
(2) Watching the display for a long time can tire the eyes. Take a break at appropriate intervals.
(3) Do not cover or wrap the product with a cloth or other covering while power is supplied to the product.
(4) Before turning on power to the product, check the wiring of the product and confirm that the supply voltage is within the rated voltage range. If the wiring is wrong or if a voltage outside the rated range is applied, the product may malfunction or be damaged.
(5) Do not store this product in a location where temperature and humidity are high. This may cause the product to malfunction. Because this product uses a discharge phenomenon, it may take time to light (operation may be delayed) when the product is used after it has been stored for a long time. In this case, it is recommended to light all cells for about 2 hours (aging).
(6) If the glass surface of the display becomes dirty, wipe it with a soft cloth moistened with a neutral detergent. Do not use acidic or alkaline liquids, or organic solvents.
(7) This product is made from various materials such as glass, metal, and plastic. When discarding it, be sure to contact a professional waste disposal operator.

4. REPAIR AND MAINTENANCE

Because this product combines the display panel and driver circuits in a single module, it cannot be repaired or maintained at users' office or plant. Arrangements for maintenance and repair will be determined later.

5. OTHERS

(1) If your system requires the user to observe any particular precautions, in addition to the above warnings and cautions, include such caution and warning statements in the manual for your system.
(2) If you have any questions concerning design, such as on housing, storage, or operating environment, consult NEC in advance.

Revise history

Date	Contents	Remarks
June.16, 2000	Issue 1st edition	