NEC

DATA SHEET

COLOR PLASMA DISPLAY MODULE

NP42B2ME01

Preliminary-1

(8th Nov.2001)

COSMOPLASMA

106 cm (42 type), Wide screen (853 x 480 Pixels), Digital Module
Digital RGB signal, 8bits signal each

DESCRIPTION

The NP42B2ME01 is a 42-inch wide color plasma display module with a power supply. And its resolution is 853(H)x480(V) pixels. The display offers vibrant colors we reproduced in a thin and low profile package. This device uses AC plasma technology by NEC and includes an 8-bit of digital video signal interface for each RGB color.

FEATURES

- Applied Capsulated Color Filter (CCF) technology, developed at NEC, which offers a high quality image match for CRT display. To offer remarkably pure colors, the color plasma display panel uses extremely clear, thin capsulated color filters to cut unnecessary light as the plasma discharges.
- Peak luminance of 700cd/m^2 (typical value) is achieved through a new driving method, which offers extremely vivid image with good contrast.
- Applied Peak Luminance Enhancement (PLE) function that enables the display to operate with the ideal contrast. The PLE function makes it possible to adjust the average luminance level of the PDP display automatically in accordance with the average luminance level of an input video signal.

APPLICATIONS

- Wide Screen TV (aspect ratio 16:9)
- Public Information Display
- Video Conference Systems
- Retail
- Education and Training Systems

The information in this document is subject to change without notice.

STRUCTURE AND PRINCIPLE OPERATION OF PLASMA DISPLAY

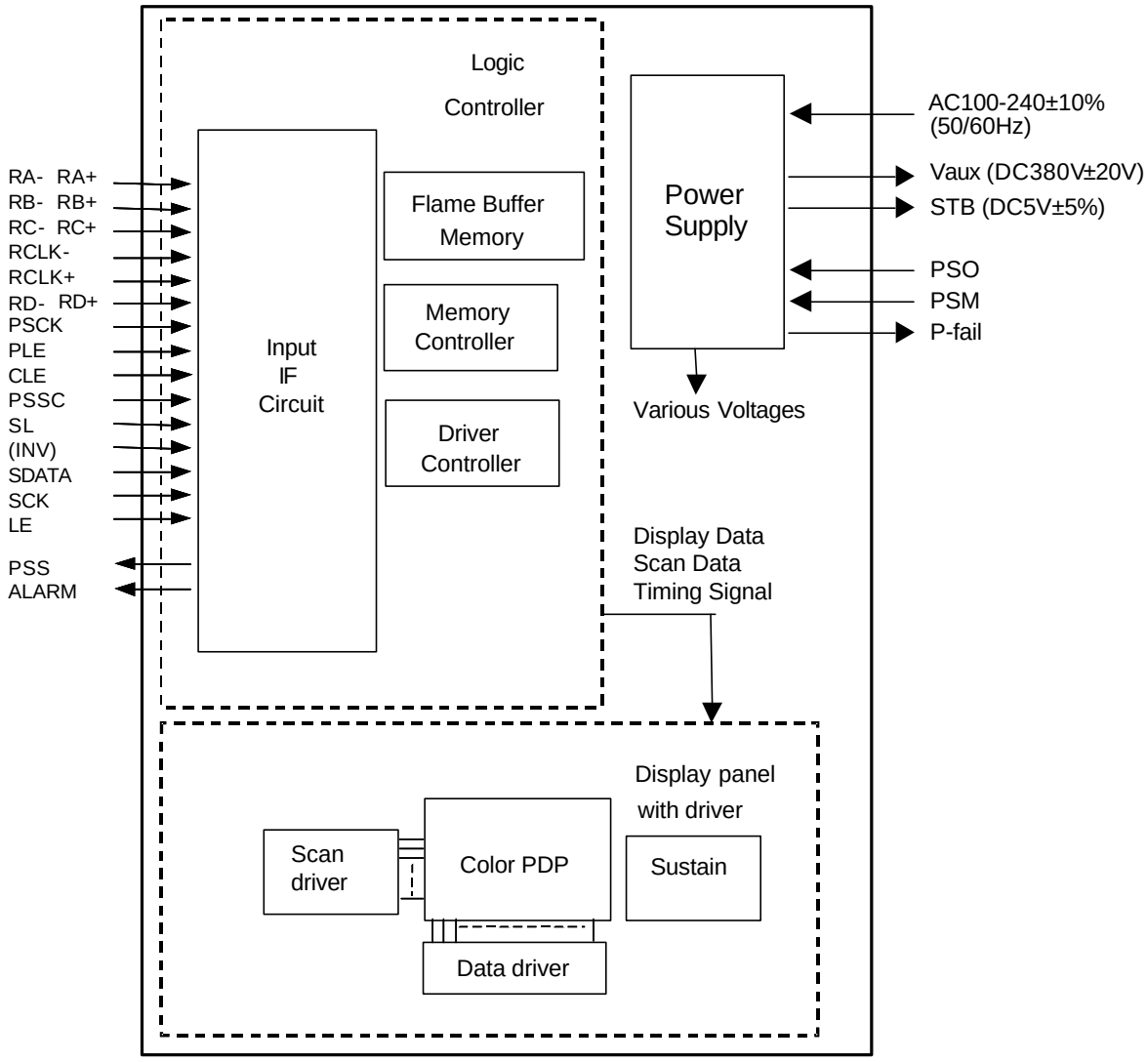
In a Plasma Display Panel, Row and Column electrodes are placed between two glass substrates. A rare gas is then filled between each substrate. When a high voltage is applied to these electrodes, the gas is activated resulting in the radiation of ultraviolet light, similar to the operation in fluorescent lamps. These ultraviolet rays then activate phosphor that has been coated on the inside of the glass substrate, and visible light is emitted from the panel.

ELECTRICAL INTERFACE OF PLASMA DISPLAY

NP42B2ME01 requires 8 bits of digital video signals for each RGB color. For the signal inputs, serial interface (LVDS video signal) is prepared in the module. In addition to the video signals, synchronous signals, mode control signals and AC voltage (100-240V±10%, 50/60Hz) are required to operate the display.

This plasma display module has a "PLE" (Peak Luminance Enhancement) function that adjusts the luminance and contrast to the suitable value in accordance with the input video signal level variance, so that images can be displayed with the ideal luminance and contrast.

BASIC CONFIGURATION



GENERAL SPECIFICATION

Display area	921(H) x 518(V) mm
Outline dimensions	987(W) x 584(H) x 61(D) mm
Weight	17 kg
Aspect ratio	16:9
Number of pixels	853(H) x 480(V) (1pixel = 3 RGB cells)
Pixel pitch	1.08 (H) x 1.08(V) mm
Color arrangement	RGB vertical stripes
Number of gradations	Video 60Hz mode : 8bits(256steps) Video 50Hz mode : 8bits(256steps) / 7bits(128steps) PC mode : 8bits(256steps)
Peak luminance	700cd/m^2 typical Video signal (high luminance mode), 1/25 white window, PLE* mode set to the maximum

* See PLE (Peak Luminance Enhancement) description.

OPERATION ENVIRONMENTAL CONDITIONS

Temperature	0 to 50 °C (with forced-air cooling)
Humidity	20 to 80% RH (without condensation)
Atmospheric pressure	720 to 1100 hPa

STRAGE ENVIRONMENTAL CONDITIONS

Temperature	-20 to 60 °C
Humidity	10 to 90% RH (without condensation)
Atmospheric pressure	700 to 1100 hPa

MECHANICAL TEST CONDITIONS

Vibration (operating)	4.9m/s^2 (0.5 G), 10 to 100 Hz, 3 directions, 10 minutes each
Vibration (non-operating)	4.9m/s^2 (0.5 G), 10 to 100 Hz, 3 directions, 2 hours each

LIFE TIME EXPECTANCY

More than 10,000 hours of continuous operations in full white display mode
(Time when the luminance decreased to half to the initial)

POWER INPUT AND OUTPUT

1) Input voltage

Table1 Input voltage		
Item	Specification	Remarks
Phase No.	Single-phase	
Rated input voltage	AC100V - AC240V	
Input voltage stability range	AC90V - AC254V	
Input frequency	50Hz / 60Hz	
Rush current	less than 50A(o-p)	Except pulse current of input-noise filter
Power consumption	TBD	All area white, Vaux:no loading

2) Output Power for external circuits

Table2 Power Output for external circuits					
Item	Rated voltage (V)	Load current (A)	Voltage stability	Ripple (mVp-p)	Noise (mVp-p)
STB	5	0 to 0.5	±5%	50	400
Vaux	380	0 to 0.15	±20V (Note 1)	20	-

STB : Output signal for a stand-by-circuit in a PDP Set. When AC Power-Input is supplied, STB-Power is always output 5V.

Vaux : DC Power output for external circuit (e.g. Analog Inter-Face Board, etc)

Note 1 : ? In case of transitionally condition as following, Vaux will be variable to 450V max..
*Soon after power is ON
* Soon after resuming from power-service momentary interruption

Note 2 : ? Ripple current is measured connecting a 100 micro F chemical capacitor and a 0.1 micro F film capacitor at the outputs with a 100MHz oscilloscope.

3) Input Signal for Power Supply control

(1) PSO: ON/OFF control signal for following output voltages. (H:ON, L:OFF)
? Vaux (DC Output power for external circuit)
? Vcc (Logic Power Supply for PDP-module)
? Vs, Vd (Driving Power Supply for PDP-module)

(2) PSM: ON/OFF control signal for Vs, Vd, Vcc (H:ON, L:OFF)

Note: ? When both PSO and PSM signals turn to ON, the Power-Supply outputs the voltages (Vs, Vd, Vcc) to the PDP module.

Table3 The relation Input Signal to Output Power						
AC Power Input	PSO	PSM	STB	Vaux	Vs, Vd, Vcc	Remarks
OFF	L	L	OFF	OFF	OFF	
ON	L	L	ON	OFF	OFF	
ON	H	L	ON	ON	OFF	
ON	H	H	ON	ON	ON	
ON	L	H	ON	OFF	OFF	Do not use this mode for safety operation.

Table4 Electrical Characteristics of Input signal for power supply control						
Item	Symbol	MIN	TYP.	MAX	Unit	Remarks
High Level Input Voltage	V_{IH}	3	-	-	V	
Low Level Input Voltage	V_{IL}	-	-	0.5	V	
High Level Input Current	I_{IH}	-	-	0.9	mA	V_I=5V
Low Level Input Current	I_{IL}	-	-	-	-	

4) Output Signal for Power Supply control

P-fail: Detection signal of AC Input voltage OFF and Vaux Output OFF.
When AC Input voltage is OFF or Vaux Output is OFF, P-fail turns to "L" level.

Table5 Electrical Characteristics of Output Signal						
Item	Symbol	MIN.	TYP.	MAX.	Unit	Remarks
High Level Output Voltage	V_{OH}	2.5	-	-	V	I_{OH}=-200uA
Low Level Output Voltage	V_{OL}	-	-	0.45	V	I_{OL}=1mA

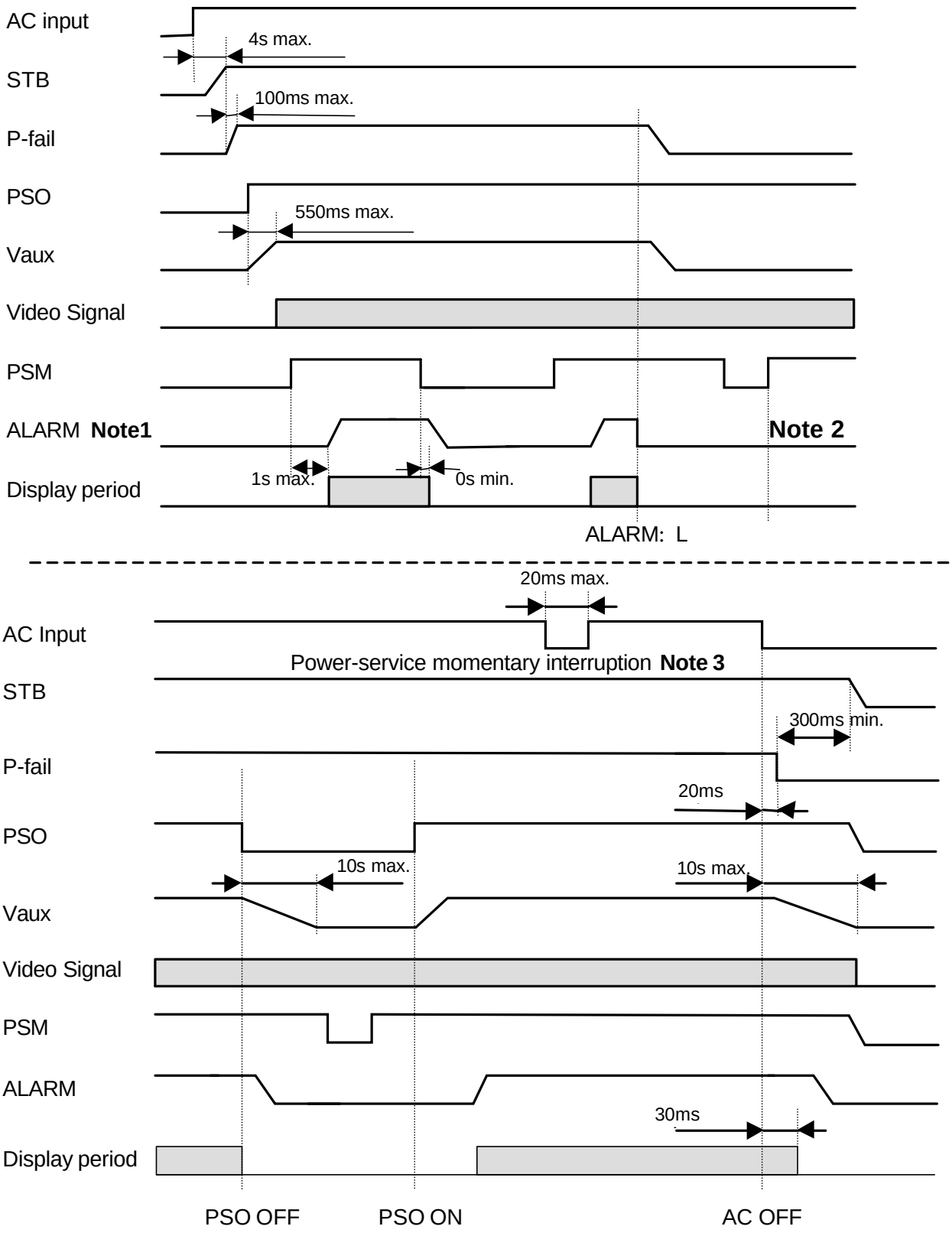
5) POWER SUPPLY ON / OFF SEQUENCE

Refer to the Input-voltage and Output-power sequence on the following page.

Note1: When the panel is broken or the PDP module operates abnormally, the ALARM signal turns to "L" level. However, the ALARM signal is also "L" level before Power-On. Please notice the above issue if ALARM signal will be detected and used for other control in video signal processing circuit

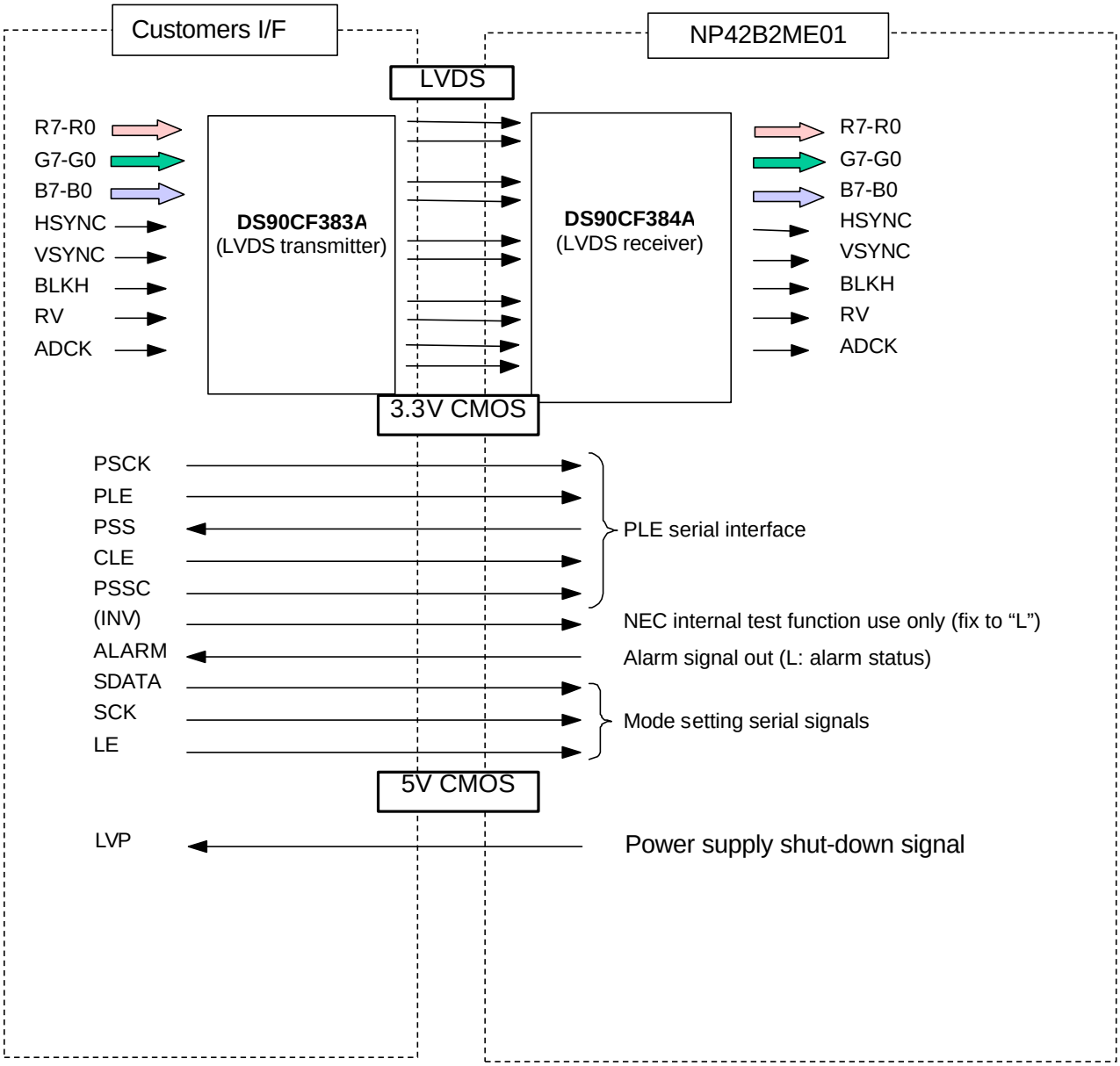
Note2: When the ALARM signal turns to "L" level, power supply shutdowns the PDP operating voltage outputs. After the ALARM signal turns to "L" level, PSM signal can not re-start the Power-supply. In this case, AC power should be re-started from the initial operation step.

Note3: In case of power-service momentary interruption is within 20ms, P-fail signal does not be output. But in case of power-service momentary interruption is over 20ms, P-fail signal will be output. And then the voltages that are supplied to the PDP module would decrease. Therefore, the PDP module will output the ALARM signal and stop the operation of the Power-supply.
(Please refer to AC Input OFF sequence in regard to stop the operation of the Power-supply.)


AC input
4s max.
STB
100ms max.
P-fail
PSO
550ms max.
Vaux
Video Signal
PSM
ALARM Note1
Note 2
Display period
1s max.
0s min.
ALARM: L
20ms max.
AC Input
Power-service momentary interruption Note 3
STB
300ms min.
P-fail
20ms
PSO
10s max.
10s max.
Vaux
Video Signal
PSM
ALARM
30ms
Display period
PSO OFF
PSO ON
AC OFF

INTERFACE SIGNAL

SERIAL INTERFACE CONFIGURATION



ELECTRICAL CHARACTERISTICS

Interface Signals; Absolute Ratings

Common conditions: Ta=25ºC, Vcc=5V

Table 6. Absolute Ratings

Item			Parameter	Symbol	Ratings	Unit
Input Signals	LVDS	RA-, RA+, RB-, RB+, RC-, RC+, RD-, RD+, RCLK-, RCLK+	Input Voltage	Vi	-0.3 to 3.6	V
			Input current	Ii	---	mA
	3.3V CMOS	PSCK, PLE, CLE, PSSC,	Input Voltage	Vi	-0.5 to 4.6	V
			Input current	Ii	-15	mA
Output Signals	3.3V CMOS	PSS, ALARM,	Output Voltage	Vo	-0.5 to 3.5	V
			Output current	Io	±20	mA
	5V CMOS	LVP	Output Voltage	Vo	-0.5 to 5.5	V
			Output current	Io	±35	mA

Interface Signals; Electrical Characteristics

Common conditions: Ta=25ºC, Vcc=5V

Table 7. Electrical Characteristics

Signal	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
LVDS	High Level Input Voltage	V_{TH}	V_{CM}=1.2V	---	---	100	mV
	Low Level Input Voltage	V_{TL}	V_{CM}=1.2V	-100	---	---	mV
	Input Current	I_{IN}	V_{IN}=+2.4/GND	---	---	±10	µA
3.3V CMOS	High Level Input Voltage	V_{IH}	-----	2.0	---	---	V
	Low Level Input Voltage	V_{IL}	-----	---	---	0.8	V
	Input Current	I_i	V_i=V_{cc} or GND	---	---	±5.0	µA
	High Level Output Voltage	V_{OH}	I_o=-1mA	2.4	---	---	V
	Low Level Output Voltage	V_{OL}	I_o=1mA	---	---	0.4	V
5V CMOS	High Level Input Voltage	V_{OH}	I_o=-6mA	4.18	---	---	mV
	Low Level Input Voltage	V_{OL}	I_o=6mA	---	---	0.26	mV

INPUT SIGNAL FUNCTION of LVDS transmitter (DS90CF383A)

Table 8. Interface Signal Function

Symbol	Function	(Remarks)
R7 to R0	8 bits red video signal (Note 1)	(R7: MSB*, R0: LSB**)
G7 to G0	8 bits green video signal (Note 1)	(G7: MSB*, G0: LSB**)
B7 to B0	8 bits blue video signal (Note 1)	(B7: MSB*, B0: LSB**)
ADCK	Clock for video signal	(latch the video signal at falling edge)
HSYNC	Horizontal synchronous signal	Pulse width (ths)=4TADCK min. (negative pulse)
VSYNC	Vertical synchronous signal	Pulse width (tvs)=10TADCK min. (negative pulse)
BLKH	Video blanking and/or muting (Note 2)	("H" in blanking, muting)
RV	Reverse the RGB video data polarity	(Set to "L" level for normal use)

* MSB: Most Significant Bit

** LSB: Least Significant Bit

Note 1: The RGB video signal should be compensated with Inverse?circuit before input to the color plasma display module.

When operate at 7bits(128steps) video data, upper 7bits (R7 to R1, G7 to G1, B7 to B1) are enable.

Note 2: While BLKH input is "H" level, all display area image turns to black color display.

INPUT SIGNAL FUNCTION PDP module (NP42B2ME01)

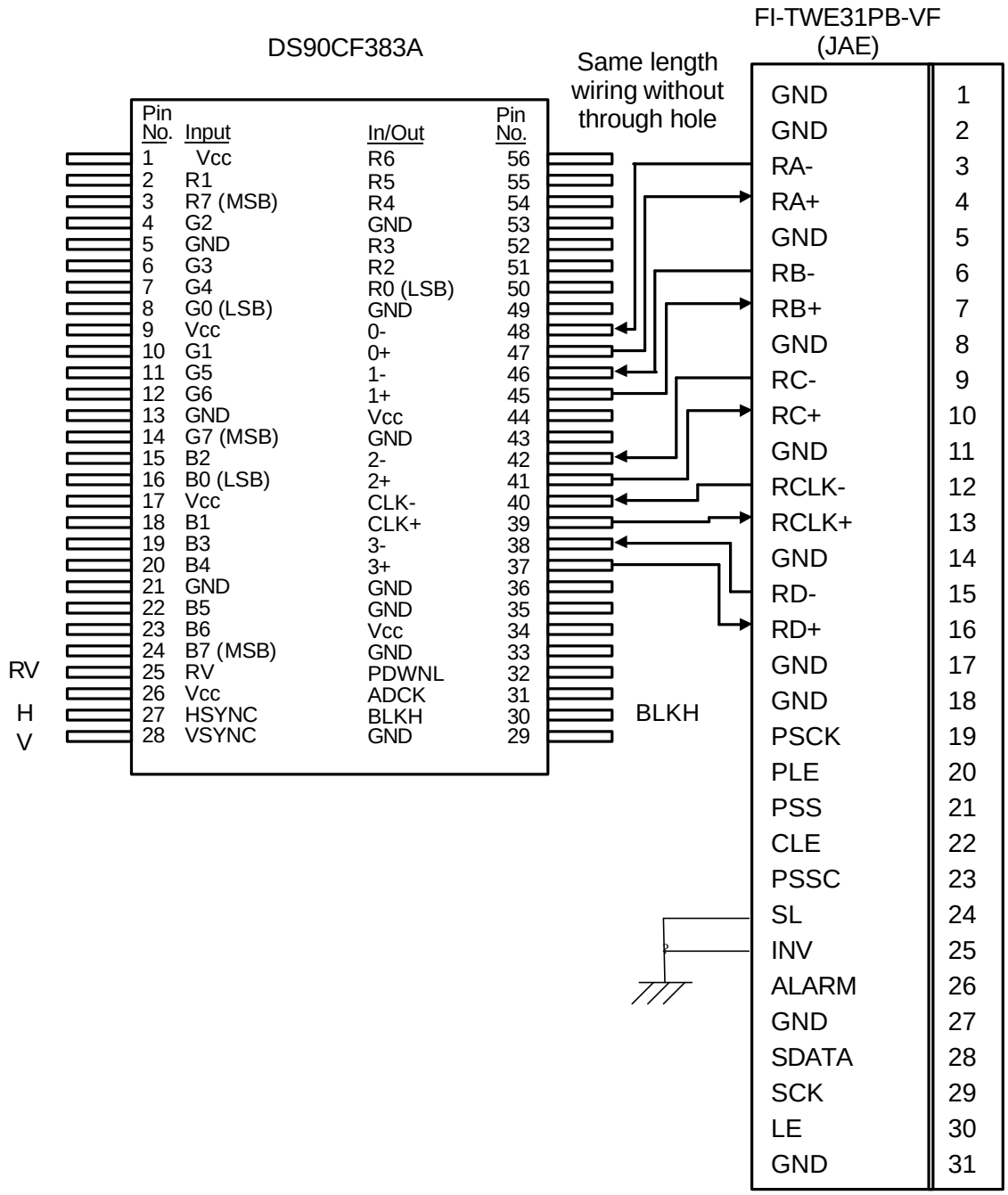
Table 9. Interface Signal Function

Symbol	I/O	Function	(Level)
RA-	I	Video signal input A-	LVDS signal
RA+	I	Video signal input A+	LVDS signal
RB-	I	Video signal input B-	LVDS signal
RB+	I	Video signal input B+	LVDS signal
RC-	I	Video signal input C-	LVDS signal
RC+	I	Video signal input C+	LVDS signal
RD-	I	Video signal input D-	LVDS signal
RD+	I	Video signal input D+	LVDS signal
RCLK-	I	Clock signal clock-	LVDS signal
RCLK+	I	Clock signal clock+	LVDS signal
SDATA	I	Mode setting serial data (48-bit)	3.3V CMOS
SCK	I	Clock signal for SDATA	3.3V CMOS
LE	I	SDATA write enable ("L" in SDATA write)	3.3V CMOS
PSCK (Note 2)	I	Clock signal for PSS, PSSC serial data (latch in positive edge)	3.3V CMOS
PLE (Note 2)	I	PSS data latch enable ("L" in PSS data read)	3.3V CMOS
PSS (Note 2)	O	PLE average luminance signal (10-bit)	3.3V CMOS
CLE (Note 2)	I	PSSC data write enable ("L" in data write)	3.3V CMOS
PSSC (Note 2)	I	PLE luminance control data (8-bit)	3.3V CMOS
INV	I	NEC internal test function use only (Fix to "L")	3.3V CMOS
ALARM	O	Alarm signal for panel broken and failure of internal power-source. (Note 1) ("L" in alarmed status)	3.3V CMOS

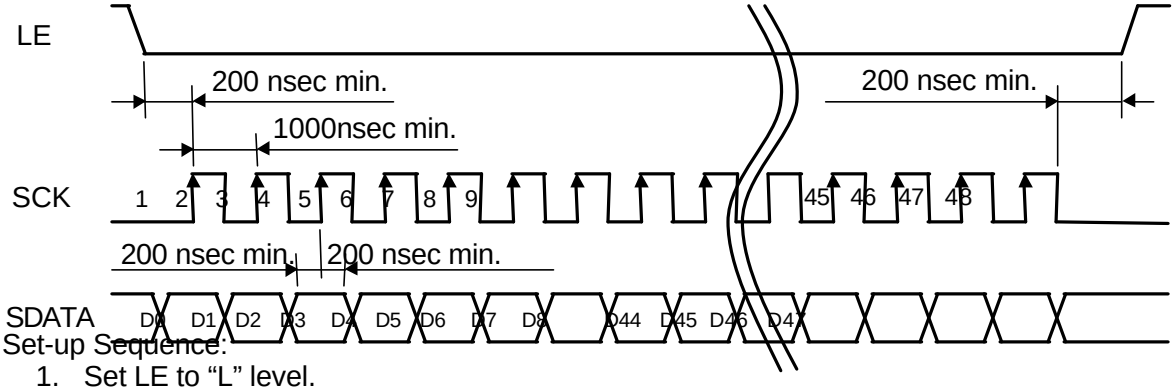
Note 1: When ALARM output turns to "L" level, high voltage power input (Sustain power supply: Vs, and Data power supply: Vd) should be switched off immediately. When glass panel is broken, high voltage may occur at the electrode section and cause electric shock. Failure of internal power-source cause over-power status and gives damage to the display panel and driver-circuits.

Note 2: When use the internal PLE function, these signals become invalid. In this case, it is recommended to the terminals must be kept open.

LVDS TRANSMITTER PIN ASSIGNMENT



Set-up of control mode signals and display position



Set-up Sequence:

1. Set LE to “L” level.
2. Enter the 48 bits of SDATA into the module synchronizing to the serial crock signal (SCK)
3. Set LE to “H” level.

Note 1: SCK clock rate: 1MHz max.

Note 2: Serial input data should be refreshed at leased in every 5 or 6 seconds or less.

Note 3: Entered serial data (SDATA) becomes effective the falling edge of the VSYNC signal while LE signal is “H” level. When VSYNC signal is overlapped with the “L” period of LE signal, the serial data becomes effective at the falling edge of the VSYNC signal after LE signal becomes “H” level.

Note 4: When only 48 SCK clocks are entered while LE is “L” level period, SDATA become enable, If SCK clocks number is not 48, SDATA is not refreshed.

Note 5: When powers are supplied to the module, serial data in the module has vague status. Therefore serial data should be refreshed after powered on.

Mode setting signals

Table10. Contents of SDATA (Mode setting serial input data)			
SDATA	Signal name	Function	Remarks
D0	RESERVE	(Spare bit)	Fix to "L" level
D1	CODE 2	Selection of Video / PC mode	Refer to the Table 11
D2	CODE 1		
D3	CODE 0		
D4	RESERVE	NEC internal use	Fix to "L" level
D5	RESERVE		Fix to "L" level
D6	RESERVE		Fix to "L" level
D7	LIFEH	Switch for PLE luminance level	L: PLE normal operation H: Fix PLE to low luminance level for longer life operation
D8	RESERVE	(Spare bit)	Fix to "L" level
D9	SELFPLEH	Switch for "Internal PLE" and "External PLE"	H: Internal PLE control L: External PLE control
D10	TSELB	Switch for ADCK data latch timing	Fix to "H" level
D11	FV 2	Vertical frequency selection	Refer to the Table 11
D12	FV 1		
D13	FV 0		
D14	DISPLINE 2	Display line number Refer to the Table12	Line 400 480 DL2 L L DL1 L L DL0 L H
D15	DISPLINE 1		
D16	DISPLINE 0		
D17	DISPDOT 2	Display pixel number/line Refer to the Table12	Pixels 640 853 DD2 L L DD1 L H DD0 L H
D18	DISPDOT 1		
D19	DISPDOT 0		
D20	VDELAY 256	Display start vertical position Refer to the "VD" in the table 12 and item "Display position:p19"	Set the display start line numbers after the falling edge of the VSYNC. Range of setting line numbers: 0 to 511 This number should not exceed the total line numbers in one frame period (1V).
D21	VDELAY 128		
D22	VDELAY 64		
D23	VDELAY 32		
D24	VDELAY 16		
D25	VDELAY 8		
D26	VDELAY 4		
D27	VDELAY 2		
D28	VDELAY 1		
D29	HDELAY 512	Display start horizontal position Refer to the "HD" in the table 12 and item "Display position:p19"	Set the display start pixel numbers after the falling edge of the HSYNC. Range of setting pixel numbers: 0 to 1023 This number should not exceed the total pixel numbers in one line period (1H).
D30	HDELAY 256		
D31	HDELAY 128		
D32	HDELAY 64		
D33	HDELAY 32		
D34	HDELAY 16		
D35	HDELAY 8		
D36	HDELAY 4		
D37	HDELAY 2		
D38	HDELAY 1		
D39	HPOS 3	Setting of horizontal display positional. Display position is adjustable by 2 pixel steps.	Position Left ------ Center ------- Right POS3 L L L ··· H··· H H H POS2 L L L ··· L··· H H H POS1 L L H ··· L··· L H H POS0 L H L ··· L··· H L H
D40	HPOS 2		
D41	HPOS 1		
D42	HPOS 0		
D43	MASKLEVEL 3	Gray level in black area (Possible to set 0-24% of white level)	Level(%) Dark ---------- Light ML2 L L L L L L L L H H H H H H H H ML1 L L L L H H H H L L L L H H H H ML0 L L H H L L H H L L H H L L H H MLL L H L H L H L H L H L H L H L H
D44	MASKLEVEL 2		
D45	MASKLEVEL 1		
D46	MASKLEVEL 0		
D47	RESERVE	(Spare bit)	Fix to "L" level

Table 11 Video Signal Mode setting Code

Input Signal	Mode setting serial Data						Maximum Vertical Synchronous Freq.	Remarks
	D1	D2	D3	D11	D12	D13		
	CODE2	CODE1	CODE0	FV2	FV1	FV0		
Video 50Hz 8bits(256 steps)	L	L	H	L	L	L	46 to 54Hz (Note1)	LSB is deleted if the freq. = 51Hz(approx.)
Video 50Hz 8bits(256 steps)	H	H	L	L	L	L	46 to 54Hz (Note1)	LSB is deleted if the freq. = 51Hz(approx.) Reduced false contour mode
Video 50Hz 7bits(128 steps)	H	L	H	L	L	L	46 to 54Hz (Note1)	LSB is deleted if the freq. = 51Hz(approx.) High luminance mode (Note 2)
Video 60Hz 8bits(256 steps)	L	H	L	L	L	H	55 to 64Hz (Note1)	LSB is deleted if the freq. = 61Hz(approx.)
Video 60Hz 8bits(256 steps)	L	H	H	L	L	H	55 to 64Hz (Note1)	LSB is deleted if the freq. = 61Hz(approx.) Reduced false contour mode
Video 60Hz 8bits(256 steps)	H	L	L	L	L	H	55 to 64Hz (Note1)	LSB is deleted if the freq. = 61Hz(approx.) High luminance mode (Note 2)
PC 60Hz 8bits(256 steps)	L	L	L	L	L	H	55 to 64Hz	Low peak luminance mode for reducing Image-Sticking
PC 66Hz 8bits(256 steps)	L	L	L	L	H	L	65 to 67Hz	Low peak luminance mode for reducing Image-Sticking
PC 60Hz 8bits(256 steps)	L	L	L	L	H	H	67 to 71Hz	Low peak luminance mode for reducing Image-Sticking
PC 60Hz 8bits(256 steps)	L	L	L	H	L	L	72 to 75Hz	Low peak luminance mode for reducing Image-Sticking

Note 1: When Vertical synchronous freq is over than the above maximum freq., the module is set to low luminance mode.

Note 2: Because the temperature of the glass surface and circuit (HIC, etc) will rise to high temperature on this high luminance mode, it is necessary to be more careful of cooling design.

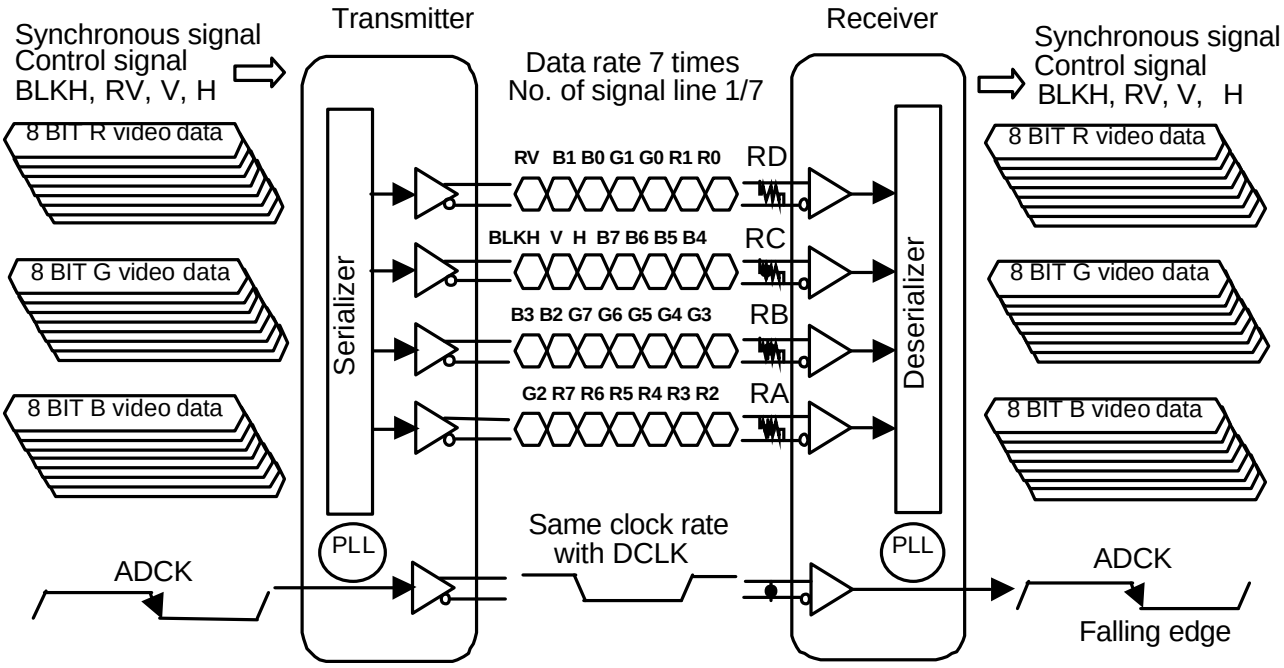
Example of video signal input and signal timing

Table 12 Relation Between Input Signal and Module RGB Signal Input

Standard Format of Video Signal						Mode Signal Data for PDP Module													
						Normal Mode (4:3) 640?480								Full mode (16:9) 853?768					
No.		Signal Name	Vertical synch-ronous Freq. (Hz)	Total number of lines (Note5)	Horizontal synch-ronous Freq. (KHz)	Recommended dot-clock number in one horizontal synchronous signal period (Horiz.freq.:MHz)		Read start timing after sync. signal		Mode bit (Note2)				Recommended dot-clock number in one horizontal synchronous signal period (Horiz.freq.:MHz)		Read start timing after sync. signal		Mode bit (Note4)			
								VD	HD	CODE	FV	DL	DD			VD	HD	CODE	FV	DL	DD
Video Mode	1	EUTV (256steps)	50.00	525	26.25	780	(20.48)	37	128	1	0	1	0	1040	(27.3)	37	171	1	0	1	3
	2	EUTV (128steps)	50.00	525	26.25	780	(20.48)	37	128	6	0	1	0	1040	(27.3)	37	171	6	0	1	3
	3	EDTV (256steps)	59.94	525	31.47	780	(24.55)	34	116	2	1	1	0	1040	(32.73)	34	154	2	1	1	3
		EDTV (128steps)	59.94	525	31.47	780	(24.55)	34	116	3	1	1	0	1040	(32.73)	34	154	3	1	1	3
	4	HDTV (256steps)	60	1125/2	33.75	---	---	--	--	--	--	--	--	1054	(35.57)	39	113	2	1	1	3
	5	HDTV (128steps)	60	1125/2	33.75	---	---	--	--	--	--	--	--	1054	(35.57)	39	113	3	1	1	3
PC Mode	6	NEC 640X400	56.4	440	24.83	848	(21.05)	32	149	0	1	0	0	1130	(28.06)	32	199	0	1	0	3
	7	NEC 640X400	70	449	31.47	800	(25.18)	35	143	0	3	0	0	1066	(33.55)	35	191	0	3	0	3
	8	IBM 640X400	70	449	31.47	800	(25.18)	35	146	0	3	0	0	1066	(33.55)	35	195	0	3	0	3
	9	VGA 640X480	59.94	525	31.47	800	(25.18)	34	144	0	1	1	0	1066	(33.55)	34	192	0	1	1	3
	10	IBM 640X480	59.94	525	31.47	800	(25.18)	26	136	0	1	1	0	1066	(33.55)	26	181	0	1	1	3
	11	NEC 640X480	59.94	525	31.47	800	(25.18)	38	145	0	1	1	0	1066	(33.55)	38	193	0	1	1	3
	12	MAC 640X480	66.66	525	35.00	864	(30.24)	41	160	0	2	1	0	1152	(40.32)	41	213	0	2	1	3
	13	VESA 640X480	72.8	520	37.86	832	(31.5)	30	168	0	4	1	0	1109	(42.00)	30	224	0	4	1	3
	14	VESA 640X480	75	500	37.5	840	(31.5)	18	184	0	4	1	0	1120	(42.00)	18	245	0	4	1	3
	15	IBM 640X480	75	525	39.38	800	(31.5)	33	144	0	4	1	0	1067	(42.00)	33	192	0	4	1	3

Note 1: Maximum data clock (ADCK) frequency is 50MHz.
Note 2: Maximum horizontal frequency in Video mode is 47 kHz.
Note 3: Maximum horizontal frequency in PC mode is 70 kHz.
Note 4: Range of setting vertical frequency is from 50 to 75Hz.
Note 5: Input signal should be applied to PDP-module after line-conversion to display line numbers (400 or 480lines).
Note 6: In case of EUTV, EDTV, HDTV signals, progressive signal should be applied to the module after scan conversion according to the display pixel numbers.
Note 7: Above mode signal (CODE, FV, DL, DD, VD, HD) described in decimal notation should be set in binary notation
Note 8: D14 to D19 (Display lines number and Display pixel number/line) of serial input data should be set correctly according to the display data. If do not correct, PLE function is not operated correctly.
Note 9: When VD and HD are set according to the above table, horizontal display position is set to the almost center of the screen.

LVDS (FPDLINK) data transfer format



(As for detail of LVDS interface, please refer to http:// www.national.com.)

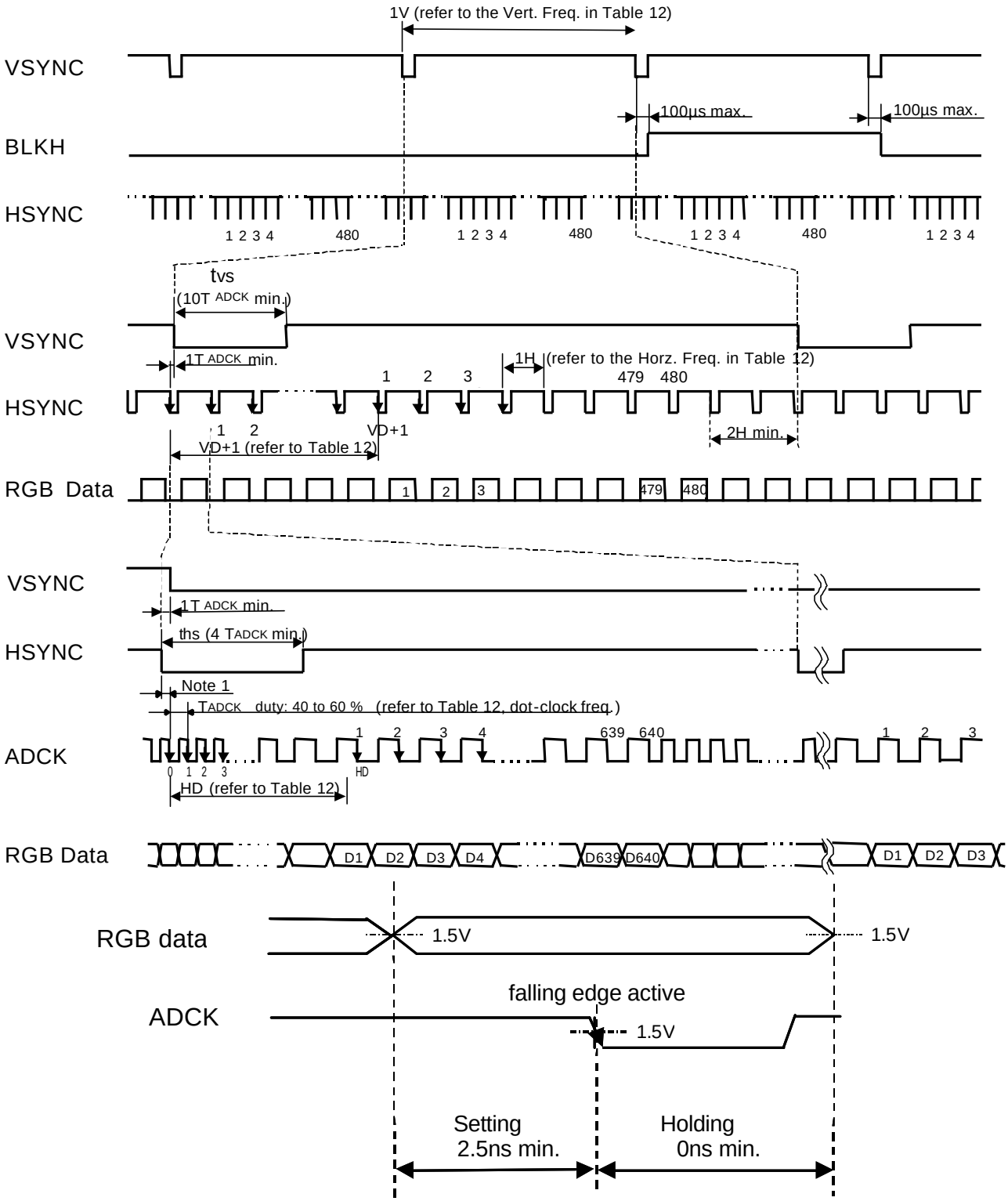
SIGNAL TIMING

Refer to the timing diagram on the following pages.

- Input video signal format is determined by Mode signal (refer to Table 9)
- "T_{ADCK}" shows 1 cycle period of ADCK.
- "tvs" shows negative pulse width of VSYNC.
- "tvh" shows negative pulse width of HSYNC.
- "1H" shows 1 cycle period of HSYNC (Horizontal Synchronous Signal).
- "1V" shows 1 cycle period of VSYNC (Vertical Synchronous Signal).
- "VD" is the data of Display start vertical position. It is set by "VDELAY 1 to 256" in the Mode Setting Signals (SDATA).
- "HD" is the data of Display start horizontal position. It is set by "HDELAY 1 to 512" in the Mode Setting Signals (SDATA).
- In case 400 line is selected, upper 40 lines and lower 40 lines are masked with gray patterns.

Timing Diagram (Normal Display Mode, 480 lines)

(Input signal of LVDS transmitter DS90CF383A)



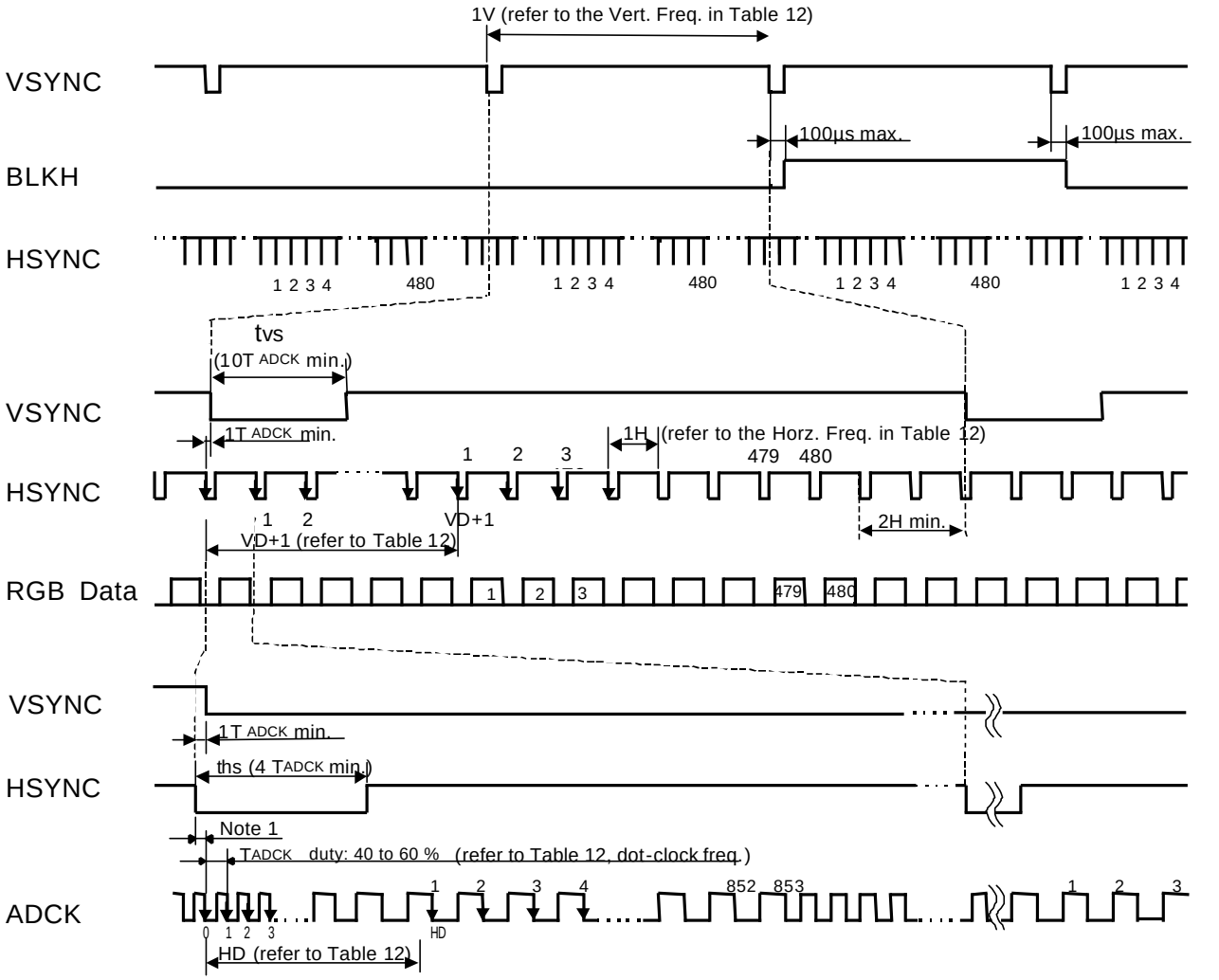
NOTE 1**:** This period is determined by each LVDS transmitter specification. And it should not be changed even if under the following conditions.

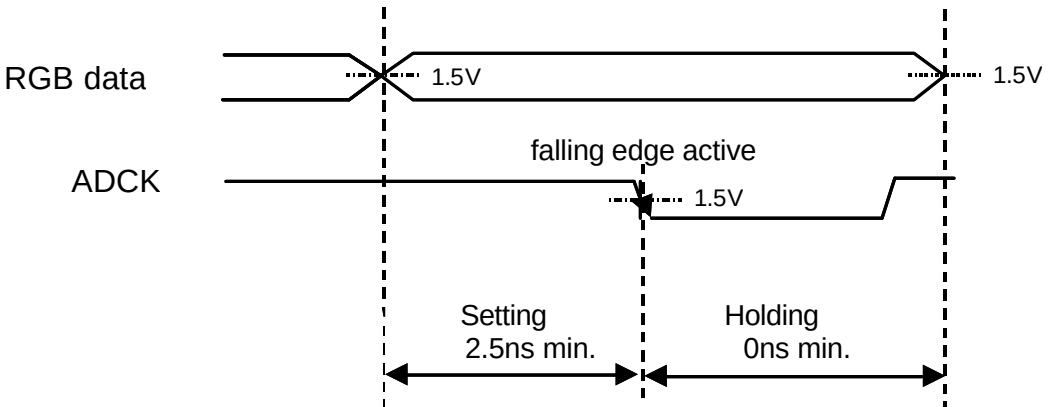
*Power ON / OFF

*Change the signal source (e.g. Video to PC)

Timing Diagram (Full Display Mode, 480 Lines)

(Input signal of LVDS transmitter DS90CF383A)





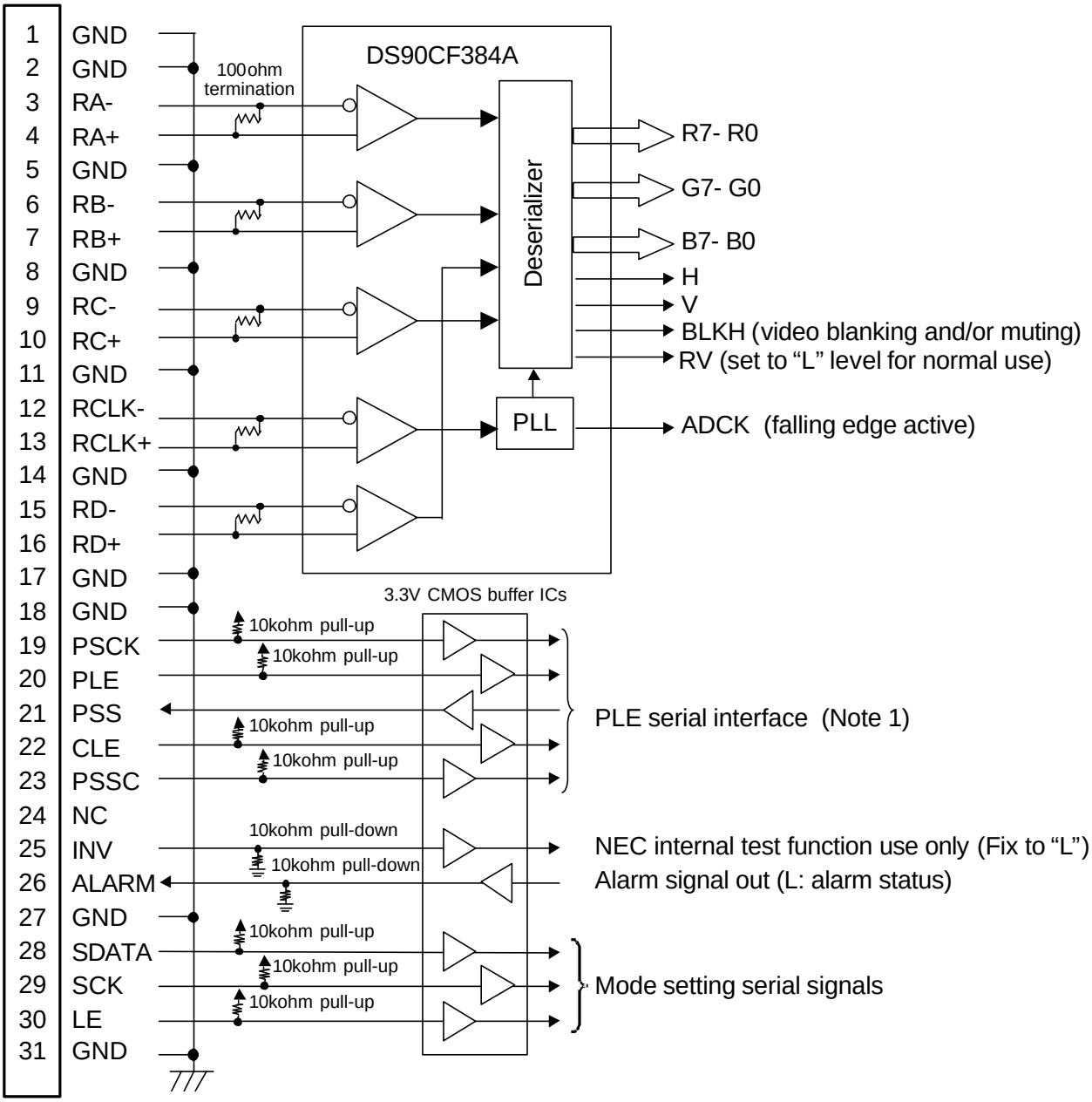
NOTE 1**:** This period is determined by each LVDS transmitter specification. And it should not be changed even if under the following conditions.

*Power ON / OFF

*Change the signal source (e.g. Video to PC)

Interface connector pin assignment and input output circuits

Following shows the interface connector pin assingnment and input output circuits in the PDP module.



Type of serial interface connector

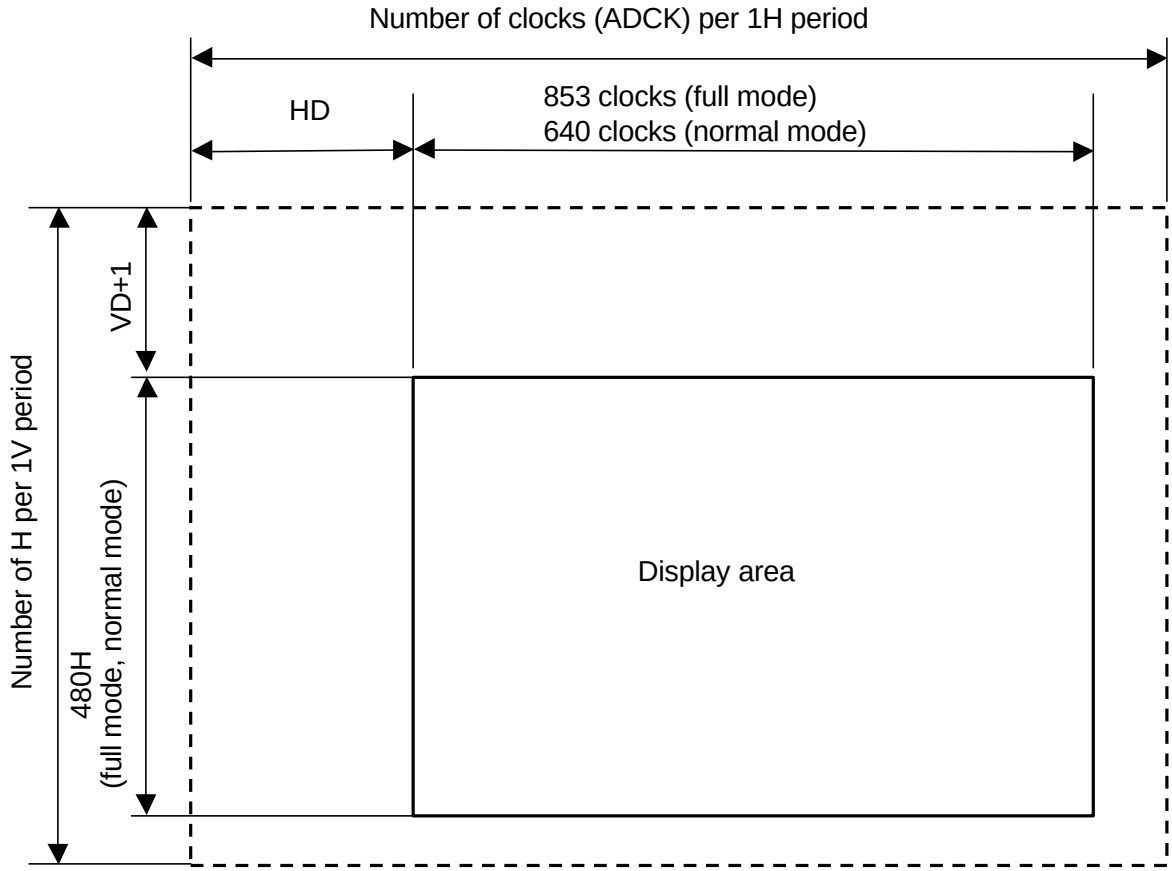
Module side connector:	FI-TWE31PB-VF
Mating connector:	FI-W31S (plug housing)
	FI-C3-A1-15000 (contact)
Connector supplier:	Japan Aviation Electronics Industry, Limited (JAE)
Fitting cable:	AWG#28 to 32 twist pair cable

(Total cable assembly recommends to be shielded)

Note 1:When use the Internal PLE function, it is recommended to keep these terminals open.

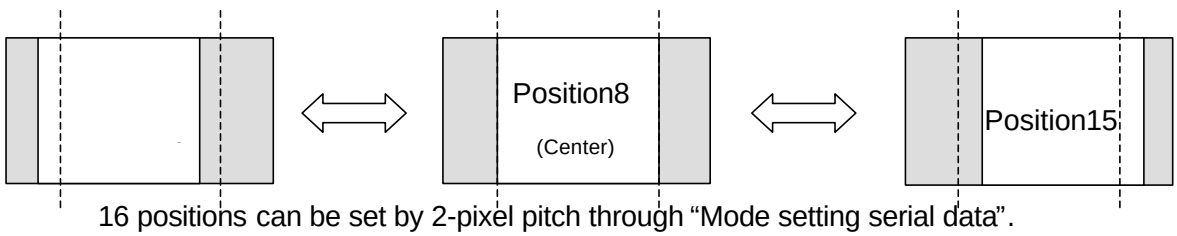
Display position

The relation among HD (HDELAY), VD (VDELAY), and the display position is as shown below.



1) Relation between VD/HD and display start position
   Display start vertical position from falling edge of VSYNC = VD+1 (Number of lines or Number of H periods)
   Display start vertical position from falling edge of HSYNC = HD (Number of pixels or Number of clocks)
2) Setting range of VD and HD
   VD: 0 to 511 lines
   HD: 0 to (Number of clocks per 1H period –1), Max.1023 pixels
3) Limitation of number of clocks per 1H period
   normal mode: 2+640 = Number of clocks per 1H period = 3071
   full mode: 2+853 = Number of clocks per 1H period = 3071
4) Limitation of number of HSYNC pulses per 1V period
   480+2 ? Number of HSYNC pulses per 1V period ? 2047 (HSYNC)
   (2 HSYNC pulse or more are necessary after display area)

Display position setting



16 positions can be set by 2-pixel pitch through “Mode setting serial data”.

Protection against excessive load comes from unexpected image display.

Plasma display module has a characteristic when data write switching operation is repeated rapidly, the load of the driver circuits become large. For example, this high load status is appeared when the following pattern is displayed. (Cell base checker pattern by on/off cells alternately by each cell. In general operation, this kind of pattern does not exist).

In case this kind of image is displayed, this plasma display module gets into the protect-operation of driving circuits.

While in the protect-operation, some display image may be deteriorated a little. However as soon as the display image returns to normal pattern, the protect-operation is released, and returns to the formal operation

R	G	B	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B
R	G	B	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B
R	G	B	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B
R	G	B	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B
R	G	B	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B
R	G	B	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B
R	G	B	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B
R	G	B	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B
R	G	B	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B
R	G	B	R	G	B	R	G	B	R	G	B	R	G	B	R	G	B

Lit cell   Unlit cell

Guideline of general display images which make to carry out the protect-operation.
The protect-operation may be carried out when following patterns are displayed.

1) When the cell base checker pattern is displayed over 50% of the whole display area, or other patterns that give equivalent on/off display loads to the driver circuits are displayed.

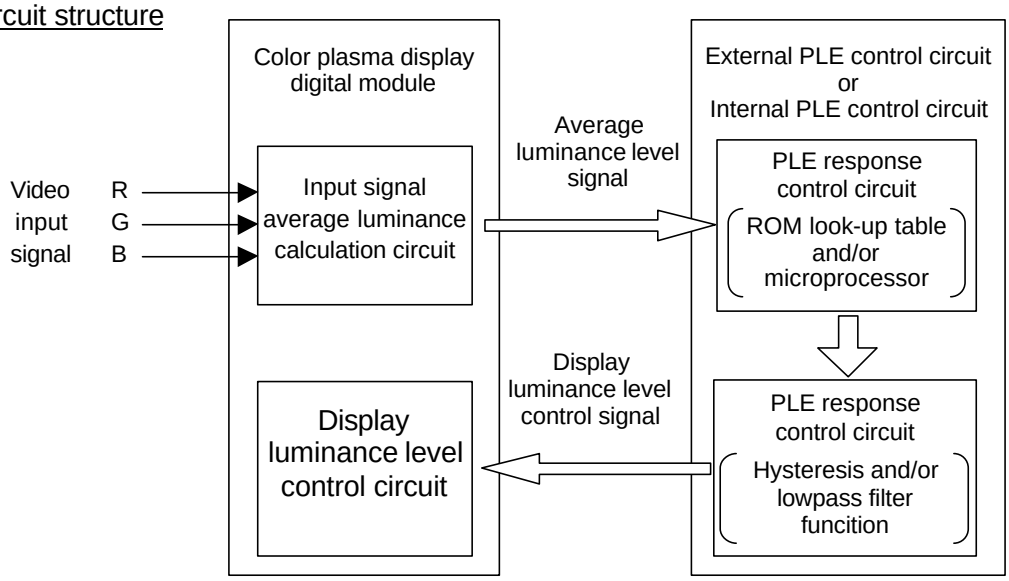
or,

2) When the cell base checker pattern is displayed over 60% of 518mm in height (all screen height) × 69mm in width (about 1/13 of screen width) area, or other patterns that give equivalent on/off display loads to the driver circuits are displayed.

PLE (Peak Luminance Enhancement) FUNCTION

The PLE function makes it possible to increase the luminance level of the PDP display when the average luminance level of the input video signal is low. This PLE function reduces the maximum power by absorbing the luminance when the high-power-load-image is displayed, and results in a higher contrast level.

PLE circuit structure



This plasma display module has following two modes. These two modes can be selected by the mode control signal.

1. "Internal PLE" mode ---- Built-in PLE function in the PDP module itself. This PLE mode realizes one of the best PLE characteristics without any additional circuit. Therefore this mode is very convenient, and it is recommend to be utilized this function actively.

2. "External PLE" mode --- Externally controlled PLE function from the customer's interface circuit. External PLE mode enables to make customer's original characteristics within the limitation range. The PLE characteristics is strongly related not only the luminance characteristics of plasma display module but also the power consumption and the generated heat, therefore it is required to obtain the acknowledgement of NEC concerning the external PLE characteristics to be set at the customer.

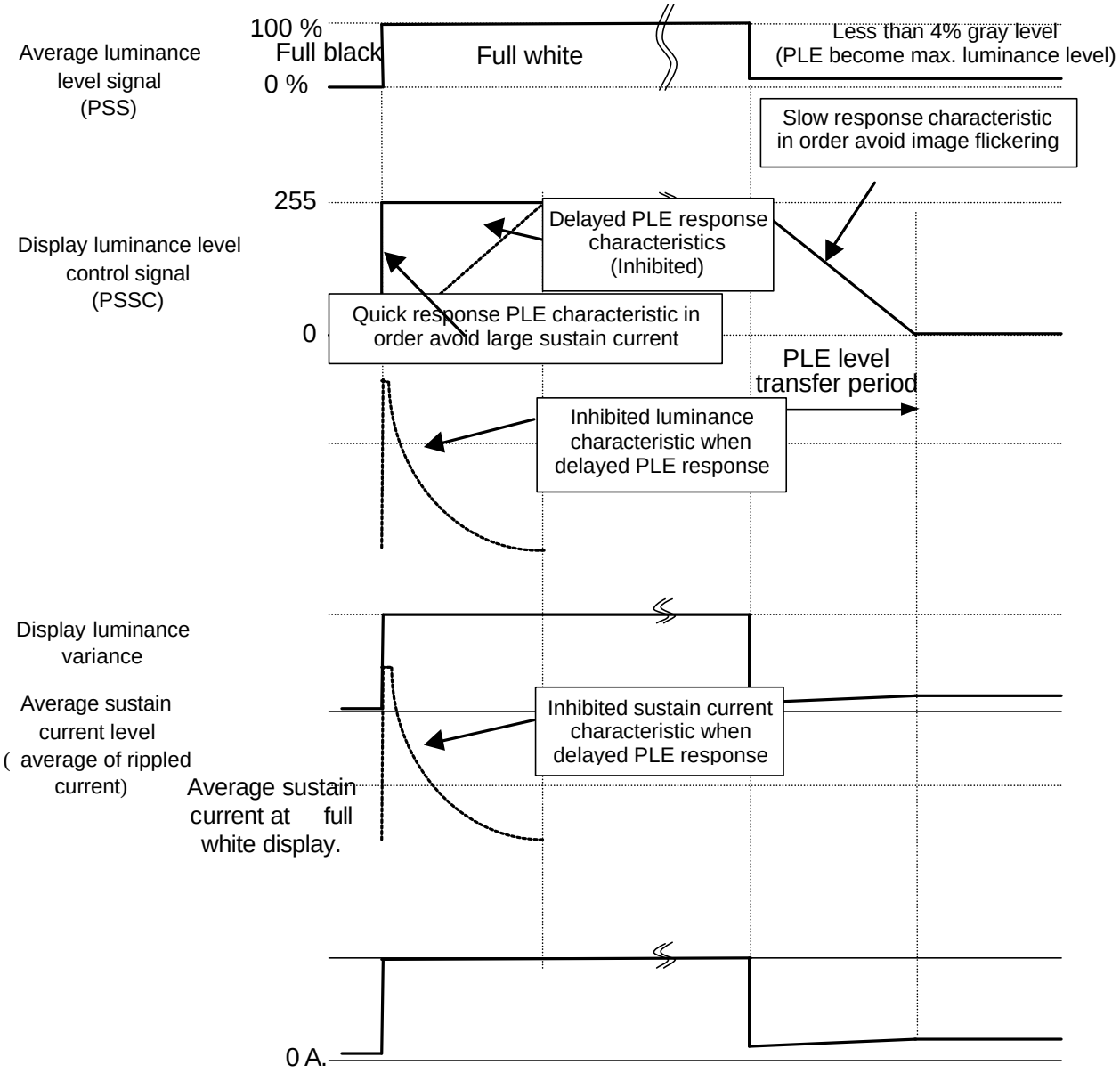
(Caution)
When use the external PLE function, please use within the limitation range. If external PLE characteristic is set outside of the limitation range, plasma display module may have damage.
Any trouble caused by this incorrect operation is not included in the warranty

Power consumption and generated heat of plasma display module varies depending on the setting values of PLE characteristic. Therefore the temperature investigation and optimization of cooling design should be done in the state mounted in the plasma display set.

Characteristics of internal PLE

When PDP module displays full white with maximum luminance, or when PLE characteristic has some delayed response and display image is changed from full black to full white, large sustain current flows, and plasma display becomes over power status.

In the internal PLE function, when the "Average luminance level" increases, in order to avoid large sustain current flow and over power status, the "Display luminance level" is immediately reduced to the setting level with quick response. And when display load decreases, in order to avoid image flickering caused by the short term average luminance level's fluctuations, the "Display luminance level" is gradually move to the setting level with a slow response characteristic.
(Refer to the following figures)



CONNECTORS PIN ASSIGNMENT
(For the connector position, please refer to the Rear View in the Outline Drawing)

1. POWER INPUT CONNECTOR

Table 13. Connector CN301 Pin Assignment	
Pin No.	Symbol
1	L
2	N

Power-supply side connector: B02B-VT
Mating connector: VTR-02 (housing),
SVT-41T-P1.1 (contact)
Connector supplier: J.S.T. TRADING COMPANY., LTD.
Fitting Cable: Equivalent to AWG#20

2. POWER OUTPUT CONNECTOR for EXTERNAL CIRCUIT

Table 14. Connector CN302 Pin Assignment	
Pin No.	Symbol
1	Vaux
2	N.C.
3	GND

N.C.: non-connection pin.
Power-supply side connector: B3P-VH-B
Mating connector: VHR-3N (housing),
SVH-21T-P1.1 (contact)
Connector supplier: J.S.T. TRADING COMPANY., LTD.
Fitting Cable: Equivalent to AWG#20

3. POWER-SUPPLY INTERFACE CONNECTOR

Table 15. Connector CN303 Pin Assignment	
Pin No.	Symbol
1	PSO
2	PSM
3	P-fail
4	GND
5	STB

Power-supply side connector: B05B-VT
Mating connector: EHR-5 (housing),
SEH-001T-P0.6 (contact)
Connector supplier: J.S.T. TRADING COMPANY., LTD.
Fitting Cable: Equivalent to AWG#26

2. SIGNAL INTERFACE CONNECTOR

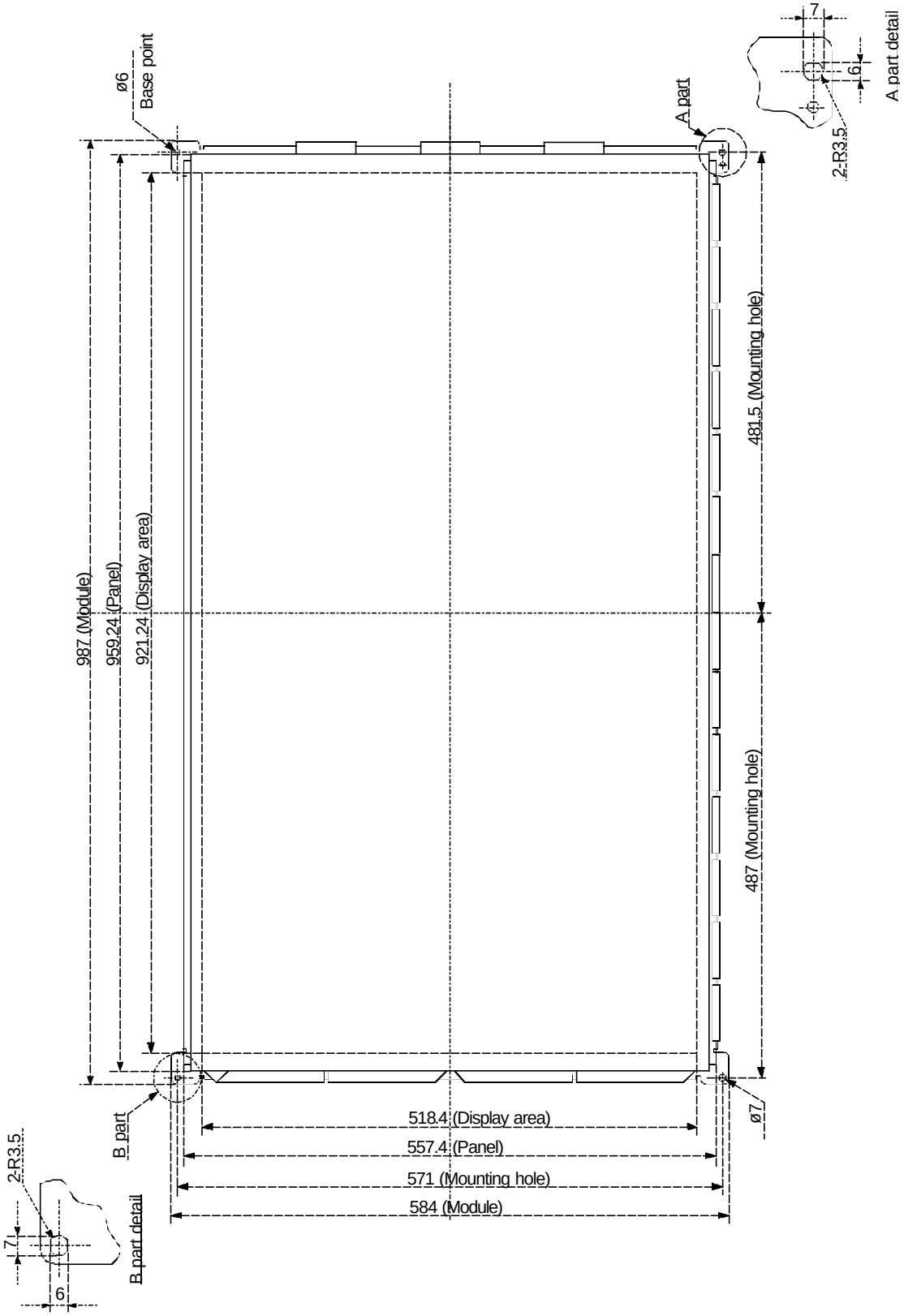
Table 16. Connector CN201 Pin Assignment			
Pin No.	Symbol	Pin No.	Symbol
1	GND	2	GND
3	RA-	4	RA+
5	GND	6	RB-
7	RB+	8	GND
9	RC-	10	RC+
11	GND	12	RCLK-
13	RCLK+	14	GND
15	RD-	16	RD+
17	GND	18	GND
19	PSCK (Note 1)	20	PLE (Note 1)
21	PSS (Note 1)	22	CLE (Note 1)
23	PSSC (Note 1)	24	SL (Note 2)
25	INV (Note 2)	26	ALARM
27	GND	28	SDATA
29	SCK	30	LE
31	GND	---	---

Module side connector: FI-TWE31PB-VF
Mating connector: FI-W31S (housing),
FI-C3-A1-15000 (contact)
Connector supplier: Japan Aviation Electronics Industry, Limited (JAE)
Fitting Cable: AWG#28 to 32 twist pair cable
(Total cable assembly recommends to be shielded.)

Note 1: When use the Internal PLE function, it is recommended to keep these terminals open.
Note 2: Fix to "L"

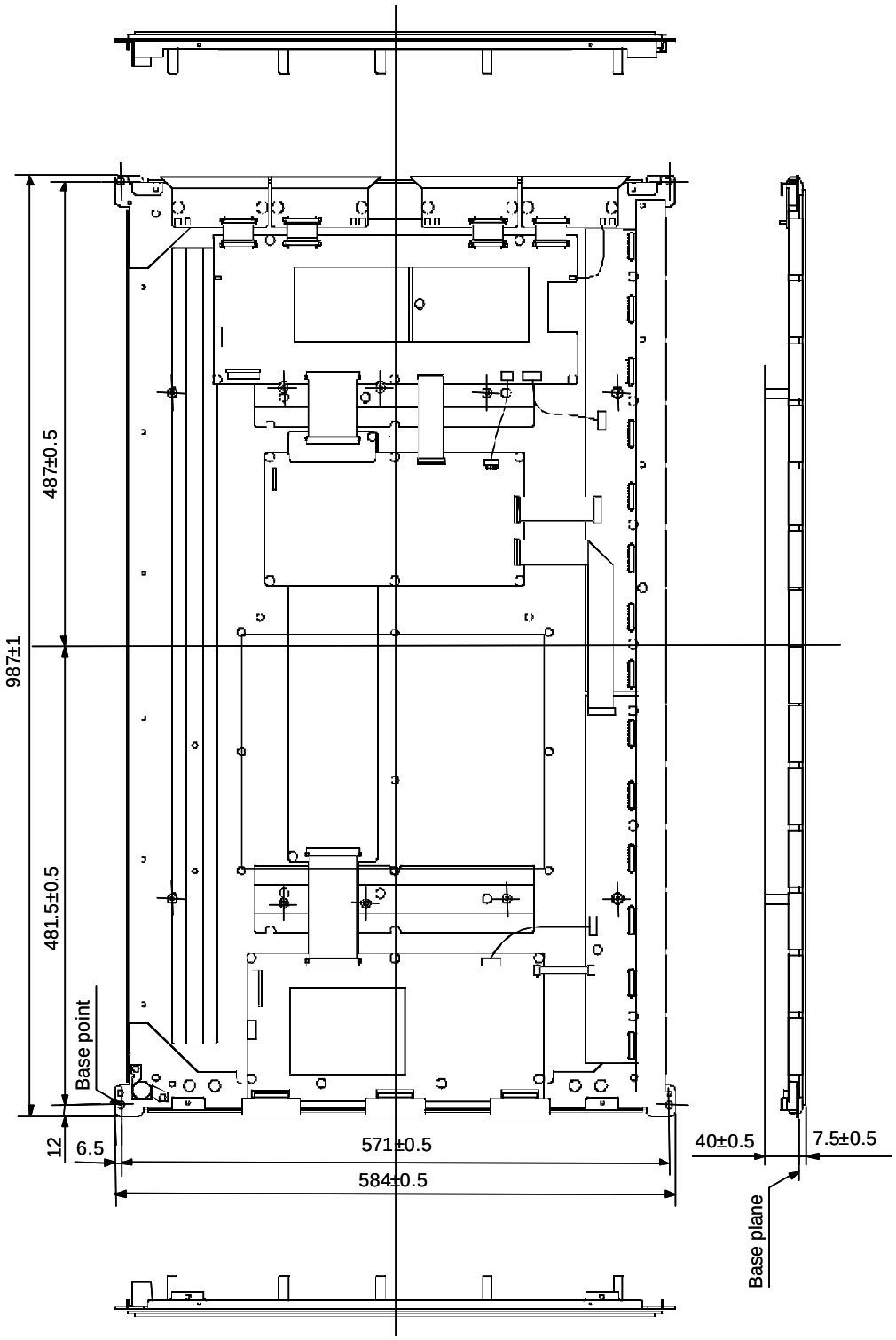
MECHANICAL DRAWING (Unit: mm)

FRONT VIEW



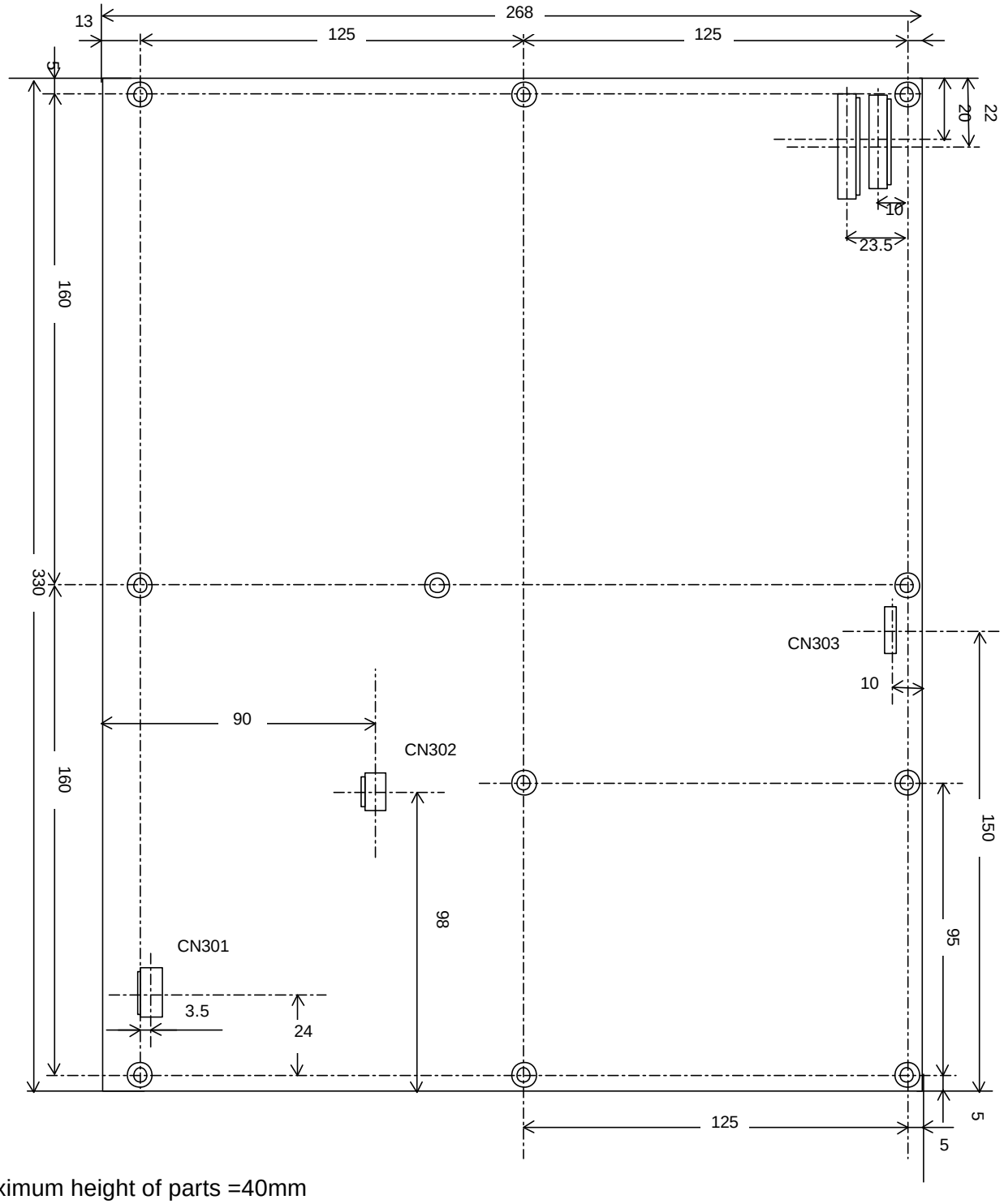
MECHANICAL DRAWING (Unit: mm)

REAR VIEW



CONNECTORS POSITION ON POWER SUPPLY (Unit: mm)

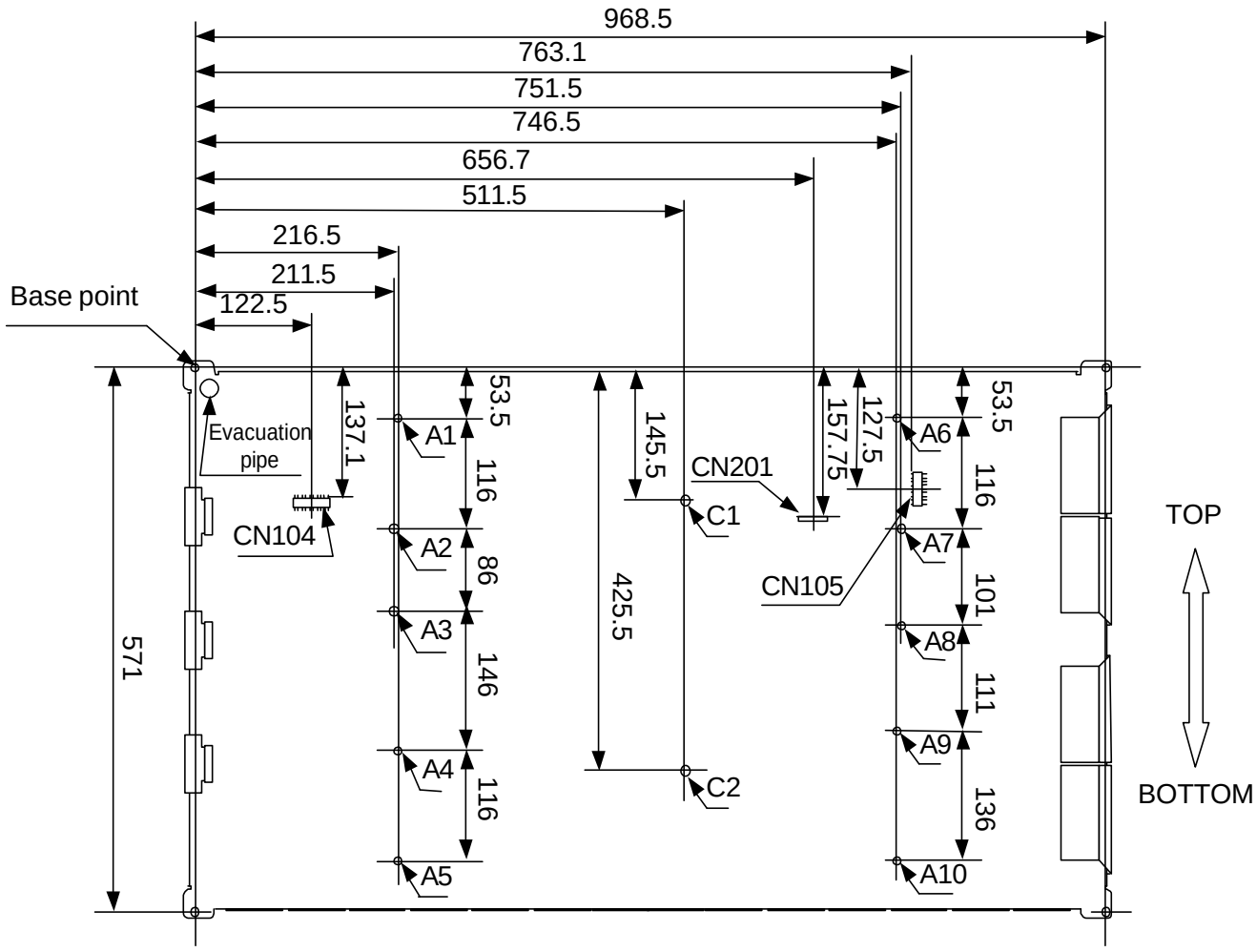
TOP VIEW OF POWER SUPPLY



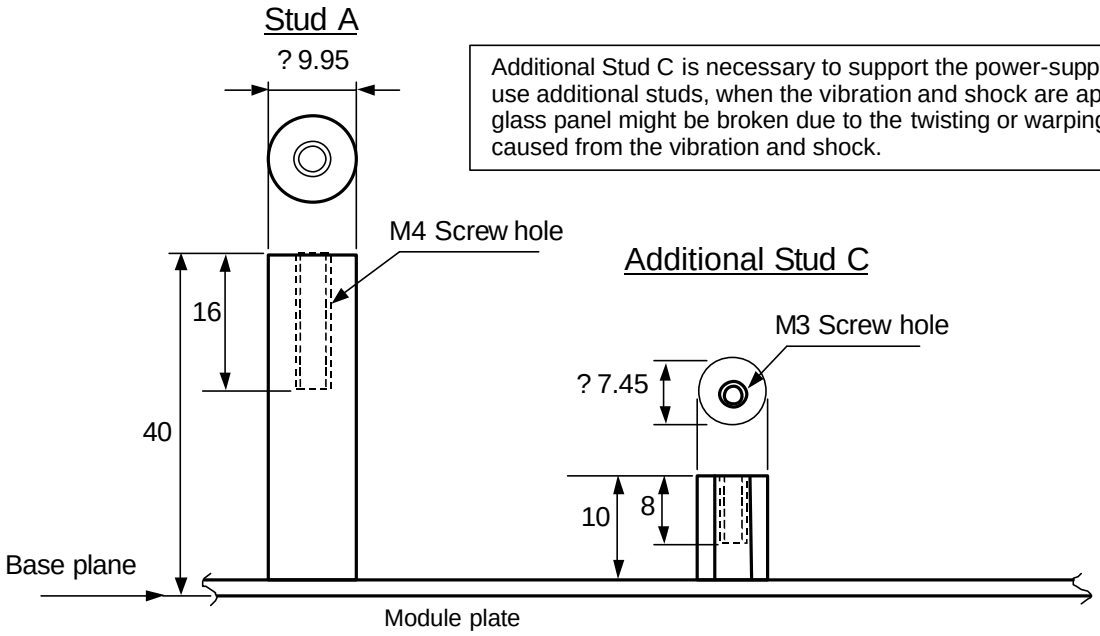
Maximum height of parts =40mm

Depth(Z) of this unit(including baseboard + soldering)=45mm

STUDS AND CONNECTORS POSITON
REAR VIEW (Unit: mm)



SHAPE OF STUD: A1 to A10, C1, C2 (Unit: mm)



Additional Stud C is necessary to support the power-supply. If do not use additional studs, when the vibration and shock are applied, the glass panel might be broken due to the twisting or warping forces caused from the vibration and shock.

Locatable position of other parts or structures adjacent to the PDP module
Rear view (Unit: mm)

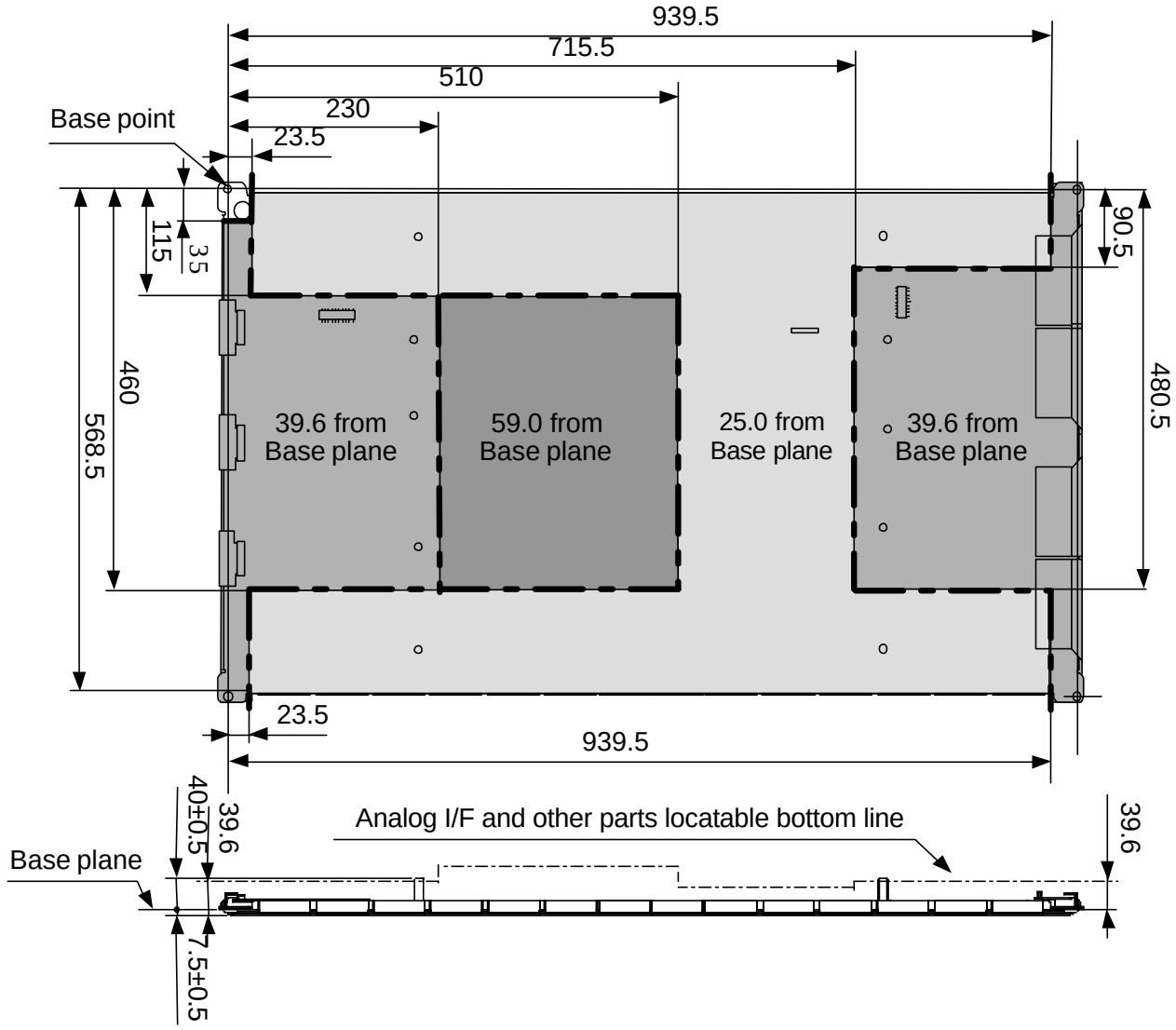


IMAGE STICKING CHARACTERISTICS

1) Image sticking

The fluorescent substance used in the plasma module loses its luminance with the lapse of lighting time.
This deterioration in luminance appears to be a difference in luminance in relation to the surroundings, and comes to be recognized as image sticking.

In other words, the image sticking is defined as follows: when the same pattern (of the fixed display) is displayed for a long time, a difference in luminance is caused around the lighting area and non-lighting area due to deterioration in the fluorescent substance.
When the present pattern is changed over to another one, the boundary comes to be seen between the lighting area and non-lighting area due to difference in luminance in the pattern shown shortly before changeover. If this condition is accumulated, the boundary or image sticking comes to be seen with the naked eyes.

2) Secular change in luminance

The life of luminance, defined as the reduction to half the initial level, is more than 10 thousand hours on average.
Conditions: All white (100% white) input at an ambient temperature of 25 °C.
However, this life time is not a guarantee value for life and luminance. It should be recognized simply as the data for reference.

3) Warranty

Image sticking and faults in luminance and picture elements are excluded from the warranty objects.

4) Cause of deterioration in luminance

A major possible cause of deterioration in luminance is damage in the fluorescent substance due to impact caused by ions generated at the time of plasma discharges.

5) Practical value for Image sticking

The relationship between integrated lighting time and luminance in this plasma module is described in the attached material. In particular, the deterioration in luminance tends to be accelerated up to 100 hours in the initial period. In the initial period, the fixed display of patterns particularly tends to cause image sticking.
The practical value for image sticking is difficult to define in concrete numerals. As described below, you are advised to take proper measures to make the occurrence of image sticking as slow as possible.

6) Proposed measures taken to relieve image sticking

So long as there is the reduction of luminance in the fluorescent substance, it is impossible to avoid the occurrence of image sticking. Therefore, to relieve image sticking, we offer you a method of entering an image input that may ensure reluctance to the generation of the difference in luminance reduction among the displayed dots.

The images from TV broadcasting involve a high rate of motion picture displays.
Therefore,
there is less chance of being a cause of difference in luminance reduction among the cells. Even when the fixed patterns are displayed, they generally last for a few minutes.
Since the same pattern is less liable to be displayed, there is almost no influence toward image sticking.

If the fixed patterns tend to be displayed for a long time, however, there occurs a substantial imbalance between the lighting and non-lighting areas, thus causing a difference in luminance as a result. In this document, we offer you some proposals of installation, paying attentions to the two points: the reduction of difference in luminance achieved by integrated lighting time leveling and the method of edge smearing to make image sticking hard to be discerned.

The result from these proposals can, however, greatly depend on the contents of images and the operating environment. Therefore, we consider that it is essential to take the suitable measures in consideration of the customer's operating environment.

Example of Proposal 1: The display position is moved while the fixed display pattern is changed over, or it is scrolled during the display.

Example of Proposal 2: If possible, a pattern of complementary color is incorporated (for integrated time leveling).

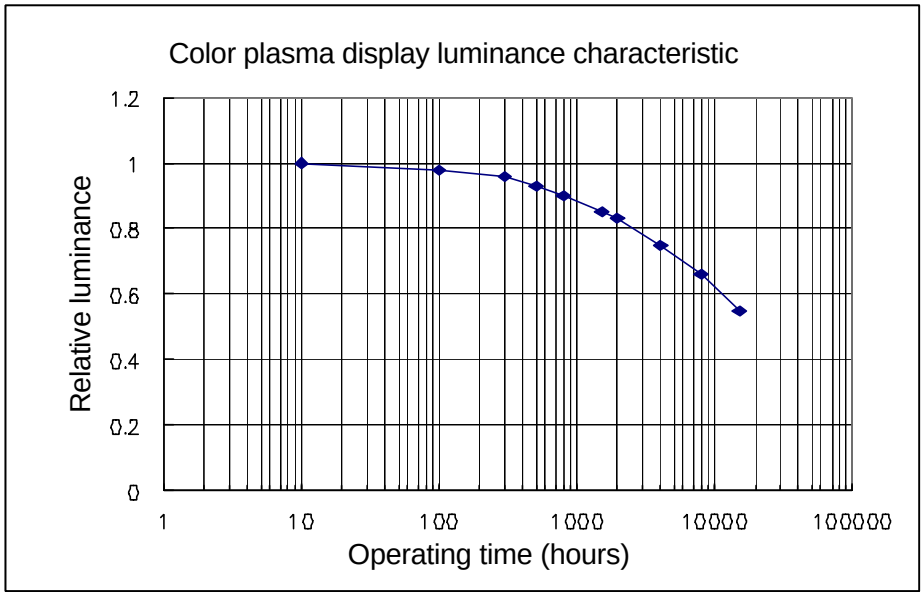
Example of Proposal 3: The fixed pattern and the motion picture display are reciprocally exchanged, in order to minimize the display period of the fixed pattern.

Example of Proposal 4: During operation, the luminance of screen is suppressed as low as possible. For the display patterns, characters are indicated not on the black ground (non-picture area) but on the colored ground (mixture of R, G, B recommended).

7) Proposed countermeasures for the plasma module

Since the PDP is a display that uses a fluorescent substance like the CRT, it is a fundamental phenomenon that image sticking occurs. Unlike the CRT, the PDP gives rise to deterioration in the fluorescent substance due to impact caused by ions generated during plasma display.

As a result of the above-mentioned improvements, it is possible to extend the PDP lifetime and relieve the effect of burning, but is impossible to realize the complete elimination of burning so far as a fixed pattern is displayed for a long time.



Usage Cautions

1) Cautions Regarding Handling of Module

(1) Plasma panel is composed of glass, when handle the product, be careful to prevent shocks and stress.

(2) The display panel used in this product is made of glass. Since shocks or vibrations may cause it to break, be very careful during handling. In case the panel breaks, be careful not to get injured with glass fragments.

(3) Since the panel surface is easily scratched, be careful not to press against the panel or scrape it with a hard object, and do not place the glass panel side down on the hard material.

(4) If the panel surface gets dirty, gently wipe it with a dry cloth. If a liquid gets on the panel, mop it up by gently applying a dry cloth without rubbing. In the case of a stubborn stain, wipe it with a cloth slightly wetted with a neutral detergent. Use only dry cloth for wiping, and avoid using the same cloth over and again. Deleterious substances such as described above or water drops getting into the module or somewhere on the module surface other than the display panel may damage the product.

(5) Handle the product with care, avoiding pressing against or scraping the glass panel surface, as this may leave the panel surface scratched or blemished.

(6) Since the flexible cables are easy breakable, when handle the plasma display module, be careful not to touch the flexible cables.

(7) Make sure that the connectors are connected tightly.

2) Cautions Regarding Design and Operation of Module

(1) Do not pull out or insert the power cable from/to an outlet with wet hands. Doing so may cause electric shock.

(2) This product emits near infrared rays (700 to 1100 nm) that may cause the remote controllers of other electric products to malfunction. To avoid this, use an infrared absorption filter and thoroughly evaluate the system and environment.

(3) This product uses a high voltage (approx. 400V). Do not touch the circuitry of this product with your hands when power is supplied to the product or immediately after turning off the power. Be sure to confirm that the voltage has dropped to a sufficiently low level.

(4) If you detect a strange smell or smoke coming out of the product, immediately turn off the power. Continuing to use the product under such conditions may cause electric shock or fire.

(5) Do not use this product with a voltage that exceeds the rated voltage as this may cause product failure or fire. The warranty does not cover problems that occur when the product is used under conditions other than those described in the specifications.

(6) When the product is used as a stationary text display device such as a text display board or for some similar display, it may get damaged by image sticking. Image sticking is a phenomenon whereby the luminance of parts of the screen where images are continuously displayed for a long time declines compared to parts of the screen where images are displayed for a shorter cumulative time, causing uneven screen luminance. The severity of image sticking is proportional to the cumulative display time and the brightness. Taking the following precautions reduces the possibility of image sticking.

<1> Lower the brightness as much as possible when displaying a stationary pattern.

<2> When displaying a stationary pattern, slightly vary the position of the pattern in the following sequence: Top? Right? Down? Left? Top and so on, or use scroll display.

<3> If possible, incorporate complementary color patterns to smooth the cumulative display time.

<4> Reduce the stationary pattern display time by alternating stationary pattern display and moving image display.

<5> When displaying stationary text, avoid display against a black background, and use a colored background instead.

Image sticking and the flicker of the lighting cell caused from the image sticking are excluded from the warranty objects.

(7) This product contains parts that generate heat during operation. During the set design stage, take into consideration the cooling method and design the frame based on careful evaluation of heating characteristics.

(8) The temperature of the glass surface of the display may rise to high temperature depending on the conditions of use. If you touch the glass inadvertently, you may be burned.

(9) This product uses a high-voltage drive pulse and emits electromagnetic noise. When this product is incorporated in a set, be sure to design the frame and fit an optical filter shield on the front side of the set so that the electromagnetic interference produced by the set falls within the allowed range.

(10) When installing this product in the frame of a set, use the indicated fixing screw holes and guide holes. Since the display panel of the product is made of glass, design the frame so as to prevent a large weight or shocks from being applied to the glass.

(11) If this product is operated after a long storage period, the screen's display performance may have deteriorated or become unstable depending on the storage conditions. In this case, it is recommended to use the product after subjecting it to two hours of aging (full-screen display).

(12) This product uses highly integrated semiconductor devices. Since these devices can be damaged by static charge, be careful to handle at the place where antistatic measure is done.

(13) Follow the procedure described in these specifications for the power ON/OFF sequence. Failure to do so will cause equipment failure.

(14) Since this product uses precise lead pitch components, be careful to prevent any foreign materials such as metal particles come out from screw part, soldering part or metal parts of cabinet, or any liquid. These foreign materials cause the short or insulation failure of the circuit, and resulting in the product failure or fire.

(15) The sulfide causes deterioration of the product and the failure. Therefore, be careful not to place the material contains sulfur such as vulcanized rubber closed to the product.

(16) Be careful not to pile up the packing boxes by two steps, and not to place the packing boxes in sideways down.

(17) When scrap the plasma display module or any sets install the plasma display module, be careful to comply with rows or rules of the region or the country.

3) Cautions Regarding Module Usage Environment

(1) Operating this product when condensation has occurred may cause failure or electric shock.

(2) Avoid using this product in locations that have a lot of dust, soot, humidity, steam, etc., as this may cause failure, electric shock, or fire.

(3) Place this product on a level surface and make sure it is stably positioned because failure or electric shock may result if it falls or turns over.

4) Others

(1) Do not overhaul or disassemble this product.

(2) When this module is repaired or modified without any acknowledgment of NEC, it voids the warranty and NEC does not have any responsibility

(3) When the plasma display module is resold to the third party or person, NEC does not have any warranty to the third party or persons.

(4) This product is designed to NEC's "Standard" quality grade. If you wish to use the product for applications outside the scope of the "Standard" grade, be sure to consult NEC in advance to assess the technological feasibility before starting to design your system.