Pioneer

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DO NOT DUPLICATE PIONEER PLASMA DISPLAY CONFIDENTIAL AND PROPRIETARY

1. APPLICATIONS

This specification is applied to the NP42H5MF01 Pioneer Corporation (hereinafter called as "Pioneer") delivered to DAEWOO Electronics Corp..

2. DESCRIPTION

The NP42H5MF01 is a 42-inch wide color plasma display module with a resolution of 1024(H) x 768(V) pixels. The display offers vibrant colors we reproduced in a thin and low profile package. This device can be operated with 8-bit, 9-bit or 10-bit of digital video signal for each RGB color, video synchronous signals, display mode control signal and 3 kinds of DC power sources. This device has a "PLE (Peak Luminance Enhancement) function that adjusts the luminance and contrast to the suitable value in accordance with the input video signal level variance, so that image can be displayed with the ideal luminance and contrast. This device has built-in video image processing functions (color space conversion, inverse gamma correction and error diffusion), and operation of these functions can be selected according to the external command.

3. BASIC CONFIGURATION

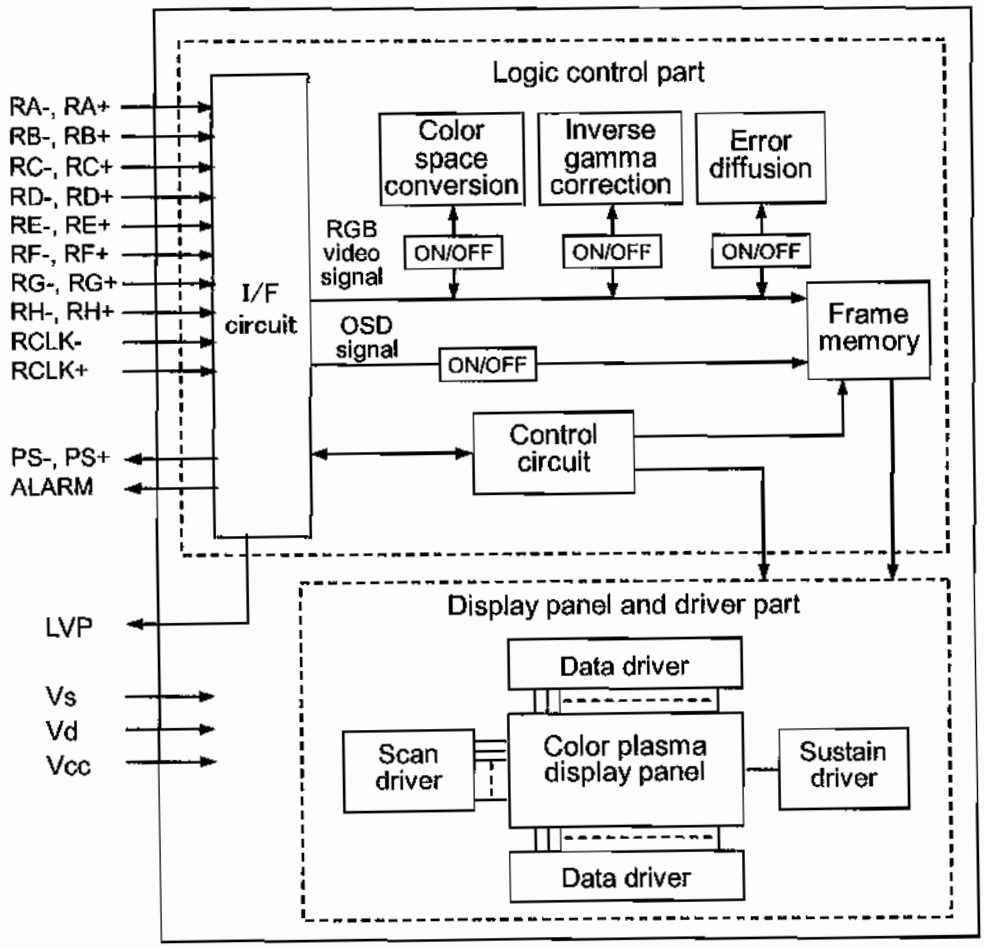


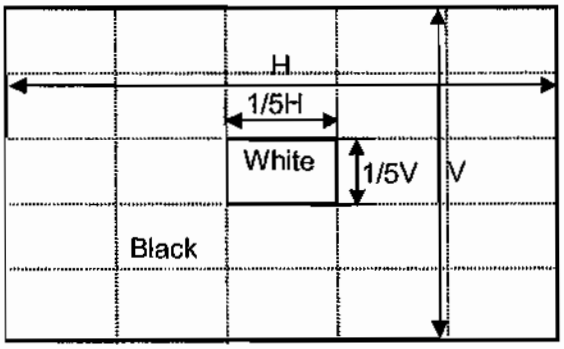
Figure 1. Basic configuration

4. DISPLAY IMAGE SPECIFICATION

Table 1. Display image specification		
Item	Specification	Remarks/Conditions
Display area	918(H) x 518(V) mm	106cm in diagonal: 42 inches
Aspect ratio	16:9	
Number of pixels	1024(H) x 768(V)	1pixel = 1 trio of R, G and B cells
Pixel pitch	0.897 (H) x 0.675 (V) mm	
Color arrangement	RGB vertical stripes	
Number of gradations	8-bit (256-grayscale)	50Hz, 60Hz Standard mode
	9-bit (512-glayscale)	50Hz, 60Hz High gradation mode
	10-bit(1024-glayscale)	60Hz High gradation mode
Peak luminance	515 cd/m^2 minimum	Refer to item 4.1 (1)
Full-screen white luminance	87 cd/m^2 minimum	Refer to item 4.1 (2)
Contrast ratio	540:1 minimum	Refer to item 4.1 (3)
Luminance uniformity (Whole screen area)	0.75 minimum	Refer to item 4.1 (4)
Color temperature	8,000 to 11,000	Refer to item 4.1 (5)

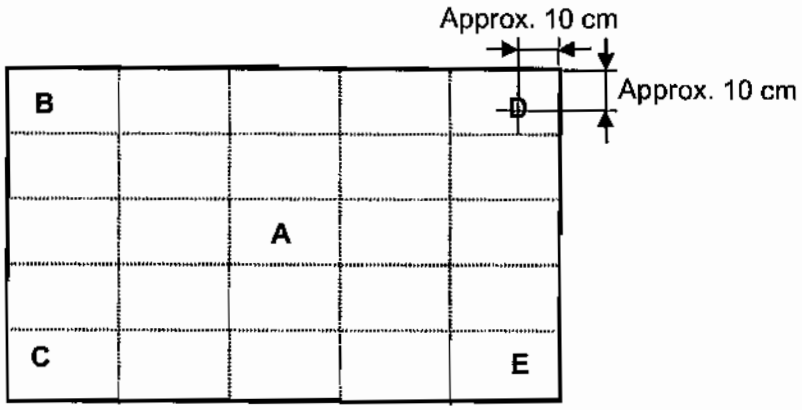
4.1. Measuring Conditions

(1) Peak luminance
- Input signal: Video signal (60Hz, Standard mode, refer to Table 13, fv=59.94Hz and fh=31.47kHz)
- Display pattern: 4% white window display
  (white window:100% signal level, back ground: 0% signal level)
- PLE condition: Internal-PLE operation
- Measuring position: Center of the following 4% white window (one point)
- Measuring equipment: Color analyzer CA-100 (Minolta)
- Measuring temperature: Room temperature



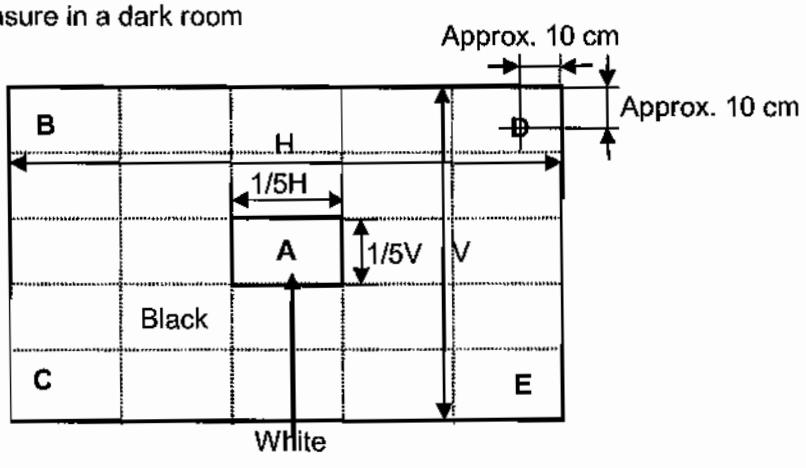
(2) Full-screen white luminance:

(Measuring Conditions)
- Input signal: Video signal (60Hz, Standard mode, refer to Table 13, fv=59.94Hz and fh=31.47kHz)
- Display pattern: Full-screen white display (100% signal level)
- PLE condition: Internal-PLE operation
- Measuring position: Measure the center and four corners luminance (total 5 points) (Full-screen white luminance = Average of above 5 points luminance)
- Measuring equipment: Color analyzer CA-100 (Minolta)
- Measuring temperature: Room temperature



(3) Contrast ratio

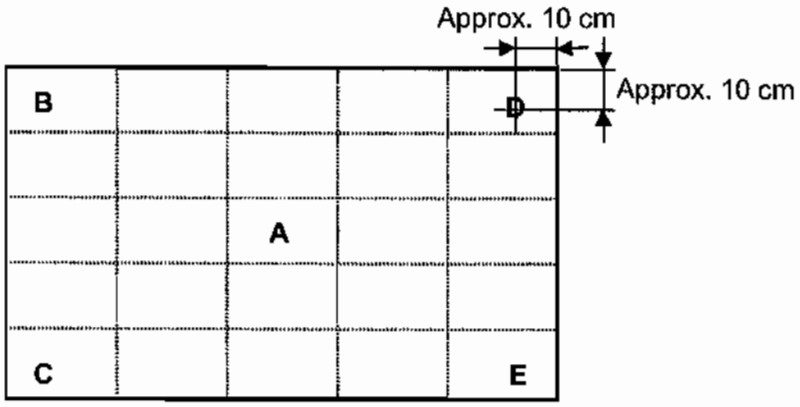
(Measuring Conditions)
- Input signal: Video signal (60Hz, Standard mode, refer to Table 13, fv=59.94Hz and fh=31.47kHz)
- Display pattern: 4% white window display
  (white window :100% signal level, back ground :0% signal level)
- PLE condition: Internal-PLE operation
- Measuring position: Center of the following 4% white window (one point) and four corners black areas (4 points).
- Contrast ratio = $\frac{\text{Luminance of A}}{\text{Average luminance of B, C, D and E}}$
- Measuring equipment: Color analyzer CA-100 (Minolta)
- Measuring temperature: Room temperature
- Measure in a dark room



(4) Luminance uniformity (Whole screen area)

(Measuring Conditions)

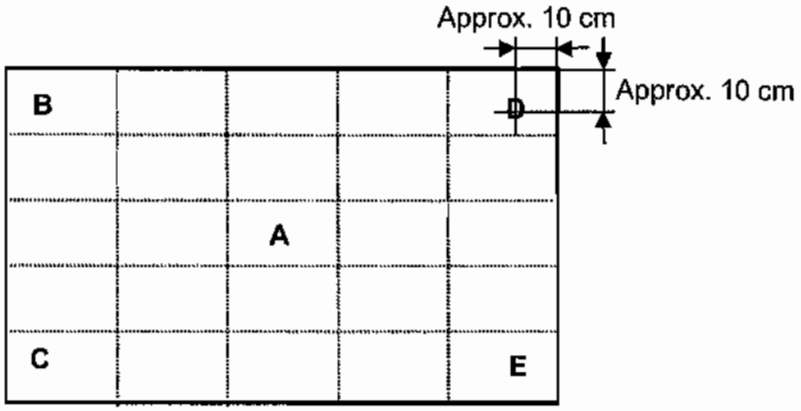
- Input signal: Video signal (60Hz, Standard mode, refer to Table 13, fv=59.94Hz and fh=31.47kHz)
- Display pattern: Full-screen white display (100% signal level)
- PLE condition: Internal-PLE operation
- Measuring position: Center and four corners (total 5 points)
- Definition of uniformity = $\frac{\text{Minimum luminance of 5 points}}{\text{Maximum luminance of 5 points}}$
- Measuring equipment: Color analyzer CA-100 (Minolta)
- Measuring temperature: Room temperature



(5) Color temperature

(Measuring conditions)

- Input signal: Video signal (60Hz, Standard mode, refer to Table 13, fv=59.94Hz and fh=31.47kHz)
- Display pattern: Full-screen white display (100% signal level)
- PLE condition: Internal-PLE operation
- Measuring position: Measure the center and four corners luminance (total 5 points) (Color temperature = Average of 5 points measurements)
- Measuring equipment: Color analyzer CA-100 (Minolta)
- Measuring temperature: Room temperature



5. DOT DEFECTS SPECIFICATIONS

Table 2. Dot defects specification			
	Display image	Allowed defect numbers	Allowed chained-dot defect
Bright dot defect (Note 1)	All area black	A zone: 2 defects max. (Note 1) B zone: 2 defects max. (Note 1)	No chained-dot defect allowed.
	All area 100% red All area 100% green All area 100% blue	A zone: 2 defects max. by each color, Total 3 defect max. for all colors B zone: 3 defects max. by each color, Total 5 defects max. for all colors	Vertically chained-dot: Chained-2-dot defect max. Horizontally chained-dot: No chained-dot allowed
Unlit dot defect	All area 100% red All area 100% green All area 100% blue	A zone: Total 4 defects max. for all colors B zone: Total 6 defects max. for all colors	----
	All area 100% white	----	Chained-2-dot defect max.

Note 1: The expected percentage of bright dot free defect panel at "All area black" display (0 bright dot defect in all area) is higher than 90%.

Note 2: Flickering bright dot defect is included in the Bright dot defect.

Note 3: Dot defect is specified with following A and B zones.

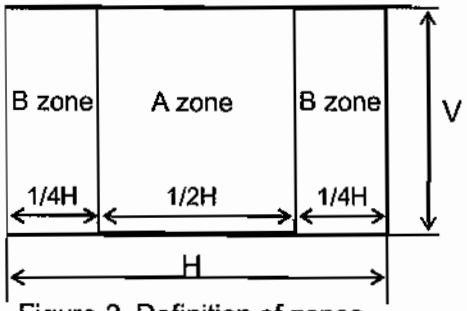


Figure 2. Definition of zones

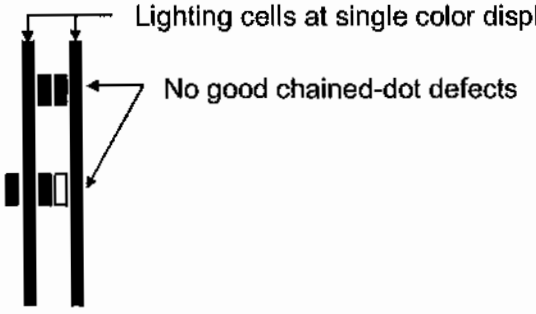
Note 4: Chained-dot in oblique direction or massed chained-dot are defined as follows.

 → Chained-3-dot defect

 → Chained-3-dot defect

 → Chained-4-dot defect

Note 5: Chained-dot defect at single color display is defined as follows.



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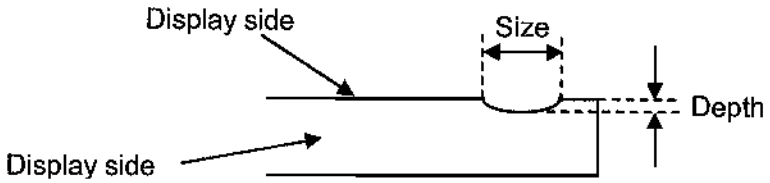
6. SCREEN SURFACE SPECIFICATION

(1) Dents on the screen glass

Size of dents	Depth of dents	Number of dents
Ø15mm or less	Less than 0.1mm	No restriction
	Equal or more than 0.1mm and less than 0.3mm	Maximum 3 pcs



(2) Scratches and bruises

When observe the display screen with following conditions, inconspicuous scratches and bruises are judged as good.

<Conditions>

1) Attach optical filter on the display screen.
2) Display image: full-white, full-red, full-green and full-blue
3) Observe distance and position: 1.5 meters from the panel, normal direction to the panel surface.

7. INPUT POWER SOURCE SPECIFICATION

7.1. Power source

(1) Sustain power supply

Table 3. Sustain power supply

Item	Symbol	MIN	TYP	MAX	Unit	Conditions/Remarks
Absolute maximum	---	---	---	210	V	---
Set-up voltage	Vs	180	---	200	V	Set-up voltage is specified by each module (Note 1)
Voltage stability	---	---	---	±1.0	%	---
Average current at Internal-PLE operation	Is		---	1.2	A	(Note 2)
Average current at External-PLE operation	---	---	---	1.9	A	(Note 2) , (Note 3)
Peak current	Isp	---	---	20	A	---
Voltage regulation	---	---	---	5	V	At peak current
Ripple/Noise	---	---	---	500	mVp-p	---

Note 1: Voltage should be set to the specified value, which is printed on the label attached to the module.

Note 2: Average current include rippled current.

Note 3: When PLE is set to maximum luminance with full-screen white display, or when PLE response has a delay and display image is changed from full-screen black to full-screen white at once, large current flows.
In these cases, maximum average current is limited at this MAX. value by the internal protection circuit.

Note 4: For safety purpose when excessive voltage and current to the above "Absolute maximum voltage" and/or "Peak current" are applied, it is essential to install over-voltage and over-current protection circuits in the Vs line of the power-supply.

(2) Data power supply

Table 4. Data power supply

Item	Symbol	MIN	TYP	MAX	Unit	Conditions/Remarks
Absolute maximum	---	---	---	75	V	---
Set-up voltage	Vd	60	---	70	V	Set-up voltage is specified by each module (Note 1)
Voltage stability	---	---	---	±1.5	%	---
Average current	Id		---	1.7	A	Varies depend on the display image (Note 2)
Peak current	Idp	---	---	7.0	A	---
Voltage regulation	---	---	---	2	V	At peak current
Ripple/Noise	---	---	---	300	mVp-p	---

Note 1: Voltage should be set to the specified value, which is printed on the label attached to the module.

Note 2: Average current that include rippled current.
While the period before limiter circuit start the operation (3 Vsync typical, 6 Vsync max.), 5 A of maximum current flows for initial 3V (3-Vsync. cycles) period. Power supply is required to support enough current in this period.

Note 3: Power limiter operates at 90W. Deviation range: ±15%.

Note 4: For safety purpose when excessive voltage and current to the above "Absolute maximum voltage" and/or "Peak current" are applied, it is essential to install over-voltage and over-current protection circuits in the Vd line of the power-supply.

(3) Logic power supply

Table 5. Logic power supply

Item	Symbol	MIN	TYP	MAX	Unit	Conditions/Remark
Absolute maximum	---	4.75	---	6.0	V	---
Voltage range (Note 1)	Vcc	4.9	5.1	5.3	V	---
Current (Note 2)	Icc	---	---	5.0	A	---
Peak current	Iccp	---	---	7.0	A	---
Ripple	---	---	---	30	mVp-p	---
Noise	---	---	---	300	mVp-p	---

Note 1: When use a long cable, applied voltage may be dropped because of its resistance. Specified voltage should be applied correctly at the input of the module side connector.

Note 2: Average current include its ripple.
This module has an automatic operation-stop function when malfunction is occurred. When the module stops the operation, logic current may reduce to almost zero (0). In this case even if logic current becomes zero, applied voltage should be kept to less than 6.0 volts.

(4) Power consumption at full-screen white display
140 W minimum, 180 W maximum
(Measuring conditions)
- Input signal: Video signal (60Hz, Standard mode, refer to Table 13, fv=59.94Hz and fh=31.47kHz)
- Display pattern: Full-screen white display (100% signal level)
- PLE condition: Internal-PLE operation
- Measuring temperature: Room temperature
- Power consumption = (Vs x Is)+(Vd x Id)+(Vcc x Icc)

Note: This power consumption does not indicate the Maximum power consumption.

(5) Capacitance attached at the power line inside of the PDP module.
5V line: 3000 to 3250 µF
Vd line: 1100 to 1300 µF
Vs line: 1700 to 2100 µF

7.2. Supplied Power and signal sequence

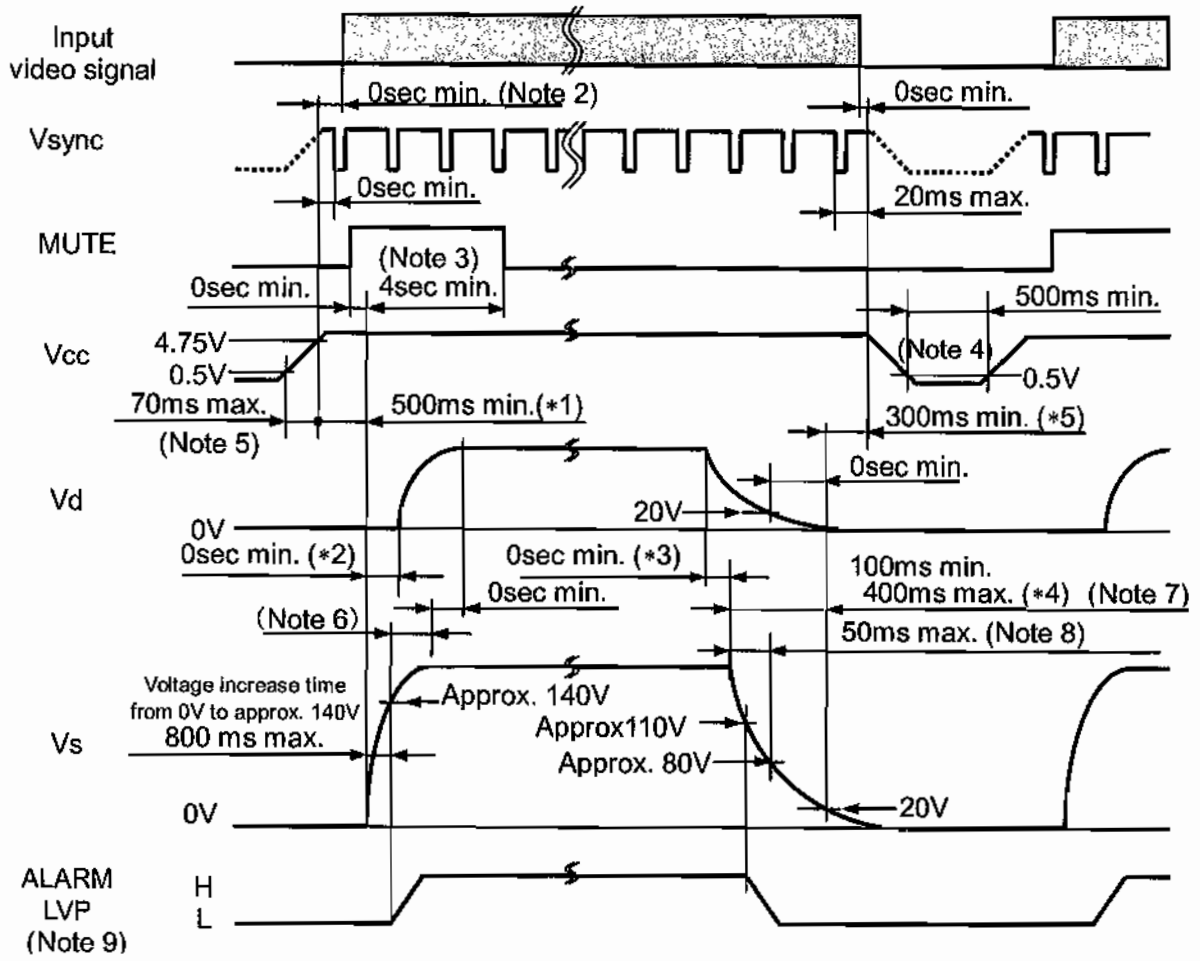


Figure 3. Supplied Power and signal sequence

Note 1: Power ON/OFF sequence is as follows (refer to the above sequence diagram):

Power ON sequence:

Vcc ON→500ms min.(*1)→Vs ON→0sec min. (*2)→Vd ON

Power OFF sequence:

Vd OFF→0sec min. (*3)→Vs OFF→400ms max.(*4)→300ms min.(*5)→Vcc OFF

(Caution)

If power sequence does not meet to the above sequence diagram, PDP drivers may have a permanent damage.

In order to decrease Vs and Vd voltages quickly to satisfy above sequence diagram, forced discharge circuits are essential in the power supply.

Note 2: Do not apply video signals before logic voltage (Vcc) is applied to the module.
(It is possible to set the output of LVDS transmitter (DS90C387) in high impedance status by using the "Power Down" function.)

Note 3: Initial set-up period when power on.
Since unexpected image may be displayed while this set-up period, display should be MUTED using MUTE signal that covers the period between the timing before Vs power-on and the timing minimum 4 seconds after Vs power-on.

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Note 4: Re-start (Power ON again) should be carried out minimum 0.5 second after Vcc decreases to 0.5V or less.
When Vcc drops o 4.9V or less because of commercial power brownout or other troubles, all supplied voltages (Vs, Vd and Vcc) should be once powered off.
When Vcc drops o 4.9V or less and recovered to the correct voltage, operation of the PDP might be stopped because of module internal protection circuit. In this case LVP and ALARM signals are outputted, power should be re-started after the power supply shut-down operation by these signals is released.

Note 5: When power supply is powered-on, Vcc voltage should be monotonously increased within 70ms (0.5V→4.75V). No fluctuation or no dip of the voltage is arrowed while Vcc is increased.

Note 6: While this period, since the discharge for display control starts gradually according to the rising of Vs voltage, momentary unexpected image may be displayed. In order to reduce this influence, it is recommended to set this period as short as possible (400ms or less).

Note 7: While this period, momentary unexpected image might be displayed. In order to reduce this affection, this period should be set between 100ms and 400ms.

Note 8: When power off, Vs voltage of this part should be dropped as quicker as possible (within 50ms), otherwise momentary unexpected image might be displayed.
This period is the rough guide line, please check at your actual set finally.

Note 9: LVP is the output signal for power supply shutdown when the trouble will happen in the circuit of PDP module.
When either ALARM or LVP signal is "L", high voltage should be shut down. However, when Vcc is applied at first, ALARM and LVP signals are kept "L" until Vs is applied. In order to enable "high voltage power supply" operation, the initial ALARM and LVP signals status "L" should be disregarded.
When ALARM signal is outputted, power supply operation should be locked not to ON until the reason of ALARM signal is solved.

8. INTERFACE SIGNAL

8.1. Interface configuration

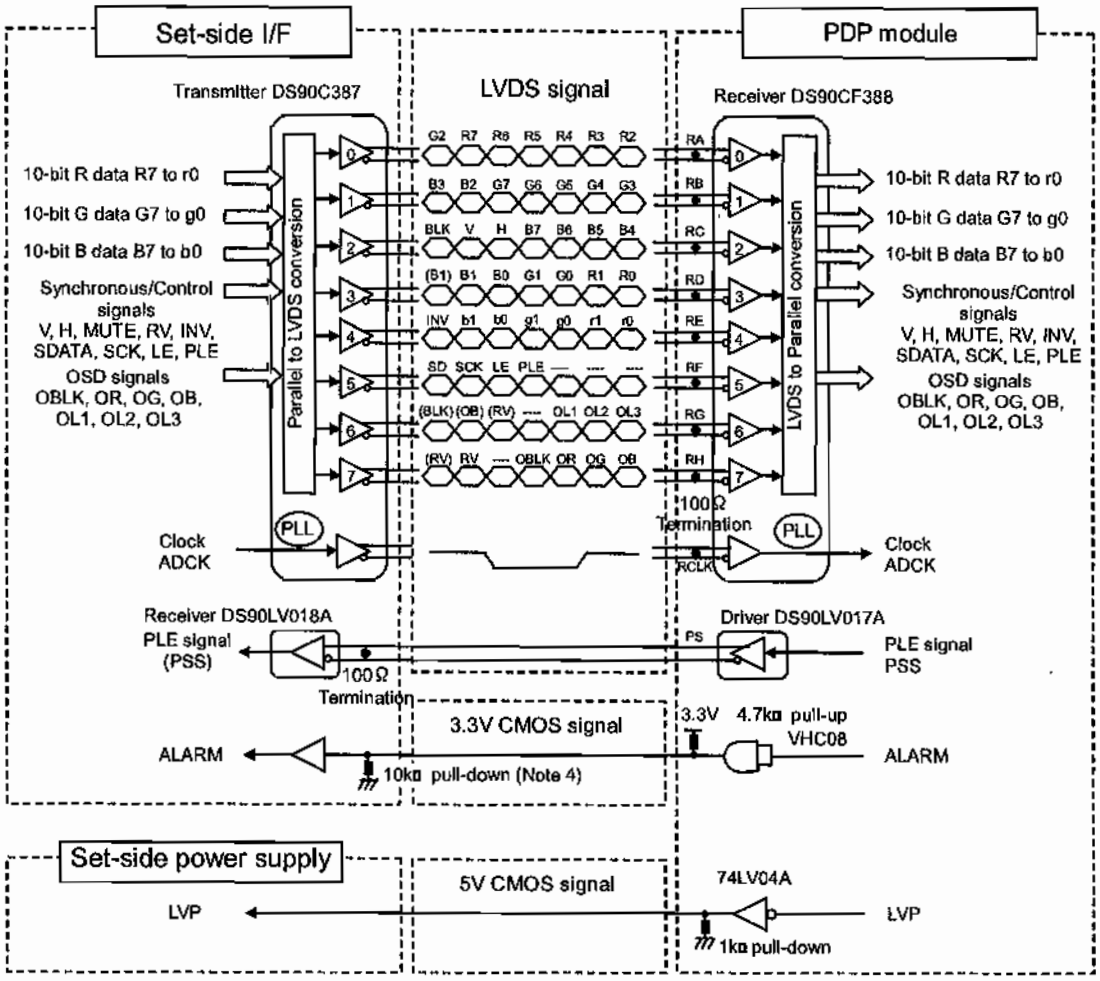

Figure 4. Interface configuration

Note 1: As for detail of LVDS interface, please refer to http:// www.national.com.

Note 2: More than 32.5MHz frequency of clock signal (ADCK) should be inputted continuously to the module while operation.

Note 3: No jitter is allowed in the clock signal, since input signals are latched-into the transmitter by the clock signal.

Note 4: ALARM signal should be terminated with 10kΩ or more of impedance.
For the failsafe function to the disconnection of interface cable, ALARM input of the Set-side I/F should be pull-down using around 10kΩ resistor.

Note 5: When either ALARM or LVP signal is "L", high voltage should be shut down. However, when Vcc is applied at first, ALARM and LVP signals are kept "L" until Vs is applied. In order to enable "high voltage power supply" operation, the initial ALARM and LVP signals status "L" should be disregarded.
When ALARM signal is outputted, power supply operation should be locked not to ON until the reason of ALARM signal is solved.

8.2. Electrical characteristics

(1) Interface signal absolute ratings

Ta=25°C, Vcc=5V

Table 6. Absolute ratings

Signal name			Item	Symbol	Rating	Unit
Input signals	LVDS	RA- to RH- RA+ to RH+ RCLK-,RCLK+	Input voltage	Vi	-0.3 to 3.6	V
			Input current	Ii	---	mA
Output signals	LVDS	PSS	Output voltage	Vo	-0.3 to 3.9	V
			Output current	Ii	---	mA
	3.3V CMOS	ALARM	Output voltage	Vo	-0.5 to 3.5	V
			Output current	Io	±20	mA
	5V CMOS	LVP	Output voltage	Vo	-0.5 to 5.5	V
			Output current	Io	±25	mA

(2) Interface signal electrical characteristics

Ta=25°C, Vcc=5V

Table 7. Electrical characteristics

Signal	Item	Symbol	Condition	MIN	TYP	MAX	Unit
LVDS	Differential input high threshold	V_{TH}	V_{CM}=1.2V	---	---	100	mV
	Differential input low threshold	V_{TL}	V_{CM}=1.2V	-100	---	---	mV
	Input current (Note 1)	I_{IN}	V_{IN}=+2.4/GND	---	---	±10	□A
	Output high voltage	V_{OH}	R_L=100□	---	1.4	1.6	V
	Output low voltage	V_{OL}	R_L=100□	0.9	1.1	---	V
3.3V CMOS	Output high voltage	V_{OH}	Io=-1mA	2.4	---	---	V
	Output low voltage	V_{OL}	Io=1mA	---	---	0.4	V
5V CMOS	Output high voltage	V_{OH}	Io=-6mA	3.8	---	---	V
	Output low voltage	V_{OL}	Io=6mA	---	---	0.6	V

Note 1: Together with this Inputs current, additional current through 10k□ termination flows to each LVDS channel.

8.3. Signal functions

(1) Input signal function of LVDS transmitter

Table 8. Input signal function of LVDS transmitter (DS90C387)

Signal name	Function	Remarks
R7 to R0	Upper 8-bit red video signals (Note 1)	(R7: MSB)
G7 to G0	Upper 8-bit green video signals (Note 1)	(G7: MSB)
B7 to B0	Upper 8-bit blue video signals (Note 1)	(B7: MSB)
r1, r0	Lower 2-bit red video signals when 9,10-bit input (Note 1)	Fix to "L" when not use
g1, g0	Lower 2-bit green video signals when 9,10-bit input (Note 1)	Fix to "L" when not use
b1, b0	Lower 2-bit blue video signals when 9,10-bit input (Note 1)	Fix to "L" when not use
ADCK	Clock for video signal	Active edge programmable
Hsync	Horizontal synchronous signal	Pulse width=4T_{ADCK} min. (negative)
Vsync	Vertical synchronous signal	Pulse width=1H min. (negative)
MUTE	Video mute signal. "H" when mute (all screen black display)	Input per video frame unit
RV	Internal test use	Fix to "L"
INV	Internal test use	Fix to "L"
PLE	When set to "L", PSS output signal appears.	
SDATA	Serial data input synchronized with SCK.	Latched with rising edge of SCK
SCK	Clock for serial data signal (1MHz maximum)	Effective when LE or PLE become L
LE	When set to "L", SDATA become enable to input,	Normally set to "H"
OR	OSD red signal	Fix to "L" when not use
OG	OSD green signal	Fix to "L" when not use
OB	OSD blue signal	Fix to "L" when not use
OL1	OSD luminance level signal 1	Fix to "L" when not use
OL2	OSD luminance level signal 2	Fix to "L" when not use
OL3	OSD luminance level signal 3	Fix to "L" when not use
OBLK	OSD mute signal (video signal of pointed pixel is muted)	Fix to "L" when not use

Note 1: Assignment of input video signal

Input signal bits	R7 G7 B7	R0 G0 B0	r1 g1 b1	r0 g0 b0
8-bit video signal	MSB	LSB	Ignored	Ignored
9-bit video signal	MSB		LSB	Ignored
10-bit video signal	MSB			LSB

MSB: Most Significant Bit
LSB: Least Significant Bit

(2) Output signal function of LVDS receiver

Table 9. Output signal function of LVDS receiver (DS90LV018A)

Signal name	Function	Remarks
PSS	Average luminance level signal of video input (for External-PLE control)	Output signal synchronized with SCK when PLE signal input of DS90C387 is set to "L".

(3) Input signal function of PDP module

Table 10. Input signal function of PDP module (I/O mean the Input/Output))

Connector	Signal name	I/O	Function	Signal level
Interface connector	RA-	I	Video signal input A-	LVDS
	RA+	I	Video signal input A+	LVDS
	RB-	I	Video signal input B-	LVDS
	RB+	I	Video signal input B+	LVDS
	RC-	I	Video signal input C-	LVDS
	RC+	I	Video signal input C+	LVDS
	RD-	I	Video signal input D-	LVDS
	RD+	I	Video signal input D+	LVDS
	RE-	I	Video signal input E- (lower 2-bit when 10-bit input)	LVDS
	RE+	I	Video signal input E+ (lower 2-bit when 10-bit input)	LVDS
	RF-	I	Mode signal input F-	LVDS
	RF+	I	Mode signal input F+	LVDS
	RG-	I	OSD signal G-	LVDS
	RG+	I	OSD signal G+	LVDS
	RH-	I	OSD signal F-	LVDS
	RH+	I	OSD signal F+	LVDS
	RCLK-	I	LVDS clock -	LVDS
	RCLK+	I	LVDS clock +	LVDS
	PS-	O	PSS signal -	LVDS
	PS+	O	PSS signal +	LVDS
	ALARM	O	Alarm signal for abnormal operation ("L" in alarm) (Note 1)	3.3V CMOS
Power connector	LVP	O	Alarm signal for abnormal operation ("L" in alarm) (Note 1)	5V CMOS

Note 1: When ALARM and LVP outputs turn to "L" level, high voltage power input (Sustain power supply voltage: Vs, and Data power supply voltage: Vd) should be switched off immediately.

(4) Pin assignment of LVDS transmitter

Table 11. Pin assignment of LVDS transmitter (DS90387)

Pin No.	I/O	Terminal name of NS	Pin assignment of Pioneer	Remarks	Pin No.	I/O	Terminal name of NS	Pin assignment of Pioneer	Remarks
1	I	G11	G3		51	-	LVDSGND	GND(LVDS)	
2	I	G10	G2		52	-	GND	GND	
3	I	R17	R1		53	-	Vcc	Vcc	
4	I	R16	R0	LSB when 8-bit input	54	I	Hsync	Hsync	
5	I	R15	R7	MSB	55	I	Vsync	Vsync	
6	I	R14	R6		56	I	DE	MUTE	
7	I	R13	R5		57	I	B27	RV	Connect to GND
8	I	R12	R4		58	I	B26	RESERVE	Connect to GND
9	I	R11	R3		59	I	B25	RESERVE	Connect to GND
10	I	R10	R2		60	I	B24	OL1	OSD function
11	I	CLKIN	ADCK		61	I	B23	OL2	OSD function
12	-	PLL Vcc	Vcc (PLL)		62	I	B22	OL3	OSD function
13	-	GND	GND		63	I	B21	SDATA	
14	I	PRE	PRE	Open	64	I	B20	SCK	
15	I	PLLSEL	PLLSEL	Connect to Vcc	65	I	G27	OBLK	OSD function
16	-	PLLGND	GND (PLL)		66	I	G26	OR	OSD function
17	-	PLLGND	GND (PLL)		67	-	Vcc	Vcc	
18	-	PLL Vcc	Vcc (PLL)		68	-	GND	GND	
19	-	PLLGND	GND (PLL)		69	I	G25	LE	
20	I	R_FB	R_FB	ADCK active edge selection	70	I	G24	PLE	
21	I	R_FDE	R_FDE	Connect to GND	71	I	G23	---	Connect to GND
22	I	$\overline{PD}$	$\overline{PD}$	H: LVDS output ON L: LVDS output OFF	72	I	G22	---	Connect to GND
23	I	DUAL	DUAL	Connect to Vcc	73	I	G21	---	Connect to GND
24	I	BAL	BAL	Connect to GND	74	I	G20	fNV	Connect to GND
25	-	LVDSGND	GND(LVDS)		75	I	R27	OG	OSD function
26	I	CLK2P/NC	N/C	Open	76	I	R26	OB	OSD function
27	I	CLK2M/NC	N/C	Open	77	I	R25	b1	LSB when 9-bit input
28	O	A7P	RH+		78	I	R24	b0	LSB when 10-bit input
29	O	A7M	RH-		79	I	R23	g1	LSB when 9-bit input
30	-	LVDS Vcc	Vcc (LVDS)		80	I	R22	g0	LSB when 10-bit input
31	O	A6P	RG+		81	I	R21	r1	LSB when 9-bit input
32	O	A6M	RG-		82	-	Vcc	Vcc	
33	O	A5P	RF+		83	-	GND	GND	
34	O	A5M	RF-		84	I	R20	r0	LSB when 10-bit input
35	-	LVDSGND	GND (LVDS)		85	I	B17	B1	
36	O	A4P	RE+		86	I	B16	B0	LSB when 8-bit input
37	O	A4M	RE-		87	I	B15	B7	MSB
38	O	A3P	RD+		88	I	B14	B6	
39	O	A3M	RD-		89	I	B13	B5	
40	-	LVDS Vcc	Vcc (LVDS)		90	I	B12	B4	
41	O	CLK1P	RCLK+		91	I	B11	B3	
42	O	CLK1M	RCLK-		92	I	B10	B2	
43	-	LVDSGND	GND(LVDS)		93	I	B17	G1	
44	O	A2P	RC+		94	I	G16	G0	LSB when 8-bit input
45	O	A2M	RC-		95	I	G15	G7	MSB
46	O	A1P	RB+		96	I	G14	G6	
47	O	A1M	RB-		97	-	Vcc	Vcc	
48	-	LVDS Vcc	Vcc (LVDS)		98	-	GND	GND	
49	O	A0P	RA+		99	I	G13	G5	
50	O	A0M	RA-		100	I	G12	G4	

NS means National Semiconductor Corporation

8.4. Module I/O signal interface circuits

Following show the PDP module I/O signal interface circuits and connector's pin assignment.

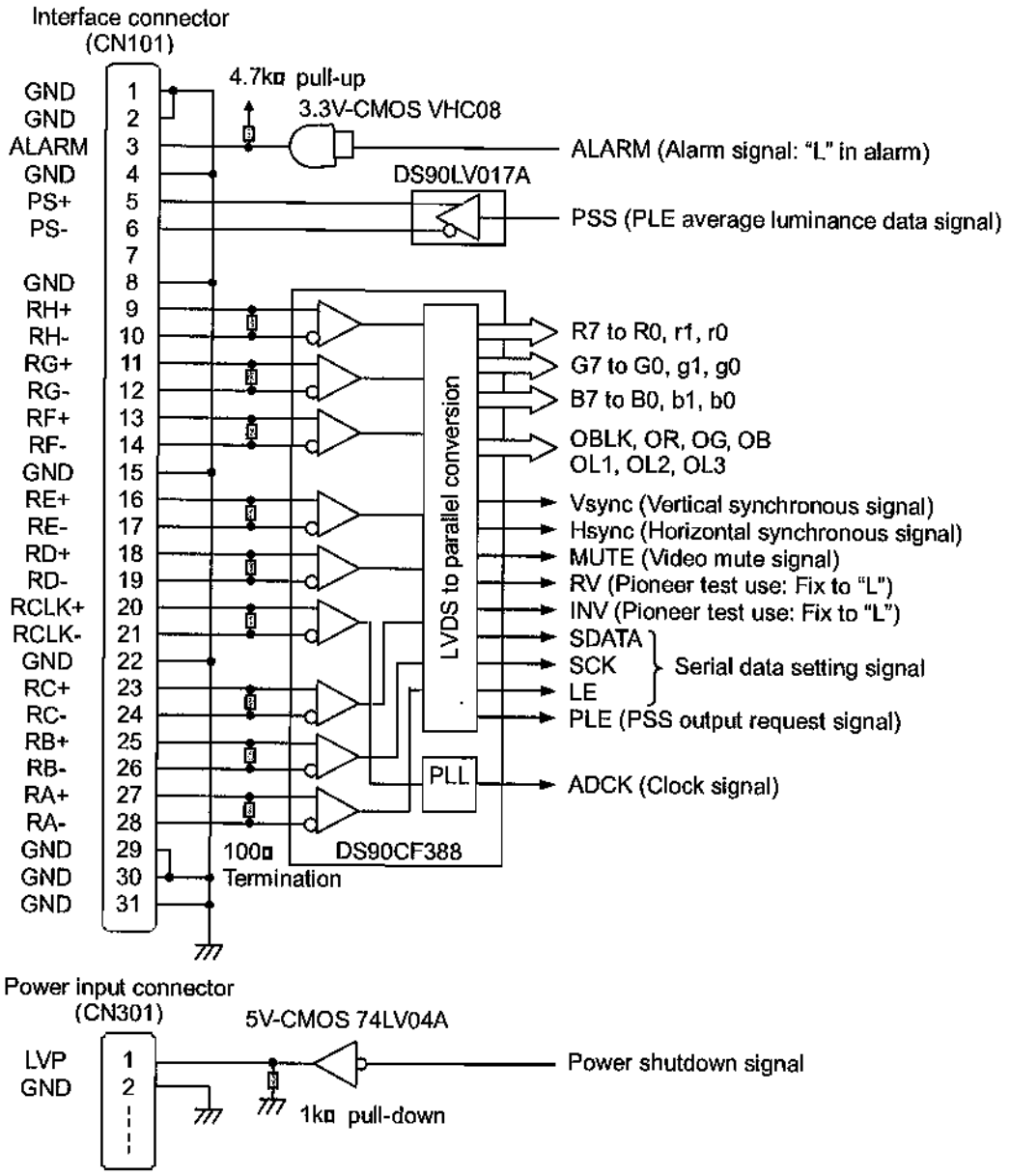

Figure 5. Module I/O signal interface circuits

9. DISPLAY MODE, PLE CONTROL AND VIDEO PROCESSING FUNCTIONS

This PDP module has setup functions of the display mode, the PLE control data and the video processing. Each function can be set up through the SDATA input using a "packet" or a "dynamic packet".

This PDP module has display modes corresponding to the 50Hz and the 60Hz input signals. One of these display modes can be selected by setting up the data in the display mode packet.

When use the External-PLE function, PSSC (PLE luminance level control signal) can be inputted to the module through the PLE dynamic packet (refer to item 11.1).

This PDP module has the built-in color space conversion, inverse gamma function and error diffusion function. Characteristics of each function can be set up by the data supplied through the dynamic packet (packet which can input the data by every video flame).

(1) Kinds of the packet and the dynamic packets.

- Display mode packet
- PLE control packet
- Error diffusion packet
- Color space conversion
- Inverse gamma packet

(2) Identifier of packet and dynamic packet data

Table 12. Identifier of packet and dynamic packet data

Packet data	Identifier bits												Bit length
	D0	D1	D2	D3	D4	D5	---	D8	---	D10	---	D47	
Display mode	0	*Set-up of display mode*					---	0	---	0	---	0	64
PLE control	1	1	1	1	1	1	---	1	---	1	---	-	16
Color space conversion	1	0	1	1	1	0		1		1			80
Inverse gamma (16-bit accuracy)	1	1	0	1	0	0	---	1	---	1	---	-	456
Inverse gamma (14-bit accuracy)	1	1	0	1	0	1	---	1	---	1	---	-	408
Inverse gamma (12-bit accuracy)	1	1	0	0	1	1	---	1	---	1	---	-	360
Inverse gamma (10-bit accuracy)	1	1	0	1	1	0	---	1	---	1	---	-	312
Error diffusion	1	1	0	0	0	0	---	1	---	1	---	-	32

"1" means high-level "H", "0" means low-level "L"

(3) Packet data input timing

It is inhibited to input packet/dynamic packet data while 5μS after falling edge of Vsync.

Minimum 1 micro second interval is necessary between packets and PSS output period.

It is essential to input the mode packet data at any time. When some other functions are not be used, it is not required to input the dynamic packet data of those functions.

Every packet can be inputted in random order. However when use the External-PLE function, it is recommended to give a priority to the PLE control packet, because PLE operation has a limitation in response time.

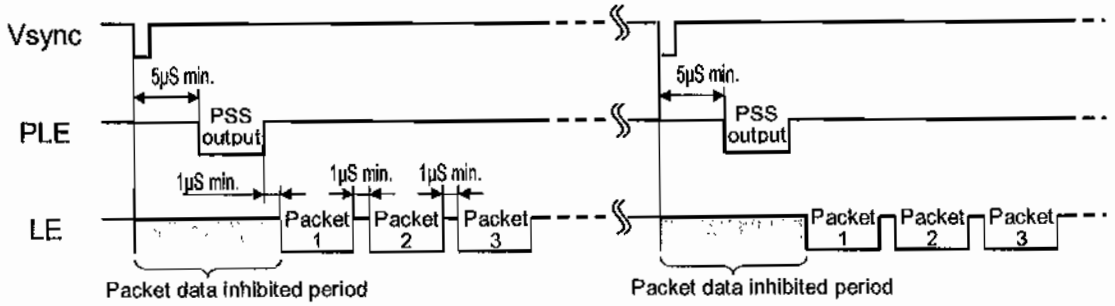

Figure 6. Packet data input timing (in case use External-PLE function)

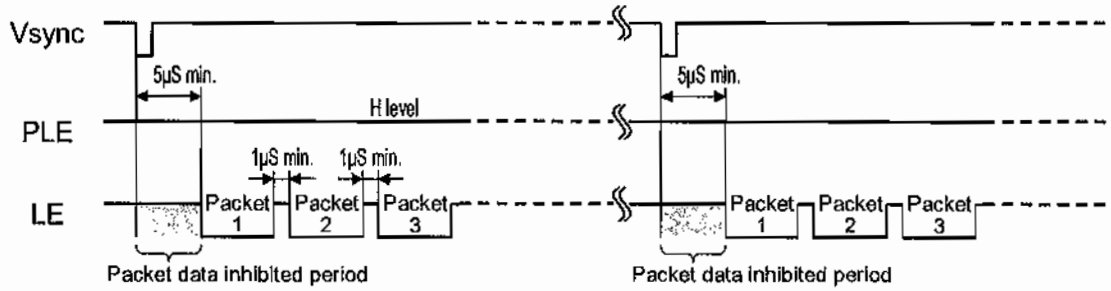

Figure 7. Packet data input timing (in case not use External-PLE function)

9.1. Set-up of packet and dynamic packet

When set-up the packet and dynamic packet data, specified bit length data is inputted as the SDATA synchronized with the SCK clock pulse.

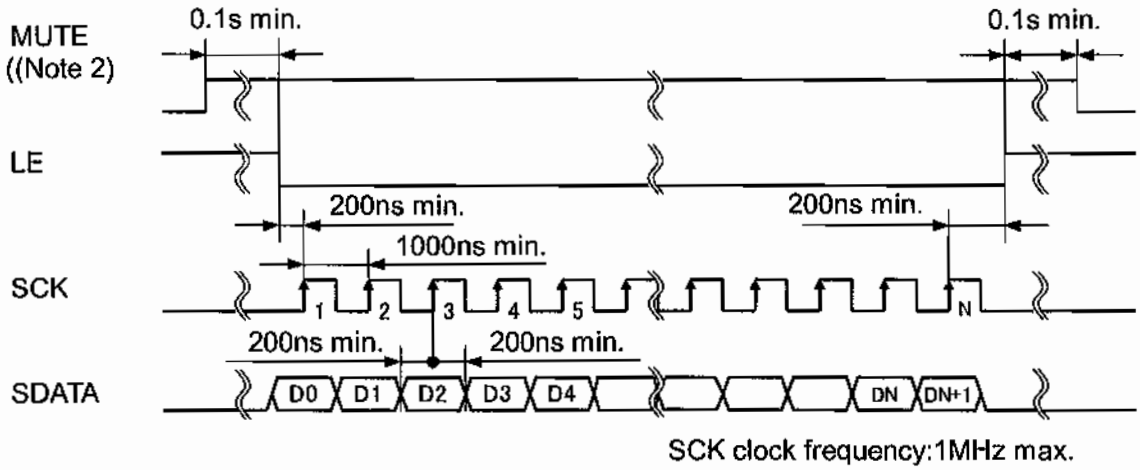

Figure 8. Input timing of packet / dynamic packet data

Set-up Sequence:

(1) Set LE (load enable) to "L" level.
(2) Enter the packet and/or the dynamic packet data (SDATA) into the module synchronizing with the positive edge of serial clock signal (SCK).
(3) Set LE to "H" level.

Note 1: Display mode packet data should be refreshed at least in every 5 seconds or less.

Note 2: When change the display mode packet data from previous data, input the MUTE signal to mute the video image.
When input the same display mode packet data periodically, do not input the MUTE signal, because muting of video image makes flickering of the video image.

Note 3: Entered SDATA becomes effective at the falling edge of the Vsync signal after "LE" signal is changed to "H" level.

Note 4: When the specified bit-length SDATA is inputted synchronously with SCK clock while LE is "L" level period, this SDATA becomes effective. When SCK clocks number is not equal to the specified bit-length of the SDATA, entered SDATA is invalid and ignored.

Note 5: Initial SDATA should be inputted while MUTE is "H" period after Sustain voltage (Vs) and Data voltage (Vd) are raised-up (Refer to the Supplied Power and signal sequence).
When SDATA is inputted while Vs and/or Vd is rising-up, malfunction of SDATA input might be happen because of noise from power source

9.2. Display mode setting function

Using display mode packet, it is possible to set-up Display picture modes (50Hz, 60Hz), Horizontal frequency, Vertical frequency, PLE mode and Video processing functions ON/OFF.

(1) Structure and se-up of display mode packet

Table 13. Structure and se-up of display mode packet

Data	Data name	Setup Value	Remarks
D0	MODE ID	L	Display mode packet identify bit
D1	CODE4	Refer to Table 14	Set-up of display picture mode
D2	CODE3		
D3	CODE2		
D4	CODE1		
D5	CODE0		
D6	---	L	Pioneer test use (Fixed)
D7	LIFE	L: Normal H: Long life	Selection of luminance mode
D8	MODE ID	L	Display mode packet identify bit
D9	SELFPLEH	H: Internal-PLE L: External-PLE	Selection of PLE control mode
D10	MODE ID	L	Display mode packet identify bit
D11	FV2	Refer to Table 14	Set-up of vertical frequency
D12	FV1		
D13	FV0		
D14	DISPLINE2	H	Set-up of 768-line display mode
D15	DISPLINE1	L	
D16	DISPLINE0	H	
D17	DISPDOT2	H	Set-up of 1024-pixel/line display mode
D18	DISPDOT1	L	
D19	DISPDOT0	H	
D20	---	L	Display start position. Start 3rd-line from the reading edge of vertical synchronous signal. (Fixed)
D21	---	L	
D22	---	L	
D23	---	L	
D24	---	L	
D25	---	L	
D26	---	L	
D27	---	L	
D28	VDELAY 1	H	
D29	---	L	
D30	---	L	
D31	---	L	

Data	Data name	Setup Value	Remarks
D32	HDELAY 64	H	Display starts position. Start 64th-pixel from the reading edge of horizontal synchronous signal. (Fixed)
D33	---	L	
D34	---	L	
D35	---	L	
D36	---	L	
D37	---	L	
D38	HDELAY 1	L	
D39	---	H	Pioneer test use (Fixed)
D40	---	L	
D41	---	L	
D42	---	L	
D43	---	L	
D44	---	L	
D45	---	L	
D46	---	L	
D47	MODE ID	L	Display mode packet identify bit
D48	INPUT Bit1	Bit-No. of input video signal	Bit-No. 8 9 10 D48 L L H D49 L H L
D49	INPUT Bit2		
D50	COLOR SPACE	H:ON L:OFF	Color space conversion function
D51	GAMMA	H :ON L :OFF	Inverse gamma function
D52	ED	H :ON L :OFF	Error diffusion function
D53	---	L	Pioneer test use (Fixed)
D54	CODE6	Refer to Table 13	Set-up of display picture mode
D55	CODE5		
D56	OSD	H :ON L :OFF	OSD function
D57	RESERVED	L	Reserve bits
D58	RESERVED	L	
D59	RESERVED	L	
D60	RESERVED	L	
D61	RESERVED	L	
D62	RESERVED	L	
D63	RESERVED	L	

(2) Setup of display picture mode

Table 14. Display picture mode set-up table

Display picture mode		Mode set-up data										Vertical synchronous frequency range	Remarks
		D54	D55	D1	D2	D3	D4	D5	D11	D12	D13		
		CODE6	CODE5	CODE4	CODE3	CODE2	CODE1	CODE0	FV2	FV1	FV0		
Video 60Hz (Note 1)	Standard mode (8-bit)	L	H	L	L	L	L	H	L	L	H	55 to 64Hz (Note 3)	
	High gradation mode (9-bit)	L	H	L	L	L	H	L	L	L	H	55 to 64Hz (Note 3)	
	High gradation mode (10-bit)	L	H	L	L	L	H	H	L	L	H	55 to 64Hz (Note 3)	
Video 50Hz (Note 2)	Standard mode (8-bit)	L	L	L	L	L	L	H	L	L	L	46 to 54Hz (Note 3)	
	High gradation mode (9-bit)	L	L	L	L	L	H	L	L	L	L	46 to 54Hz (Note 3)	

Note 1: LSB is deleted when the frequency is over about 61Hz.
Note 2: LSB is deleted when the frequency is over about 51Hz.
Note 3: When vertical synchronous frequency is over than these frequency ranges, average sustain frequency is set into the minimum, and get into the low luminance mode.

When change the display picture mode from different number display bit modes, mute the video image using the MUTE signal as follows.
If the MUTE signal is not inputted, irregular video image such as flickering may be displayed.

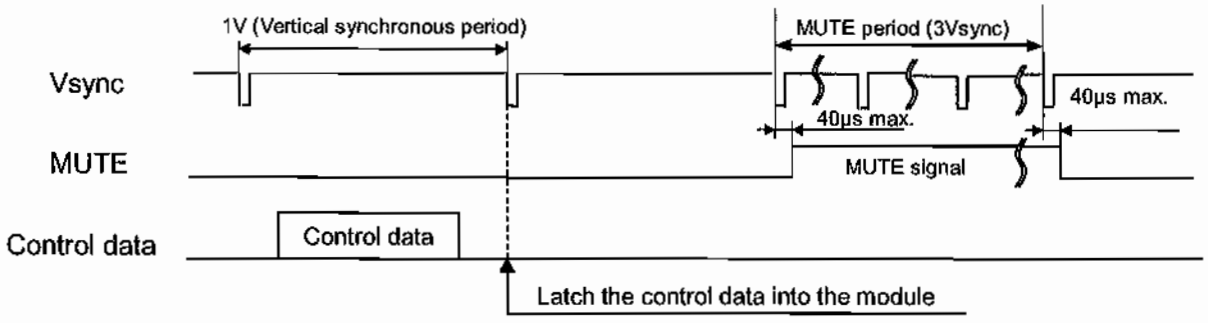

Figure 9. Mute signal input timing

10. INPUT VIDEO SIGNAL

10.1. Input video signal specifications

This color PDP module input the progressive (non-interlace) digital video signals.
Input signal specifications to the LVDS transmitter (DS90C387) are shown in following table.

Table 15. Input video signal specifications to the LVDS transmitter (DS90C387)

Items		Specifications
Effective pixels numbers		1024 (horizontal) × 768(vertical)
RGB input video signal (Note1)		Progressive signal 8, 9 or 10-bit input
Clock (ADCK)	Frequency	32.5MHz to 88MHz
	Others	Duty: 40 to 60% Setup time: 2.7ns min. Hold time: 0ns min. Continuous pulse is required Image is displayed from 64th clock video data signal.
Horizontal synchronous signal (Hsync) (Note 2)	Frequency	61kHz max.
	Others	Image is displayed from 3rd line video data signal. Minimum 4-clock of Hsync's "L" (low level) period is required. Minimum 4-clock of Hsync's "H" (high level) period is required.
Vertical synchronous signal (Vsync) (Note 2)	Frequency	50Hz mode: 46Hz to 54Hz (LSB is deleted when the frequency is over about 51Hz.) 60Hz mode: 55Hz to 64Hz (LSB is deleted when the frequency is over about 61Hz.)
	Others	Minimum 1H of Vsync's "L" (low level) period is required. Minimum 4H of Vsync's "H" (high level) period is required.
Limit of clock numbers in 1H period		1430 ≤ Number of clock pulse in 1H period ≤1800 Number of clock pulse in 1H period should be EVEN number.
Limit of Hsync pulse (line) numbers in 1V period		775 ≤ Number of Hsync pulse in 1V period ≤ 1280 (More than 4Hsync pulses period is required after display area.)

Note 1: Picture image on the PDP becomes the selected bit-width image from table 14 independent of the bit-width of the input video signal. (Refer to table 16.)
Note 2: Falling transitions of Hsync and Vsync should be taken into the LVDS transmitter synchronizing within the same ADCK timing (refer to figure 11).
Note 3: "1H" means the 1 cycle period of Hsync (Horizontal synchronous signal).
Note 4: "1V" means the 1 cycle period of Vsync (Vertical synchronous signal).

10.2. Relations between bit-width of input video signal and gray scale of display image

Table 16 Relations between bit-width of input video signal and gray scale of display image

	Setting						Bit-width of output video signal from signal processing function		Display image
	Bit-width of selected display picture mode from Table 13	Display mode packet data in Table 12					Output from inverse gamma	Output from error diffusion. (Least 2 bits of input signals are diffused in these output signals.)	
		Inverse gamma	Error diffusion	Selection of input video signal bit-width					
		D51	D52	D48	D49	Bit-width			
In case do not use the inverse gamma nor error diffusion functions	8-bit	L (OFF)	L (OFF)	L	L	8-bit	---	---	8-bit (256 gray scale) video image
	9-bit	L (OFF)	L (OFF)	L	H	9-bit	---	---	9-bit (512 gray scale) video image
	10-bit	L (OFF)	L (OFF)	H	L	10-bit	---	---	10-bit (1024 gray scale) video image
In case use the inverse gamma function only	8-bit	H (ON)	L (OFF)	L	L	8-bit	10-bit	---	8-bit (256 gray scale) video image
				L	H	9-bit	11-bit		
				H	L	10-bit	12-bit		
	9-bit	H (ON)	L (OFF)	L	L	8-bit	10-bit	---	9-bit (512 gray scale) video image
				L	H	9-bit	11-bit		
				H	L	10-bit	12-bit		
	10-bit	H (ON)	L (OFF)	L	L	8-bit	10-bit	---	10-bit (1024 gray scale) video image
				L	H	9-bit	11-bit		
				H	L	10-bit	12-bit		
In case use the error diffusion functions only	8-bit	L (OFF)	H (ON)	L	L	8-bit	---	6-bit video signal	Equiv. 8-bit video image
				L	H	9-bit	---	7-bit video signal	Equiv. 9-bit video image
				H	L	10-bit	---	8-bit video signal	Equiv. 10-bit video image
	9-bit	L (OFF)	H (ON)	L	L	8-bit	---	6-bit video signal	Equiv. 8-bit video image
				L	H	9-bit	---	7-bit video signal	Equiv. 9-bit video image
				H	L	10-bit	---	8-bit video signal	Equiv. 10-bit video image
	10-bit	L (OFF)	H (ON)	L	L	8-bit	---	6-bit video signal	Equiv. 8-bit video image
				L	H	9-bit	---	7-bit video signal	Equiv. 9-bit video image
				H	L	10-bit	---	8-bit video signal	Equiv. 10-bit video image
In case use the inverse gamma and error diffusion functions	8-bit	H (ON)	H (ON)	L	L	8-bit	10-bit	8-bit video signal	Equiv. 10-bit video image
				L	H	9-bit			
				H	L	10-bit			
	9-bit	H (ON)	H (ON)	L	L	8-bit	11-bit	9-bit video signal	Equiv. 10-bit video image
				L	H	9-bit			Equiv. 11-bit video image
				H	L	10-bit			
	10-bit	H (ON)	H (ON)	L	L	8-bit	12-bit	10-bit video signal	Equiv. 10-bit video image
				L	H	9-bit			Equiv. 11-bit video image
				H	L	10-bit			Equiv. 12-bit video image

equiv. =equivalent

10.3. Display position

Relations between Clock pulse (ADCK), Synchronous signals, Video signals and display position are as follows.

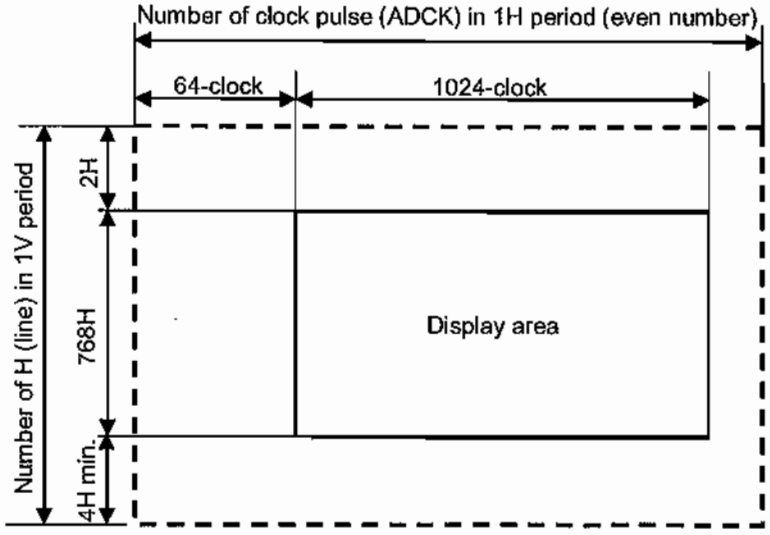

Figure 10. Display position

10.4. Video signal input timing

Following chart show the signal input timing to the LVDS transmitter (DS90C387).

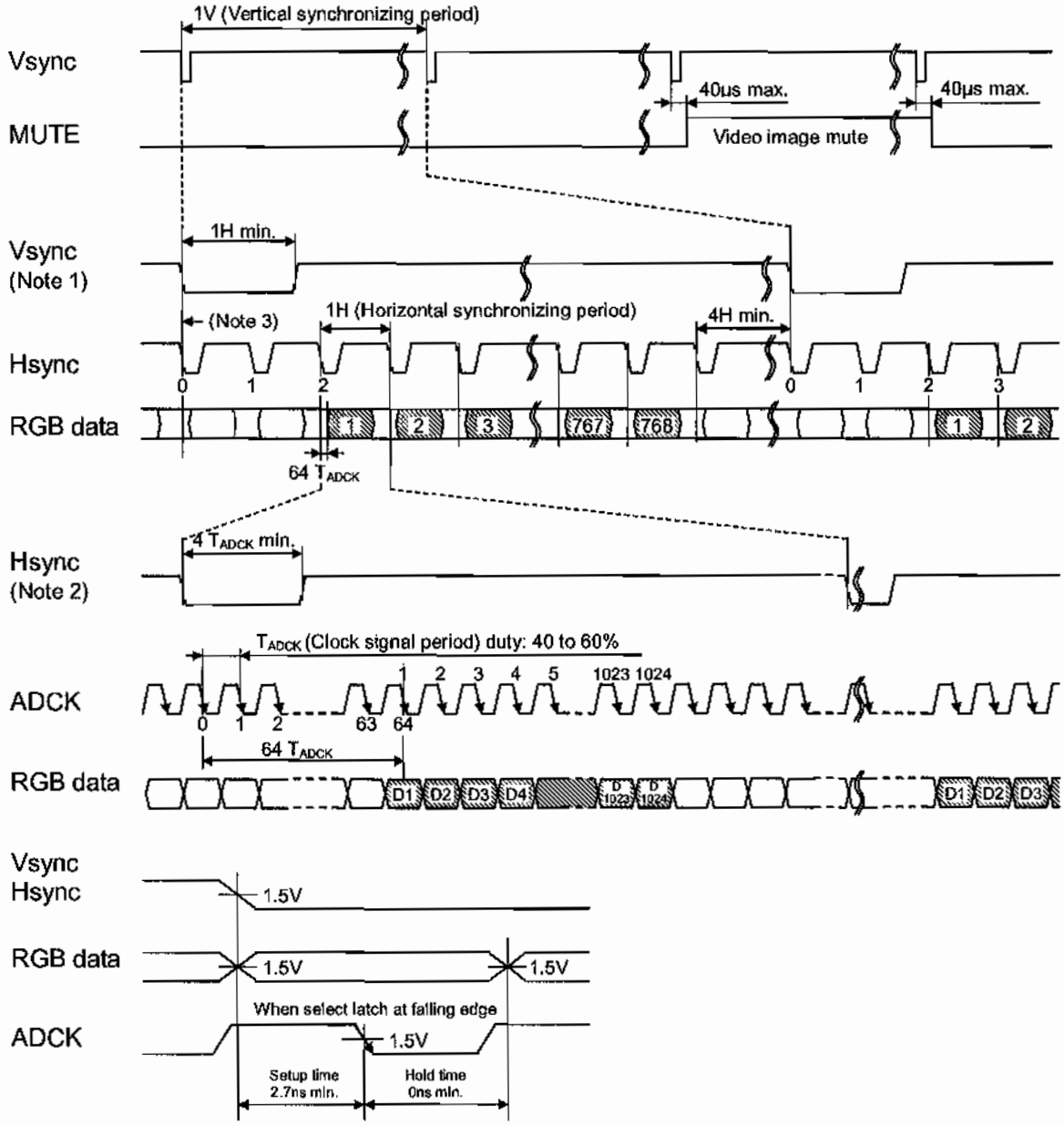

Figure 11. Input timing of LVDS transmitter DS90C387

Note 1: 1 cycle of Vsync (1V period) should be 775 Hsync periods or more.
"L (low level)" period of Vsync pulse should be 1 Hsync periods or more.
"H (high level)" period of Vsync pulse should be 4 Hsync periods or more
Note 2: 1 cycle of Hsync (1H period) should be 998 T_{ADCK} periods or more.
"L (high level)" period of Hsync pulse should be $4T_{ADCK}$ periods or more.
"H (high level)" period of Hsync pulse should be $4T_{ADCK}$ periods or more.
Note 3: Falling transitions of Hsync and Vsync should be taken into the LVDS transmitter synchronizing within the same ADCK timing.

11. PLE (Peak Luminance Enhancement) FUNCTION

The PLE function makes it possible to increase the luminance of video flame when the input signal level is low (include the case, when there are some high level input signal regions), and to decrease the luminance of video flame when the input signal level is high (include the case, when there are some low level input signal regions). This function can realize an improvement of the contrast and a reduction of the power consumption.

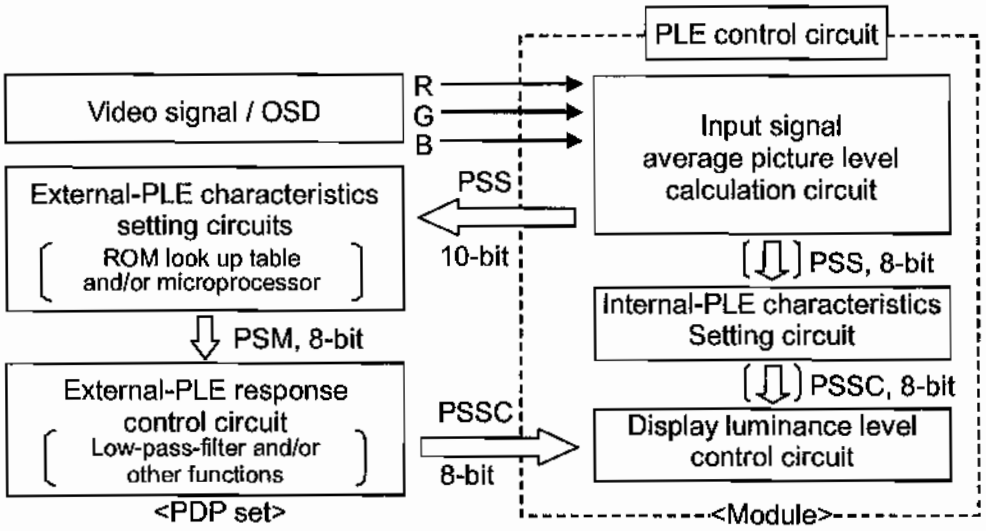

Figure 12. Configuration of PLE circuit

This PDP module has two PLE operation modes, built-in PLE operational function (Internal-PLE mode) and externally characteristics settable and controllable PLE operational function (External-PLE mode). These two modes can be selected by the mode control signal.

[Internal-PLE mode]
Because "Internal-PLE" uses built-in PLE function in the PDP module itself, it can realizes one of the best PLE characteristics in the image such as contrast, power consumption, etc. without any additional circuit. This mode is very convenient, and it is recommended to be utilized this function actively

[External-PLE mode]
The External-PLE can set the PLE characteristics freely within the allowed setting area.
However PLE characteristic gives influences on the performance and reliability, because it is concerned not only with the display characteristics but also with the power consumption and the generated heat.
Therefore, when use the External-PLE, it is essential that both companies (customer and Pioneer) should check and confirm followings each other, and conclude written agreement that both companies have no problem with the customer's External-PLE characteristics.
When use the External-PLE without the written agreement, it void the warranty.

1) Customer discloses its designed PLE curve to Pioneer.
2) Both of customer and Pioneer investigate and confirm about the PLE curve that it makes no problem on the display image quality of the PDP module (temperature characteristics, PDP panel write-ability characteristic, etc), reliability and other characteristics.

3) After both companies confirm to have no problem on the PLE curve, both companies conclude a written agreement that both companies have no problem when apply the PLE curve designed by the customer.

Caution 1: When setup the External-PLE control data outside of the allowed setting area, input PLE control data is forced to change within the allowed setting area by the limiter circuit in the module.

Caution 2: Power consumption and generated heat of PDP module varies depending on the setting values of the PLE characteristic. Therefore it is very important to check and confirm that each component and panel of the PDP module are cooled correctly within the specified temperature, and to optimize the cooling design with the assembled state in the PDP set.

Characteristics of Internal-PLE

As shown in below figure, Internal-PLE has a characteristic that increases the luminance level when the input video signal level is low, and reduces the maximum power by suppressing the luminance when the high the input video signal level is high.

Display luminance level is controlled by 256-step and it follows the variance of the input video signal level quickly. This operation realizes a smooth transition characteristic on display luminance level.

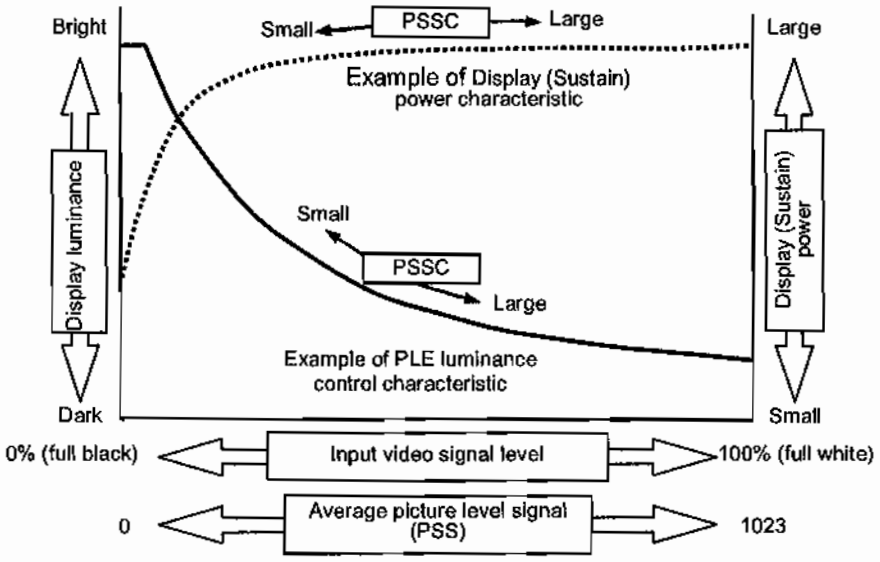

Figure 13. Example of PLE characteristic

Following figure shows the transfer characteristics of "Input video signal", "Average picture level signal", "Luminance level control signal", "Display luminance" and "Display (Sustain) power" in case input video signal is increased/decreased gradually between "Full-screen black" and "Full-screen white" and increased/ decreased quickly between "Full-screen black" and "Full-screen white".

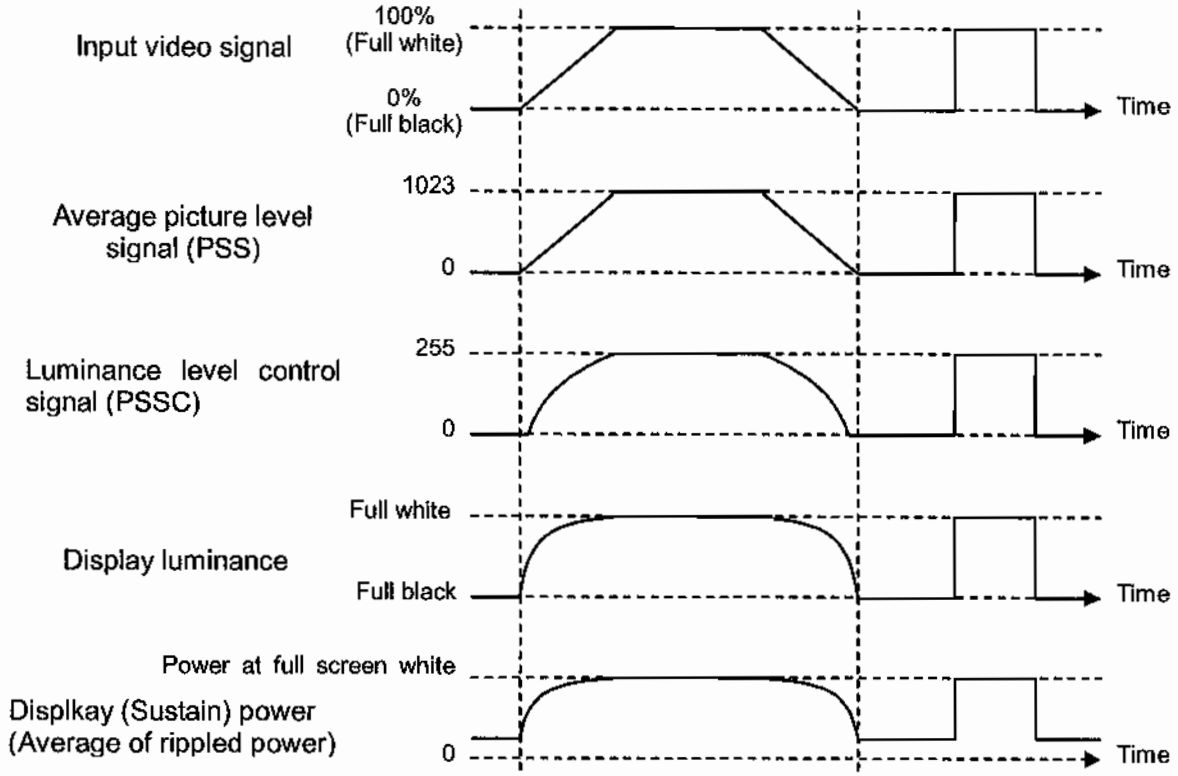

Figure 14. Example of PLE transfer characteristics

11.1. Set-up timing of External-PLE.

As shown in the figure 14, set-up of External-PLE should be completed within 700µs.

If do not be completed within 700µs, PLE control can be delayed by 1 video frame to the input video signal. In this condition, when the image is changed from a low average picture level frame to a high average picture level frame, power consumption (display discharge current) may increases temporally, because high load display status (e.g.: full-screen white→ large PSSC value) is driven with a condition of low load display status (e.g.: less than 4% of white window→small PSSC value).
In this case, in order avoid the circuits breakdown, quick increase of temperature and/or increase of power consumption, this module suppress the consuming power by the limiter circuit.

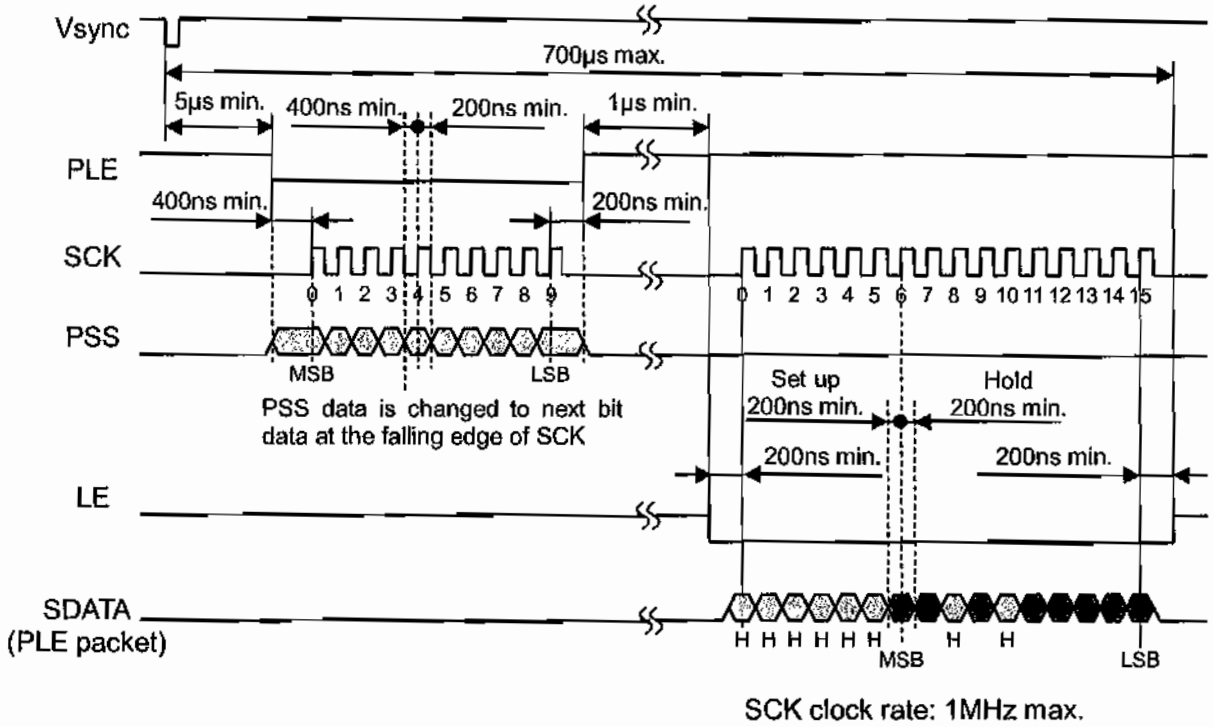

Figure 15. External-PLE control timing

11.2. External-PLE luminance level control data input function.

When use the External-PLE function, PSSC (PLE luminance level control signal) is inputted through the PLE dynamic packet.

(1) Contents of PLE dynamic packet data

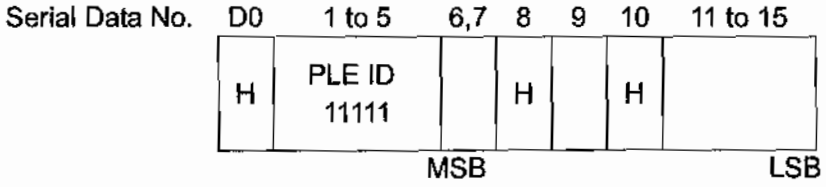

Table 17. Contents of PLE dynamic packet data		
Serial Data No.	Data name	Setup value
D0	Identify	1
D1 to D5	PLE ID	11111
D6, D7	PLE / PSSC 7, PSSC6	PLE control data bit#7, bit#6
D8	Identify	1
D9	PLE / PSSC 5	PLE control data bit#5
D10	Identify	1
D11 to D15	PLE / PSSC 4 to 0	PLE control data bit#4 to bit#0

Note: PSSC7 is MSB (most significant bit), PSSC0 is LSB (least significant bit)

12. COLOR SPACE CONVERSION FUNCTION

This PDP module incorporates the color space conversion function that converts Y, Cb, Cr input color differential video signal to RGB video signal.

(1) Set-up of Color space conversion function

This function can be enabled by setting the status of bit number D50 (COLOR SPACE) in the display mode packet data to "H" (ON), and bypassed by setting it to "L" (OFF) (refer to table 12).

(2) Set-up of the input video signal bit-width

Bit-width of the input video signal (8, 9 or 10-bit) can be selected by D48 and D49 in the display mode packet data (default is 8-bit) (refer to table 10)

(3) Set-up of the parameters for color space conversion

The parameters can be set through the color space conversion packet data.

The coefficients Cs1 to Cs5 (13-bit each) are defined to the input setting data C_cs_1 to C_cs_5 (13-bit each) as follows.

Most significant bit (MSB) of the setting data is the sign-bit that shows minus. This value is expressed as "2's complement" of the setting data.

C_cs_1 / 1024 = Cs1
C_cs_2 / 1024 = Cs2
C_cs_3 / 1024 = Cs3
C_cs_4 / 1024 = Cs4
C_cs_5 / 1024 = Cs5

Relation between input Y、Cb、Cr color differential video signal and output RGB video signal is as follows.

R = Cs1(Y – Yc) + Cs4(Cr – Cc)
G = Cs1(Y – Yc) + Cs2(Cr – Cc) + Cs3(Cb – Cc)
B = Cs1(Y – Yc) + Cs5(Cb – Cc)

Yc, Cc are the constant value defined as follows.

Bit No. of input video signal	8-bit	9-bit	10-bit
Yc	16	32	64
Cc	128	256	512

(4) Input terminal of Y、Cb、Cr color differential signal

Y signal input			Cb signal input			Cr signal input			Assign of input signal		
Signal		Input terminal	Signal		Input terminal	Signal		Input terminal	8-bit	9-bit	10-bit
Y7	→	G7	Cb7	→	B7	Cr7	→	R7	MSB	MSB	MSB
Y0	→	G0	Cb0	→	B0	Cr0	→	R0	LSB		
y1	→	g1	cb1	→	b1	cr1	→	r1	Ignored	LSB	
y0	→	g0	cb0	→	b0	cr0	→	r0	Ignored	Ignored	LSB

y1, cb1, cr1 are the LSB bit of 9-bit signal or 2nd bit from lowest signal of 10-bit color differential signal.

y0, cb0, cr0 are the LSB bit of 10-bit color differential signal.

Default setting value

Followings are se-up as the default setting values.

Table 18 Color space conversion default setting value

Data name	Default data	Default setting value	(Reference) Standard value
C_cs_1 [12:0]	13d' 1191	Cs1 = C_cs_1 / 1024 =1191 / 1024 = 1.163	1.164
C_cs_2 [12:0]	13d' –830	Cs2 = C_cs_2 / 1024 = –830 / 1024 =–0.811	–0.813
C_cs_3 [12:0]	13d' –402	Cs3 = C_cs_3 / 1024 =–402 / 1024 = –0.393	–0.392
C_cs_4 [12:0]	13d' 1631	Cs4 = C_cs_4 / 1024 =1631 / 1024 = 1.593	1.596
C_cs_5 [12:0]	13d' 2071	Cs5 = C_cs_5 / 1024 = 2071 / 1024 = 2.022	2.017

(5) Contents of dynamic packet data

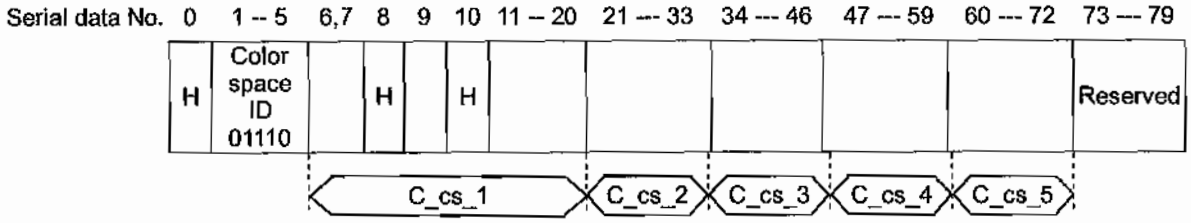

Table 19 Contents of color space conversion data

Serial Data No.	Data name	Set up value
D0	Identify	1
D1~D5	Color space ID	01110
D6, 7	C_cs_1_12, C_cs_1_11	Data for coefficient Cs1 bit# 12 and 11
D8	Identify	1
D9	C_cs_1_10	Data for coefficient Cs1 bit# 10
D10	Identify	1
D11~D20	C_cs_1_9~C_cs_1_0	Data for coefficient Cs1 bit# 9 to 0
D21~D33	C_cs_2_12~C_cs_2_0	Data for coefficient Cs2 bit# 12 to 0
D34~D46	C_cs_3_12~C_cs_3_0	Data for coefficient Cs3 bit# 12 to 0
D47~D59	C_cs_4_12~C_cs_4_0	Data for coefficient Cs4 bit# 12 to 0
D60~D72	C_cs_5_12~C_cs_5_0	Data for coefficient Cs5 bit# 12 to 0
D73~D79	Reserve	000 0000

13. INVERSE GAMMA CORRECTING FUNCTION

This PDP module incorporates the inverse gamma correcting function that can be set by each of R, G, and B color signal.

Inverse gamma characteristic is separated in 3 input signal gray-scale areas that are separated by 2-border values r1 and r2 (refer to figure 15). The characteristic can be set using parameters that determine the coefficients "a" to "f", "h" of gamma characteristic functions by each color respectively. These parameters can be set through a gamma dynamic-packet.

(1) Set-up of the inverse gamma function

This function can be enabled by setting the status of bit number D51 in the display mode packet data to "high", and bypassed by setting it to "Low" (refer to Table 12).

(2) Set-up of the input video signal bit-width

Bit-width of the input video signal (8, 9, or 10bit) can be selected by the bit-numbers D48 and D49 of the display mode packet data (default is 8 bits) (refer to Table 12).

(3) Set-up of the parameters for inverse gamma characteristics

The parameters can be set through the inverse gamma dynamic packet data.

The coefficients (a to f and h) are the binary numbers with sign digits (to designate the algebraic sign + or -) that can be set with 10, 12, 14 or16-bit accuracy for conversion (default is 16-bit).

Though the bit accuracy can be selected depend on the processing ability of the connected control circuits, in order to keep accurate inverse gamma characteristics, it is recommends to use l6-bit accuracy as much as possible.

Most significant bit (MSB) of the parameters corresponded to "a" to "f", "h" is the sign bits with "2's complement" expression.

(Example) 65534 in decimal is expressed as 1111_1111_1111_1110 in binary.
The complement of this number is 0000_0000_0000_0010 in binary.
Thus, this number means –2 in decimal.

Parameters for border-values r1 and r2 are the 10 bit-binary numbers without sign bit.

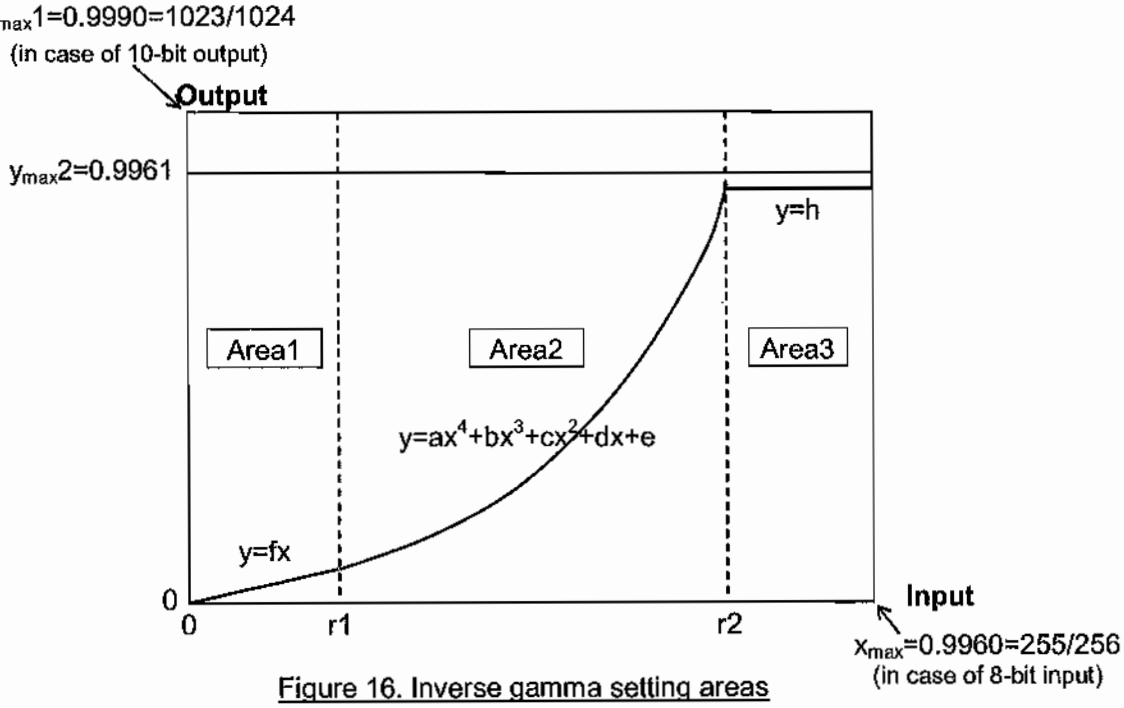

Figure 16. Inverse gamma setting areas

x and y are determined to the input video signal X and the output signal Y respectively as follows.

$x=X/(X_{max}+1)$

$y=Y/(Y_{max}+1)$

(Example)

When the input signal is 8-bit, maximum input value x_{max} is 255/256 = 0.9960.

When the output signal is 10 bits, maximum output value $y_{max}1$ is 1023/1024 = 0.9990

Coefficients "a" to "f", "h" and border-values "r1", "r2" are determined as follows correspond to the input data in the dynamic packet (refer to Table 20 to Table 23).

a = C_ga_a_R / Normalization constant
b = C_ga_b_R / Normalization constant
:
f = C_ga_f_R / Normalization constant
h = C_ga_h_R / Normalization constant
r1 = C_ga_x1_R / 1024
r2 = C_ga_x2_R / 1024

Normalization constant in 16-bit accuracy: 8192
in 14-bit accuracy: 2048
in 12-bit accuracy: 512
in 10-bit accuracy: 128

Mathematical formula of Inverse gamma curve and border of the Areas are defined as follows.

Area1: $y=fx$ (settable range: $0 \le f \le 3.9999$)
Area2: $y=ax^4+bx^3+cx^2+dx+e$
Area3: $y=h$ (settable range: $0 \le h < 1$)
Range of Area1: $0 \le$ Area1 $\le r1$,
Range of Area2: $r1 <$ Area2 $\le r2$
Range of Area3: $r2 <$ Area3 < 1

Note 1: If the both value of r1, r2 are same, area 2 is eliminated.
Note 2: Values specify these parameters have limitations, because of incorporated calculator's ability.

(4) Bit-width of output signal

Bit-width of the output signal becomes 2-bit larger than the bit-width of the selected display mode (8 or 9-bit) in "Table 13 Display picture mode set-up table".
(For relation with display image, refer to Table 15)

(5) Default setting value

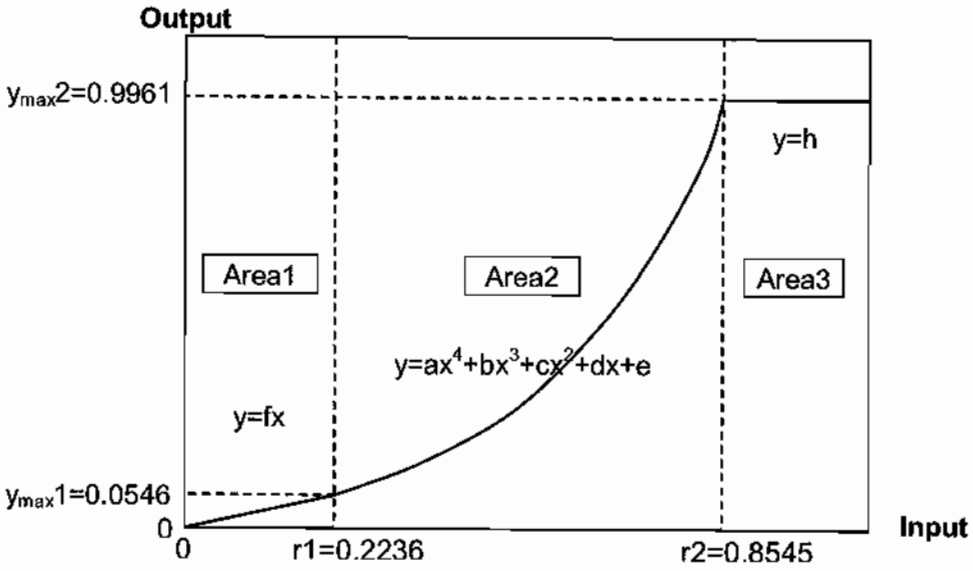

Figure 17. Inverse gamma conversion default characteristics

a = C_ga_a_R / 8192 = -1717 / 8192 = - 0.2096
b = C_ga_b_R / 8192 = 5228 / 8192 = 0.6382
c = C_ga_c_R / 8192 = 8079 / 8192 = 0.9862
d = C_ga_d_R / 8192 = -85 / 8192 = - 0.0104
e = C_ga_e_R / 8192 = -12 / 8192 = - 0.0015
f = C_ga_f_R / 8192 = 1914 / 8192 = 0.2336
h = C_ga_h_R / 8192 = 8160 / 8192 = 0.9961
r1 = C_ga_x1_R / 1024 = 229 / 1024 = 0.2236
r2 = C_ga_x2_R / 1024 = 875 / 1024 = 0.8545

$y1 = f \times r1 = 0.2336 \times 0.2336 = 0.0546$
$y2 = a \times r2^4 + b \times r2^3 + c \times r2^2 + d \times r2 + e = h = 0.9961$

Table 20. Inverse gamma characteristic default value (Red) note

Data name	Contents	Default value
C_ga_a_R[15:0]	Inverse gamma coefficient "a"	16'd -1717
C_ga_b_R[15:0]	Inverse gamma coefficient "b"	16'd 5228
C_ga_c_R[15:0]	Inverse gamma coefficient "c"	16'd 8079
C_ga_d_R[15:0]	Inverse gamma coefficient "d"	16'd -85
C_ga_e_R[15:0]	Inverse gamma coefficient "e"	16'd -12
C_ga_f_R[15:0]	Inverse gamma coefficient "f"	16'd 1914
C_ga_h_R[15:0]	Inverse gamma coefficient "h"	16'd 8160
C_ga_x1_R[9:0]	Border value "r1"	10'd 229
C_ga_x2_R[9:0]	Border value "r2"	10'd 875

Note: Green and Blue have same default coefficients

(6) Contents of dynamic packet data

(a) 16-bit accuracy inverse gamma conversion

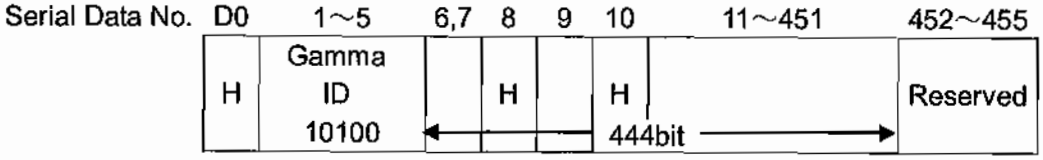

Table 21. Contents of 16-bit accuracy inverse gamma conversion data

Serial Data No.	Data Name	Set up value
D0	Identify	1
D1 to D5	Gamma_ID	10100
D6, D7	C_ga_a_R15,R14	Coefficient a for bit#15 and 14
D8	Identify	1
D9	C_ga_a_R13	Coefficient a for bit#13
D10	Identify	1
D11 to D23	C_ga_a_R12 to R0	Coefficient a for red bit# from 12 to 0
D24 to D39	C_ga_b_R15 to R0	Coefficient b for red bit# from 15 to 0
D40 to D55	C_ga_c_R15 to R0	Coefficient c for red bit# from 15 to 0
D56 to D71	C_ga_d_R15 to R0	Coefficient d for red bit# from 15 to 0
D72 to D87	C_ga_e_R15 to R0	Coefficient e for red bit# from 15 to 0
D88 to D103	C_ga_f_R15 to R0	Coefficient f for red bit# from 15 to 0
D104 to D119	Reserve	0000 0000 0000 0000
D120 to D135	C_ga_h_R15 to R0	Coefficient h for red bit# from 15 to 0
D136 to D151	C_ga_a_G15 to G0	Coefficient a for green bit# from 15 to 0
D152 to D167	C_ga_b_G15 to G0	Coefficient b for green bit# from 15 to 0
D168 to D183	C_ga_c_G15 to G0	Coefficient c for green bit# from 15 to 0
D184 to D199	C_ga_d_G15 to G0	Coefficient d for green bit# from 15 to 0
D200 to D215	C_ga_e_G15 to G0	Coefficient e for green bit# from 15 to 0
D216 to D231	C_ga_f_G15 to G0	Coefficient f for green bit# from 15 to 0
D232 to D247	Reserve	0000 0000 0000 0000
D248 to D263	C_ga_h_G15 to G0	Coefficient h for green bit# from 15 to 0
D264 to D279	C_ga_a_B15 to B0	Coefficient a for blue bit# from 15 to 0
D280 to D295	C_ga_b_B15 to B0	Coefficient b for blue bit# from 15 to 0
D296 to D311	C_ga_c_B15 to B0	Coefficient c for blue bit# from 15 to 0
D312 to D327	C_ga_d_B15 to B0	Coefficient d for blue bit# from 15 to 0
D328 to D343	C_ga_e_B15 to B0	Coefficient e for blue bit# from 15 to 0
D344 to D359	C_ga_f_B15 to B0	Coefficient f for blue bit# from 15 to 0
D360 to D375	Reserve	0000 0000 0000 0000
D376 to D391	C_ga_h_B15 to B0	Coefficient h for blue bit# from 15 to 0
D392 to D401	C_ga_x1_R9 to R0	Border r1 for red bit# from 9 to 0
D402 to D411	C_ga_x2_R9 to R0	Border r2 for red bit# from 9 to 0
D412 to D421	C_ga_x1_G9 to G0	Border r1 for green bit# from 9 to 0
D422 to D431	C_ga_x2_G9 to G0	Border r2 for green bit# from 9 to 0
D432 to D441	C_ga_x1_B9 to B0	Border r1 for blue bit# from 9 to 0
D442 to D451	C_ga_x2_B9 to B0	Border r2 for blue bit# from 9 to 0
D452 to D455	Reserve	0000

(b) 14-bit accuracy inverse gamma conversion

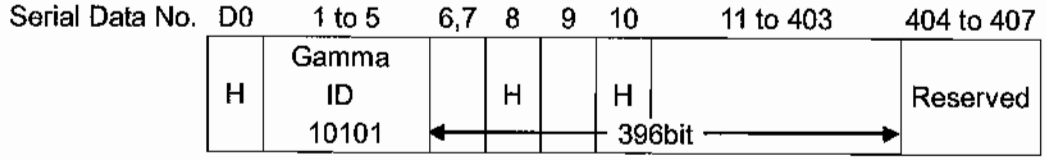

Table 22. Contents of 14-bit accuracy inverse gamma conversion data		
Serial Data No.	Data name	Setup value
D0	Identify	1
D1 to D5	Gamma_ID	10101
D6, D7	C_ga_a_R13, R12	Coefficient a for red bit#13 and 12
D8	Identify	1
D9	C_ga_a_R11	Coefficient a for red bit#11
D10	Identify	1
D11 to D21	C_ga_a_R10 to R0	Coefficient a for red bit# from 10 to 0
D22 to D35	C_ga_b_R13 to R0	Coefficient b for red bit# from 13 to 0
D36 to D49	C_ga_c_R13 to R0	Coefficient c for red bit# from 13 to 0
D50 to D63	C_ga_d_R13 to R0	Coefficient d for red bit# from 13 to 0
D64 to D77	C_ga_e_R13 to R0	Coefficient e for red bit# from 13 to 0
D78 to D91	C_ga_f_R13 to R0	Coefficient f for red bit# from 13 to 0
D92 to D105	Reserve	00 0000 0000 0000
D106 to D119	C_ga_h_R13 to R0	Coefficient h for red bit# from 13 to 0
D120 to D133	C_ga_a_G13 to G0	Coefficient a for green bit# from 13 to 0
D134 to D147	C_ga_b_G13 to G0	Coefficient b for green bit# from 13 to 0
D148 to D161	C_ga_c_G13 to G0	Coefficient c for green bit# from 13 to 0
D162 to D175	C_ga_d_G13] to G0	Coefficient d for green bit# from 13 to 0
D176 to D189	C_ga_e_G13 to G0	Coefficient e for green bit# from 13 to 0
D190 to D203	C_ga_f_G13 to G0	Coefficient f for green bit# from 13 to 0
D204 to D217	Reserve	00 0000 0000 0000
D218 to D231	C_ga_h_G13 to G0	Coefficient h for green bit# from 13 to 0
D232 to D245	C_ga_a_B13 to B0	Coefficient a for blue bit# from 13 to 0
D246 to D259	C_ga_b_B13 to B0	Coefficient b for blue bit# from 13 to 0
D260 to D273	C_ga_c_B13 to B0	Coefficient c for blue bit# from 13 to 0
D274 to D287	C_ga_d_B13 to B0	Coefficient d for blue bit# from 13 to 0
D288 to D301	C_ga_e_B13 to B0	Coefficient e for blue bit# from 13 to 0
D302 to D315	C_ga_f_B13 to B0	Coefficient f for blue bit# from 13 to 0
D316 to D329	Reserve	00 0000 0000 0000
D330 to D343	C_ga_h_B13 to B0	Coefficient h for blue bit# from 13 to 0
D344 to D353	C_ga_x1_R9 to R0	Border r1 for red bit# from 9 to 0
D354 to D363	C_ga_x2_R9 to R0	Border r2 for red bit# from 9 to 0
D364 to D373	C_ga_x1_G9 to G0	Border r1 for green bit# from 9 to 0
D374 to D383	C_ga_x2_G9 to G0	Border r2 for green bit# from 9 to 0
D384 to D393	C_ga_x1_B9 to B0	Border r1 for blue bit# from 9 to 0
D394 to D403	C_ga_x2_B9 to B0	Border r2 for blue bit# from 9 to 0
D404 to D407	Reserve	0000

(c) 12-bit accuracy inverse gamma conversion

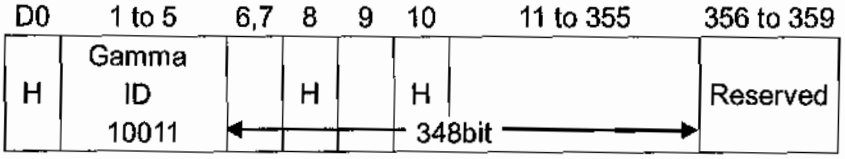

Table 23. Contents of 12-bit accuracy inverse gamma conversion data

Serial Data No.	Data name	Setup value
D0	Identify	1
D1 to D5	Gamma_ID	10011
D6, D7	C_ga_a_R11, R10	Coefficient a for red bit# 11 and 10
D8	Identify	1
D9	C_ga_a_R9	Coefficient a for red bit# 9
D10	Identify	1
D11 to D19	C_ga_a_R8 to R0	Coefficient a for red bit# from 8 to 0
D20 to D31	C_ga_b_R11 to R0	Coefficient b for red bit# from 11 to 0
D32 to D43	C_ga_c_R11 to R0	Coefficient c for red bit# from 11 to 0
D44 to D55	C_ga_d_R11 to R0	Coefficient d for red bit# from 11 to 0
D56 to D67	C_ga_e_R11 to R0	Coefficient e for red bit# from 11 to 0
D68 to D79	C_ga_f_R11 to R0	Coefficient f for red bit# from 11 to 0
D80 to D91	Reserve	0000 0000 0000
D92 to D103	C_ga_h_R11 to R0	Coefficient h for red bit# from 11 to 0
D104 to D115	C_ga_a_G11 to G0	Coefficient a for green bit# from 11 to 0
D116 to D127	C_ga_b_G11 to G0	Coefficient b for green bit# from 11 to 0
D128 to D139	C_ga_c_G11 to G0	Coefficient c for green bit# from 11 to 0
D140 to D151	C_ga_d_G11 to G0	Coefficient d for green bit# from 11 to 0
D152 to D163	C_ga_e_G11 to G0	Coefficient e for green bit# from 11 to 0
D164 to D175	C_ga_f_G11 to G0	Coefficient f for green bit# from 11 to 0
D176 to D187	Reserve	0000 0000 0000
D188 to D199	C_ga_h_G11 to G0	Coefficient h for green bit# from 11 to 0
D200 to D211	C_ga_a_B11 to B0	Coefficient a for blue bit# from 11 to 0
D212 to D223	C_ga_b_B11 to B0	Coefficient b for blue bit# from 11 to 0
D224 to D235	C_ga_c_B11 to B0	Coefficient c for blue bit# from 11 to 0
D236 to D247	C_ga_d_B11 to B0	Coefficient d for blue bit# from 11 to 0
D248 to D259	C_ga_e_B11 to B0	Coefficient e for blue bit# from 11 to 0
D260 to D271	C_ga_f_B11 to B0	Coefficient f for blue bit# from 11 to 0
D272 to D283	Reserve	0000 0000 0000
D284 to D295	C_ga_h_B11 to B0	Coefficient h for blue bit# from 11 to 0
D296 to D305	C_ga_x1_R9 to R0	Borderline r1 for red bit# from 9 to 0
D306 to D315	C_ga_x2_R9 to R0	Borderline r2 for red bit# from 9 to 0
D316 to D325	C_ga_x1_G9 to G0	Borderline r1 for green bit# from 9 to 0
D326 to D335	C_ga_x2_G9 to G0	Borderline r2 for green bit# from 9 to 0
D336 to D345	C_ga_x1_B9 to B0	Borderline r1 for blue bit# from 9 to 0
D346 to D355	C_ga_x2_B9 to B0	Borderline r2 for blue bit# from 9 to 0
D356 to D359	Reserve	0000

(d) 10-bit accuracy inverse gamma conversion

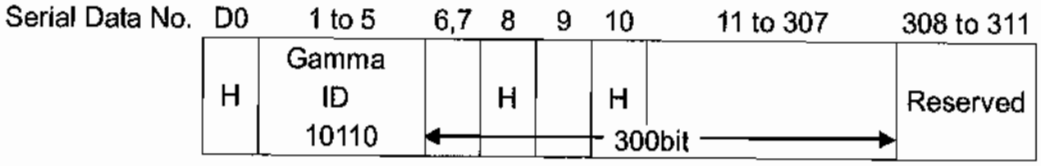

Table 24. Contents of 10-bit accuracy inverse gamma conversion data		
Serial Data No.	Data name	Setup value
D0	Identify	1
D1 to D5	Gamma ID	10110
D6, D7	C_ga_a_R9, R8	Coefficient a for red bit# from 9 and 8
D8	Identify	1
D9	C_ga_a_R7	Coefficient a for red bit# 7
D10	Identify	1
D11 to D17	C_ga_a_R6 to R0	Coefficient a for red bit# from 6 to 0
D18 to D27	C_ga_b_R9 to R0	Coefficient b for red bit# from 9 to 0
D28 to D37	C_ga_c_R9 to R0	Coefficient c for red bit# from 9 to 0
D38 to D47	C_ga_d_R9 to R0	Coefficient d for red bit# from 9 to 0
D48 to D57	C_ga_e_R9 to R0	Coefficient e for red bit# from 9 to 0
D58 to D67	C_ga_f_R9 to R0	Coefficient f for red bit# from 9 to 0
D68 to D77	Reserve	00 0000 0000
D78 to D87	C_ga_h_R9 to R0	Coefficient h for red bit# from 9 to 0
D88 to D97	C_ga_a_G9 to G0	Coefficient a for green bit# from 9 to 0
D98 to D107	C_ga_b_G9 to G0	Coefficient b for green bit# from 9 to 0
D108 to D117	C_ga_c_G9 to G0	Coefficient c for green bit# from 9 to 0
D118 to D127	C_ga_d_G9 to G0	Coefficient d for green bit# from 9 to 0
D128 to D137	C_ga_e_G9 to G0	Coefficient e for green bit# from 9 to 0
D138 to D147	C_ga_f_G9 to G0	Coefficient f for green bit# from 9 to 0
D148 to D157	Reserve	00 0000 0000
D158 to D167	C_ga_h_G9 to G0	Coefficient h for green bit# from 9 to 0
D168 to D177	C_ga_a_B9 to B0	Coefficient a for blue bit# from 9 to 0
D178 to D187	C_ga_b_B9 to B0	Coefficient b for blue bit# from 9 to 0
D188 to D197	C_ga_c_B9 to B0	Coefficient c for blue bit# from 9 to 0
D198 to D207	C_ga_d_B9 to B0	Coefficient d for blue bit# from 9 to 0
D208 to D217	C_ga_e_B9 to B0	Coefficient e for blue bit# from 9 to 0
D218 to D227	C_ga_f_B9 to B0	Coefficient f for blue bit# from 9 to 0
D228 to D237	Reserve	00 0000 0000
D238 to D247	C_ga_h_B9 to B0	Coefficient h for blue bit# from 9 to 0
D248 to D257	C_ga_x1_R9 to R0	Borderline r1 for red bit# from 9 to 0
D258 to D267	C_ga_x2_R9 to R0	Borderline r2 for red bit# from 9 to 0
D268 to D277	C_ga_x1_G9 to G0	Borderline r1 for green bit# from 9 to 0
D278 to D287	C_ga_x2_G9 to G0	Borderline r2 for green bit# from 9 to 0
D288 to D297	C_ga_x1_B9 to B0	Borderline r1 for blue bit# from 9 to 0
D298 to D307	C_ga_x2_B9 to B0	Borderline r2 for blue bit# from 9 to 0
D308 to D311	Reserve	0000

14. ERROR DIFFUSION FUNCTION

This PDP module integrates error diffusion function. Diffuse factor can be set-up using 5-bit width parameter.

(1)Set-up of the error diffusion function

This function can be enabled by setting the bit number D52 (ED) in the display mode packet data to "H"(ON). When set to "L"(OFF), this function does not operate.

(2)Set-up of the input video signal bit-width

Bit-width of the input video signal (8, 9, or 10bit) can be selected by the bit-numbers D48 and D49 of the display mode packet data (default is 8 bits) (refer to Table 12).

(3)Output of error diffusion function

When use the incorporated inverse gamma function together, lower 2-bit of output video signal from the inverse gamma function is used for error diffusion data.

When use the error diffusion function alone, lower 2-bit of the input video signal is used for error diffusion data. (For relation with display image, refer to Table 15)

(4)Set-up of error diffusion coefficient

Set the error diffusion parameters for adjacent 4 pixels with 5-bit binary data through the error diffusion dynamic packet.

Error diffusion coefficients are defined as one sixteenth (1/16) of the error diffusion parameters.

(5)Default setting value

erd_1=C_erd_1/16=7/16
erd_2=C_erd_2/16=3/16
erd_3=C_erd_3/16=5/16
erd_4=C_erd_4/16=1/16

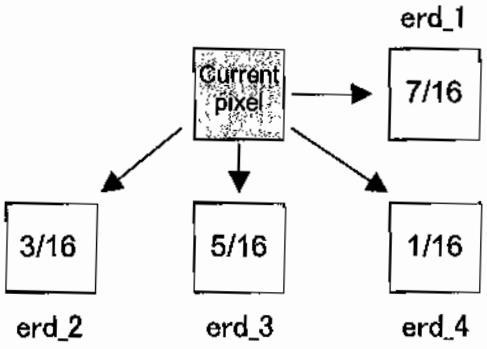

Figure 18. Default setting data of error diffusion

Table25. Default setting value of error diffusion

Data name	Contents	Default value
C_erd_1[4:0]	Error diffusion coefficient (numerator)	5'd 7
C_erd_2[4:0]	Error diffusion coefficient (numerator)	5'd 3
C_erd_3[4:0]	Error diffusion coefficient (numerator)	5'd 5
C_erd_4[4:0]	Error diffusion coefficient (numerator)	5'd 1

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(6)Data contents of dynamic packet for error diffusion

Input the error diffusion parameters for adjacent 4 pixels with 5-bit binary data.

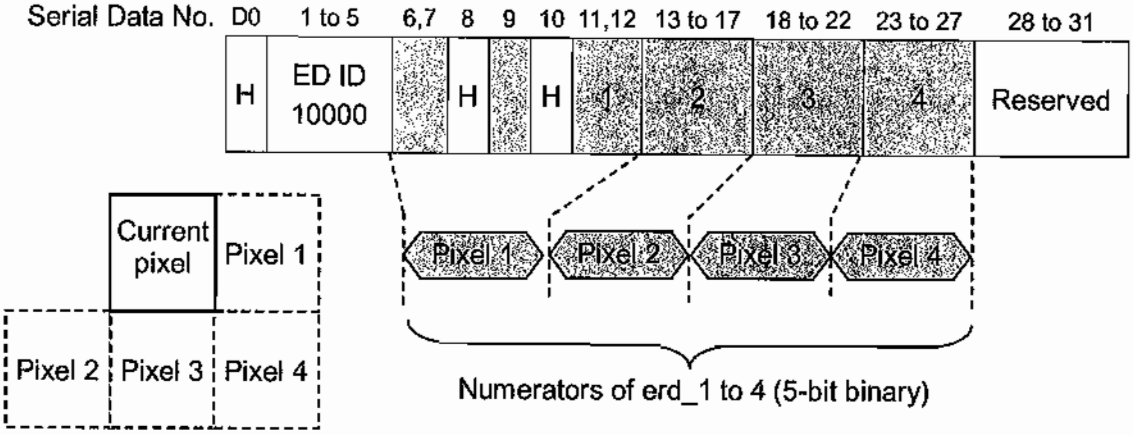


Table 26. Contents of error diffusion dynamic packet data		
Serial Data No.	Data Name	Setup value
D0	Identify	1
D1 to D5	Error Diffusion ID	10000
D6	C_erd_1_4	Diffusing coefficient for pixel 1, bit#4
D7	C_erd_1_3	Diffusing coefficient for pixel 1, bit#3
D8	Identify	1
D9	C_erd_1_2	Diffusing coefficient for pixel 1, bit#2
D10	Identify	1
D11	C_erd_1_1	Diffusing coefficient for pixel 1, bit#1
D12	C_erd_1_0	Diffusing coefficient for pixel 1, bit#0
D13	C_erd_2_4	Diffusing coefficient for pixel 2, bit#4
D14	C_erd_2_3	Diffusing coefficient for pixel 2, bit#3
D15	C_erd_2_2	Diffusing coefficient for pixel 2, bit#2
D16	C_erd_2_1	Diffusing coefficient for pixel 2, bit#1
D17	C_erd_2_0	Diffusing coefficient for pixel 2, bit#0
D18	C_erd_3_4	Diffusing coefficient for pixel 3, bit#4
D19	C_erd_3_3	Diffusing coefficient for pixel 3, bit#3
D20	C_erd_3_2	Diffusing coefficient for pixel 3, bit#2
D21	C_erd_3_1	Diffusing coefficient for pixel 3, bit#1
D22	C_erd_3_0	Diffusing coefficient for pixel 3, bit#0
D23	C_erd_4_4	Diffusing coefficient for pixel 4, bit#4
D24	C_erd_4_3	Diffusing coefficient for pixel 4, bit#3
D25	C_erd_4_2	Diffusing coefficient for pixel 4, bit#2
D26	C_erd_4_1	Diffusing coefficient for pixel 4, bit#1
D27	C_erd_4_0	Diffusing coefficient for pixel 4, bit#0
D28 to D31	Reserved	0000

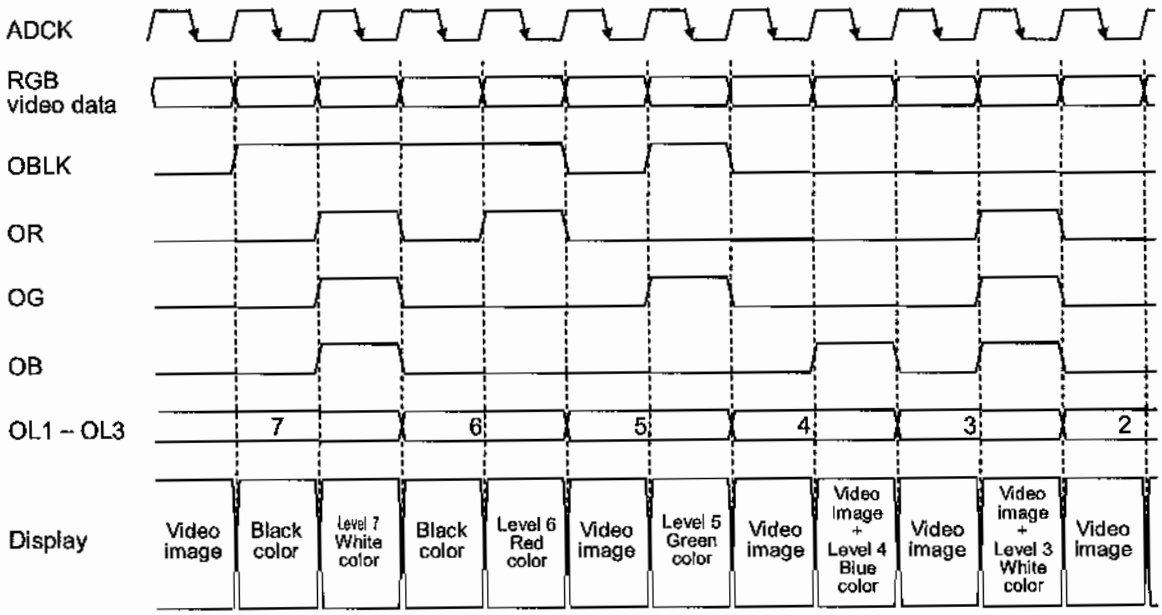
15. INPUT METHOD OF OSD SIGNALS

This module can display superposed OSD signal on the video signal by inputting the OSD signals from external OSD pattern generator synchronizing with the video signals.
Functions of OSD control signals are as follows.

Table 27. Functions of OSD control signals

Signal name	Function								
OBLK	Video mute signal. While OBLK is "H", video image of the corresponded pixel is changed to "black" color image.								
OR	While this signal is "H", red color is added on the "black" or the "video image" of corresponded pixel.								
OG	While this signal is "H", green color is added on the "black " or the "video image" of corresponded pixel.								
OB	While this signal is "H", blue color is added on the "black" or the "video image" of corresponded pixel.								
OL3 OL2 OL1	These signals determine the brightness of OSD pattern. Following 8-step brightness levels are adjustable.								
	OL3	L	L	L	L	H	H	H	H
	OL2	L	L	H	H	L	L	H	H
	OL1	L	H	L	H	L	H	L	H
	Level	0	1	2	3	4	5	6	7
	Brightness of OSD	0%	13%	25%	38%	50%	63%	75%	88%
Remarks	By the combination of OG, OR and OB signals, 7 colors are possible. For example, when OR, OG and OB are inputted simultaneously, white color pattern can be displayed.								

Following chart show the OSD signal input timing, and an example of the OSD input signals
When combined with the control of OBLK signal, OSD pattern can be displayed on the black display image, or OSD pattern can be displayed overlaid on the video image.



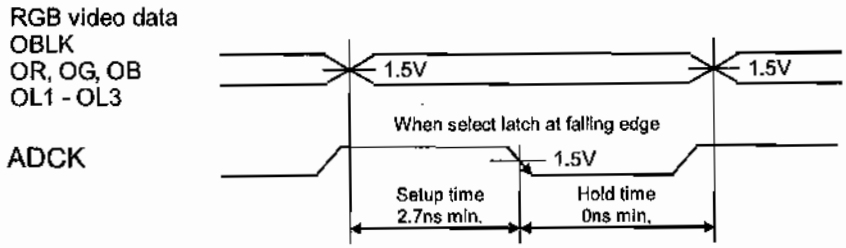


Figure 19. Example of OSD signals and their input timings

16. PROTECTION AGAINST EXCESSIVE LOAD COMES FROM UNUSUAL IMAGE DISPLAY.

Plasma display module has a characteristic when data write switching operation is repeated rapidly, the load of the driver circuits become large. For example, this high load status is appeared when the following pattern is displayed (Cell base checker pattern by on/off cells alternately by each cell).

In case this kind of image is displayed, this plasma display module gets into the protect-operation of driving circuits.

While the protect-operation, some display image may be deteriorated a little. However as soon as the display image returns to normal pattern, the protect-operation is released, and returns to the formal operation (At the protect-operation in 50Hz mode, display image may be observed like flickering.)

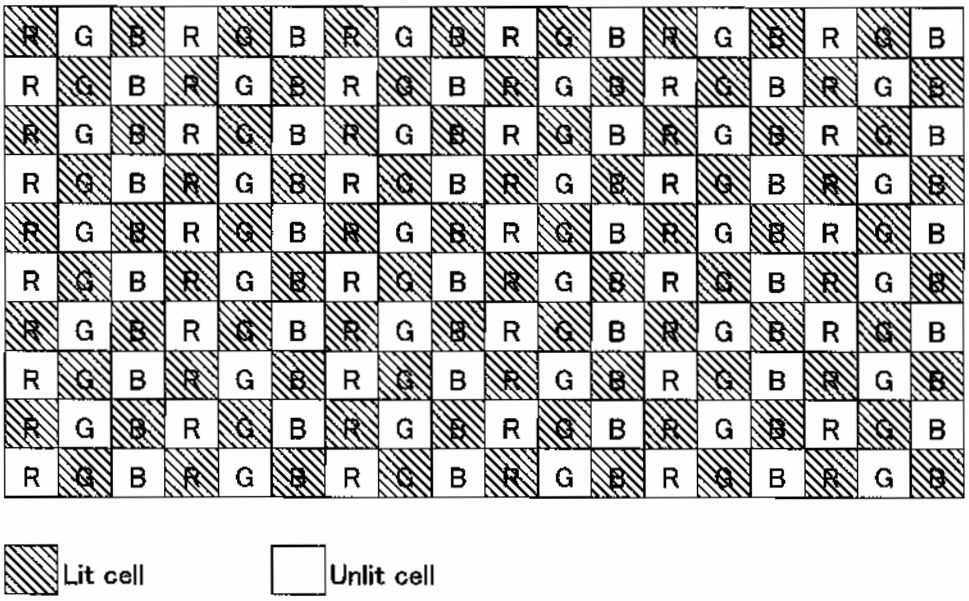


Figure 20. Example of display pattern that carries out protect-operation

When above pattern or other patterns that give equivalent on/off loads to the driver circuits are displayed in the concentrated area even if the size is about 10% of the total screen. The protect-operation can be carried out.

17. TYPE OF CONNECTORS AND PIN ASSIGNMENTS

For the connector positions, refer to the mechanical drawing (rear view)

17.1. Power input connectors

Table 28 Connector CN301 pin assignment (10-pin)			
Pin No.	Connection	Pin No.	Connection
1	LVP	2	GND
3	GND	4	GND
5	GND	6	Vd
7	Vd	8	NC
9	Vs	10	Vs

(NC): Non-connection pin (keep it open)

Module side connector: B10PS-VH
Mating connector: VHR-10N (housing),
SVH-21T-P1.1 (contact)
Connector supplier: J.S.T. TRADING COMPANY., LTD.
Fitting cable: Equivalent to AWG#20

Table 29 Connector CN302 pin assignment (4-pin)			
Pin No.	Connection	Pin No.	Connection
1	Vcc	2	Vcc
3	GND	4	GND

Module side connector: B4PS-VH
Mating connector: VHR-4N (housing),
SVH-21T-P1.1 (contact)
Connector supplier: J.S.T. TRADING COMPANY., LTD.
Fitting cable: Equivalent to AWG#20

Note: When use a long cable, applied voltage may be dropped because of its resistance.
Specified voltage should be applied correctly at the input of the module side connector.

17.2. Signal interface connector

Table 30. Connector CN101 pin assignment (31-pin)			
Pin No.	Signal name	Pin No.	Signal name
1	GND	2	GND
3	ALARM	4	GND
5	PS+	6	PS-
7	NC	8	GND
9	RH+	10	RH-
11	RG+	12	RG-
13	RF+	14	RF-
15	GND	16	RE+
17	RE-	18	RD+
19	RD-	20	RCLK+
21	RCLK-	22	GND
23	RC+	24	RC-
25	RB+	26	RB-
27	RA+	28	RA-
29	GND	30	GND
31	GND	---	---

(NC): Non-connection pin (keep it open)

Module side connector:	FI TWE31PB-VF
Mating connector:	FI-W31S (housing), FI-C3-A1-15000 (contact)
Connector supplier:	Japan Aviation Electronics Industry, Limited (JAE)
Fitting cable:	AWG#28 to 32 twist pair cable (It is recommended to shield whole cable assembly)

Note: Do not bundle the signal interface cable with the power cables. If do so, PDP module might have a malfunction due to the noise from the power cables.

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18. MECHANICAL SPECIFICATIONS

18.1. External dimensions 987(W)×584(H)×63.6(D)mm
(For details, refer to the mechanical drawing)

18.2. Weight 16kg typ.

19. ENVIRONMENTAL CONDITIONS AND RELIABILITY

19.1. Operating environmental conditions

(1) Temperature: 0 to 60°C
(2) Humidity: 20 to 80% RH (without condensation)
(3) Atmospheric pressure: 720 to 1114hPa

19.2. Storage environmental conditions

(1) Temperature: -20 to 60°C
(2) Humidity: 10 to 90% RH (without condensation)
(3) Atmospheric pressure: 700 to 1114hPa

19.3. Mechanical test conditions

(1) Vibration (Operating): 4.9m/s2 (0.5G), 10 to100Hz、3 directions, 10 minutes each
(2) Vibration (Non-operating) 4.9m/s2 (0.5G), 10 to100Hz、3 directions, 2 hours each
(3) Shock:
X、Y directions: 196m/s^2 (20G) peak, half sign wave form, 11ms, 3 times for each direction
Z direction: 98m/s^2 (10G) peak, half sign wave form, 11ms, 3 times for each direction

19.4. Life time expectancy

More than 10,000 hours of continuous operations in full-screen white display mode

Condition: Time when the luminance decreases to the half of initial luminance.
Full screen-display image (100% signal level)
Internal-PLE operation
Ambient temperature: 25°C

Caution: This is not a guarantee for each individual product.

19.5. Maximum temperature rating of electronic components in the module

The temperatures of each component mounted in the plasma display module must satisfy the following temperature specifications, with the condition when the plasma display module is mounted in the cabinet.

- Resistors (winding, metal oxide film, carbon film)	:	85°C max. (Soldering parts of lead-wires)
- Ceramic capacitors	:	85°C max. (Surface)
- Electrolytic capacitor (8mm or less in diameter)	:	80°C max. (Surface)
- Electrolytic capacitor (Over 8mm in diameter)	:	85°C max. (Surface)
- Digital LSI's	:	85°C max. (Surface)
- Display panel driver IC (Scan)	:	105°C max. (Surface)
- Display panel driver IC (Data)	:	100°C max. (Surface of heat sink)
- Power transistor, Diode	:	105°C max. (Surface)
- MOS FET power module (with aluminum heat sink)	:	105°C max. (Surface of heat sink)

19.6. Display panel temperature and stress specification

(1) Maximum temperature specification for display image performance

Following temperature at the display panel surface is specified in order to keep good display image performance.

¤ Tp=120°C max. (absolute maximum) : In case displays small area image
¤ Tp= 70°C max. : In case displays full-screen white image

When use the PDP module exceeding above temperatures, there is a possibility to have some missing display cells.
According to the decease of the "display image area ratio", the "panel surface temperature" has a tendency to increase. Relation between the "display image area ratio" and the "panel surface temperature" is as follows.

¤ 70°C (large display image area ratio) ←→ 120°C (small display image area ratio)

When display image area ratio is large, the temperature should be less than 70°C. Even if the display image area ratio is small, it is recommended to keep the temperature as low as possible.

(2) Panel stress specification

¤ Panel stress : 200 kg/cm^2 max.

< Reference> Rough estimation for temperature gradient of the panel

¤ Panel surrounding area :3 °C/cm or less
(less than 13mm from panel surrounding edge)
¤ Other area than panel surrounding :7 °C/cm or less
(over 13mm from panel surrounding edge)

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20. WARRANTY

All products are warranted to be free of defect for 2 years after EX-GO factory (Japan) in workmanship and materials that are proven to be defective within the warranty period.

Image sticking and defects such as blinking pixel caused by image sticking are excluded from the warranty objects. Any mishandling or incorrect operation of the product may void the warranty.

The obligation of Pioneer is limited to such repair or replacement, and does not extend to consequential damages. Equipment that has been repaired or replaced will be warranted only for remaining portion of the original warranty period.

21. SAFETY REGULATION

UL1492 Second Edition
UL 6500 Second Edition
UL 60950-1 First Edition
CSA C22.2 No.1-98
CSA E-60065-00
CSA C22.2 No. 60950-1-03
IEC/EN 60950 Third Edition
IEC/EN 60065 Sixth Edition

22. DELIBERATION

When other defects and/or problems that are not specified in this specification occur, they should be treated in accordance with mutual discussion and agreement between both parties.

23. MECHANICAL DRAWINGS

23.1. Front view (Unit:mm)

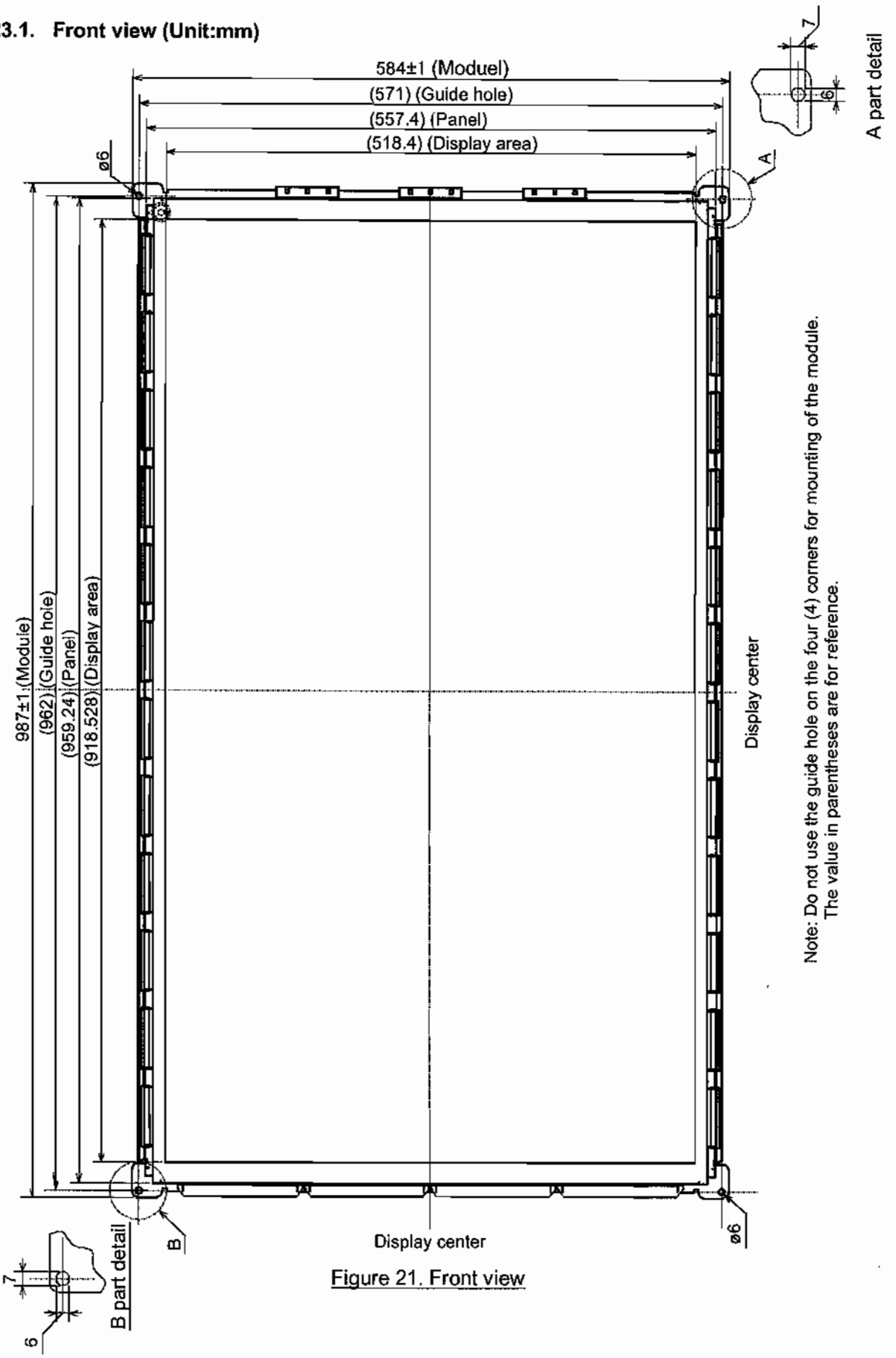

Figure 21. Front view

23.2. Rear view (Unit:mm)

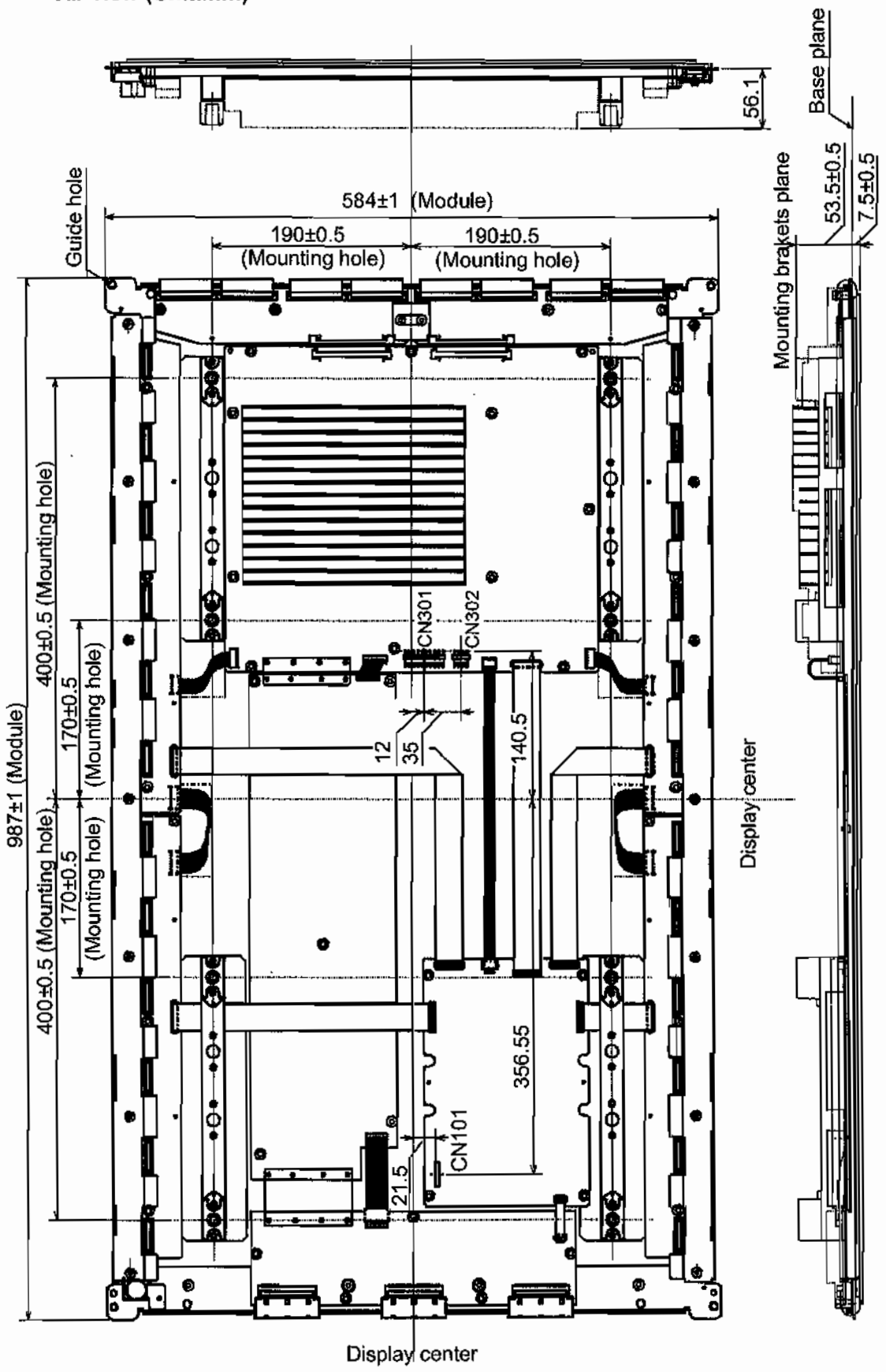

Figure 22. Rear view

23.3. Shape of mounting brackets

(Unit: mm)

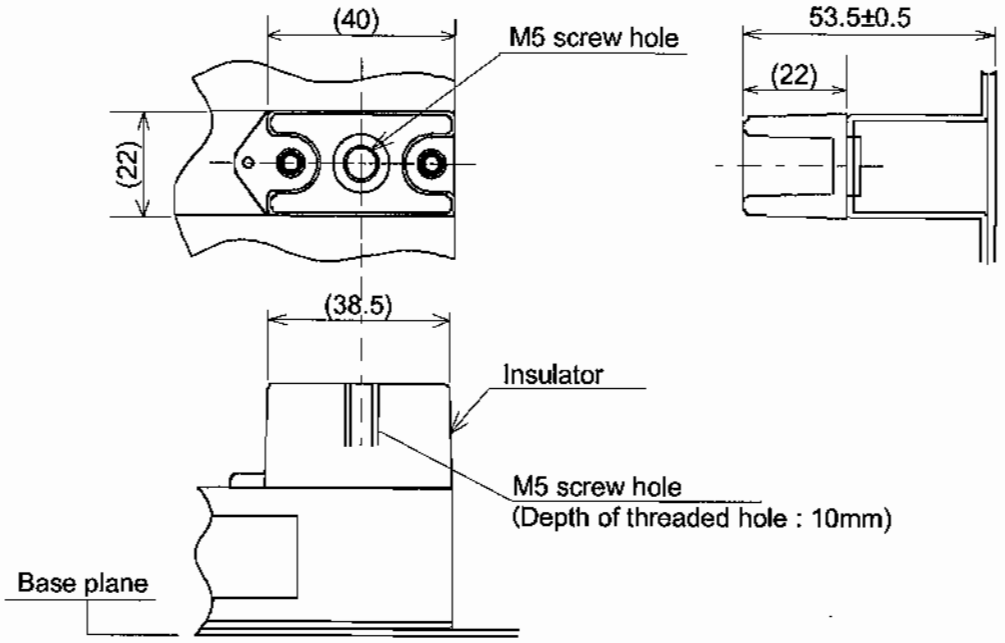

Figure 23. Shape of mounting brackets

23.4. Inhibited placing area of other parts or structures adjacent to the module

Rear view (Unit: mm)

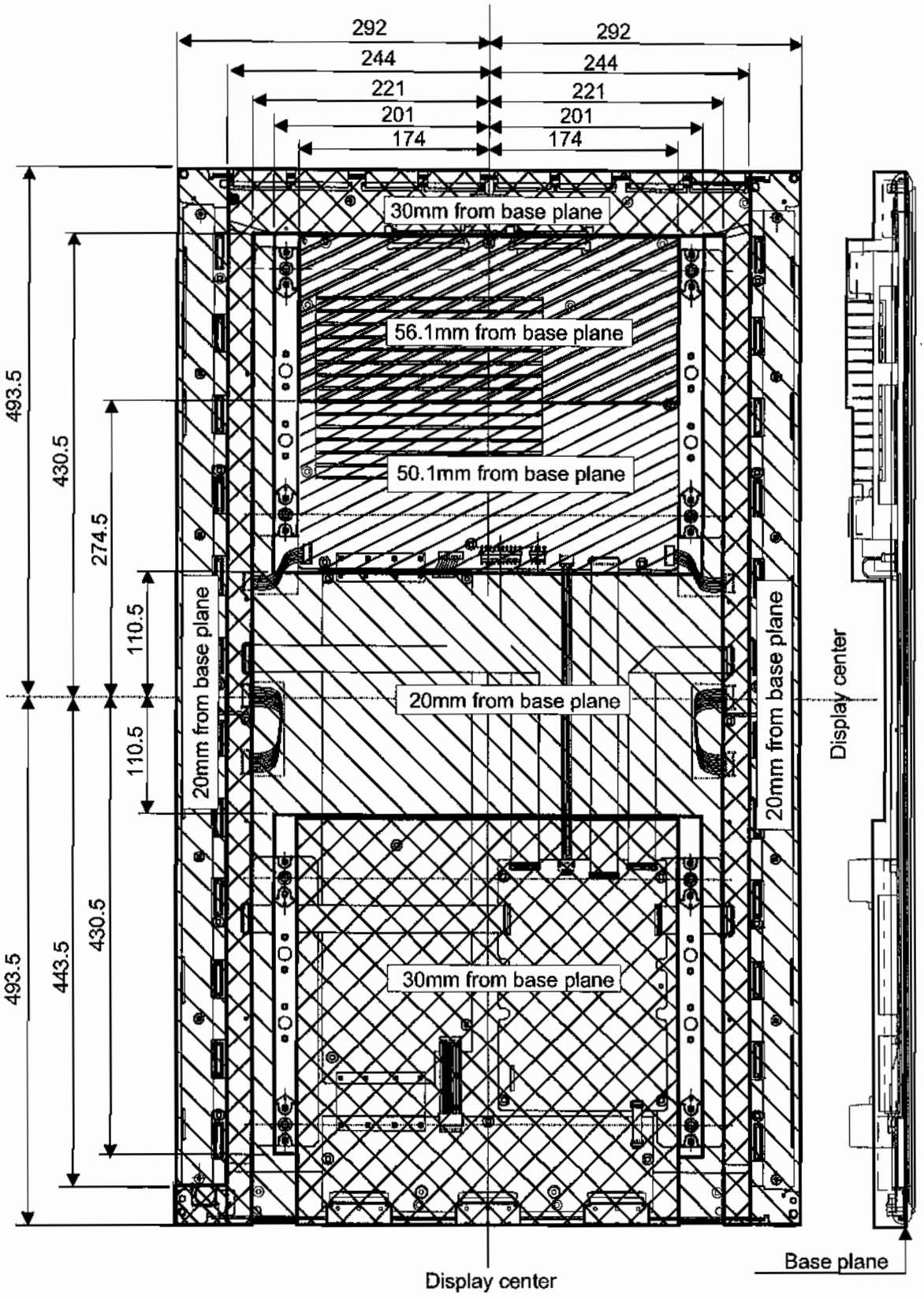

Figure 24. Inhibited placing area of other parts or structures adjacent to the module

24. PACKING AND TRANSPORTATION

Supplier will pack products to be delivered to customer in accordance with supplier's packing specifications, and will deliver them to customer in such a state that they will not suffer damage during transportation.

1) Shipping box

As shown in the following figure, shipping box is consisted of one box. Less than twelve modules are packed with inner boxes in one shipping box.

There is a risk of damage to the products if the shipping box is rolled, or dropped from a height of 30 cm or more. Therefore care should be taken in handling the box during the transportation and move the products.

During transportation, do not keep open this shipping box or remove shock-absorbing materials.

When the box is stored in a warehouse, etc., care should be taken to ensure that the storage conditions are within the specification.

2) Inner box.

This inner box is not designed for transportation use, therefore do not transport the products with this inner box alone.

This inner box does not have any shock absorbing materials, therefore never drop, roll, bump or shock while handling. If do so, products are easily broken.

When transport the products, additional shipping box and shock absorbing materials are required.

3) Means of transportation

Products are to be transported by hand, light van, truck, by air, or by sea.

4) Dimension and Weight

Table 31. Dimension and Weight (Rough approximation)

	External dimensions (mm)	Weight (include products)
PDP Module	987(L) x 63.6(W) x 585(H)	16 kg
Inner box	1112(L) x 77 (W) x 671 (H)	26 kg
Shipping box	1120(L) x 1080(W) x 850(H)	344 kg

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5) Packaging method (Inner box)

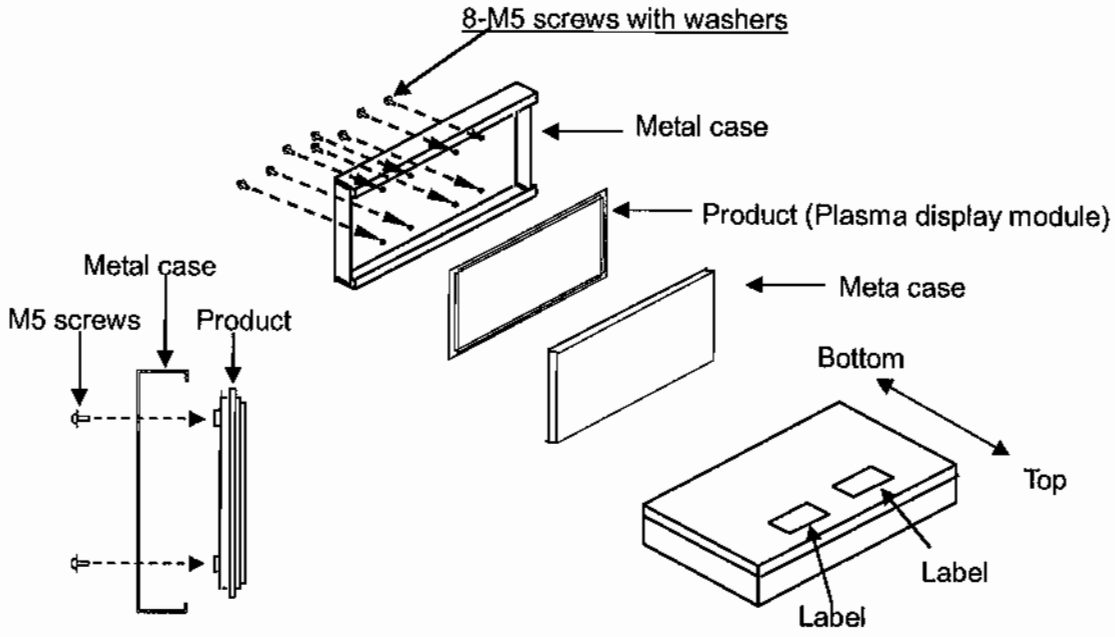

Figure 25. Packing method (Inner box)

6) Packaging method (Shipping box)

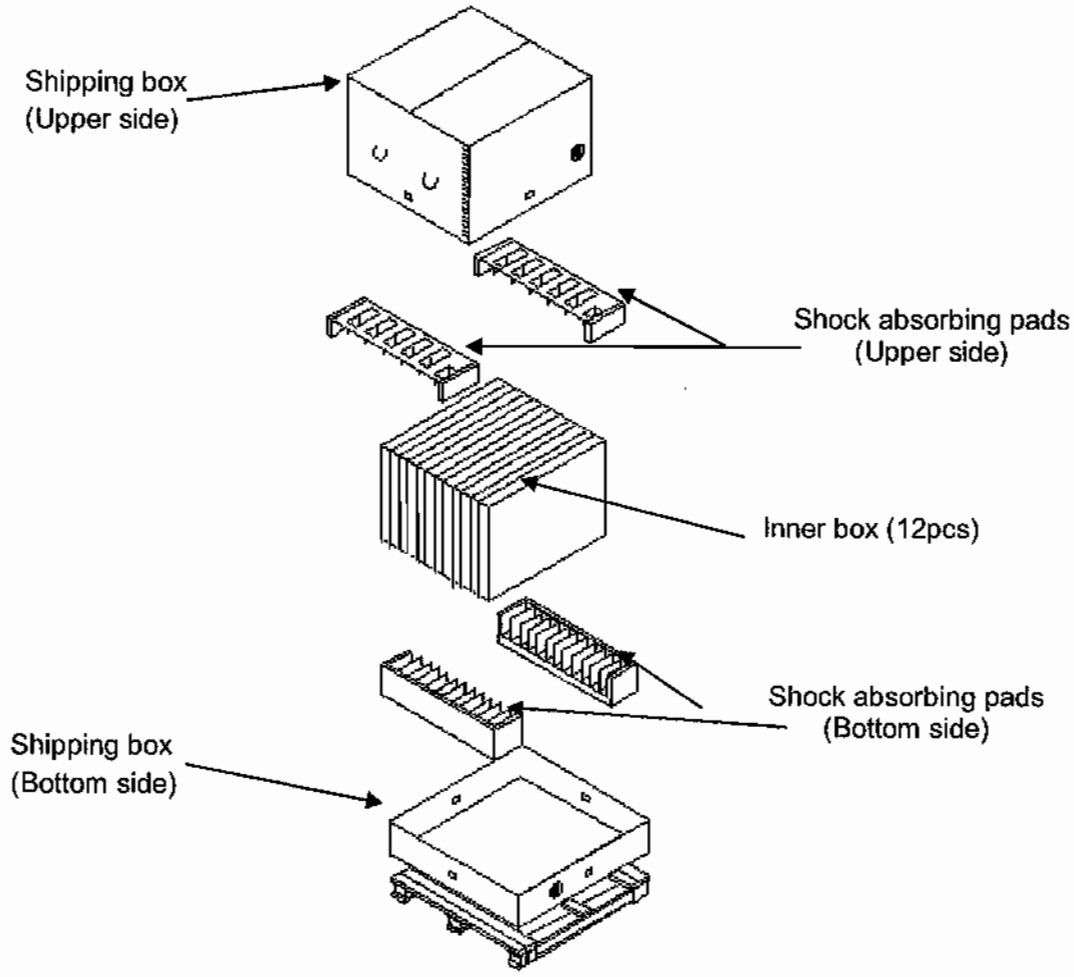

Figure 26. Packing method (shipping box)

7) Outline of Shipping box

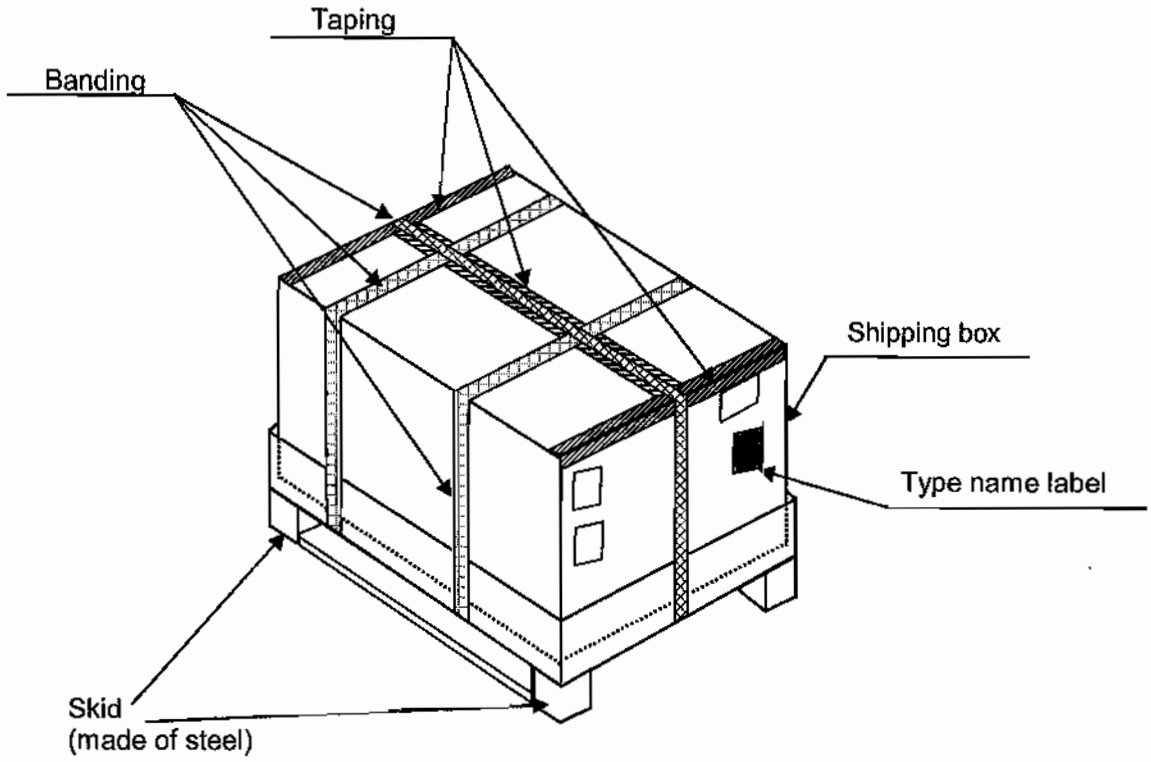

Figure 27. Outline of shipping box

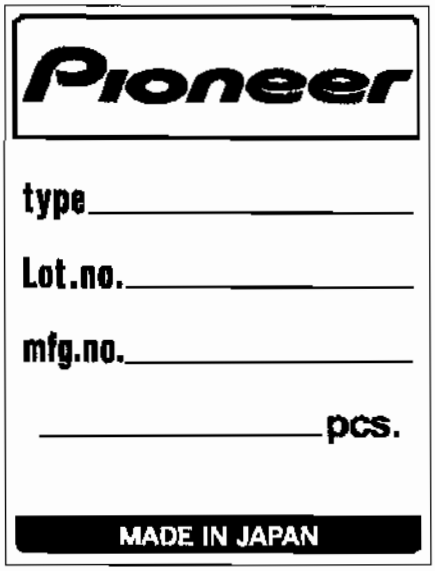

Figure 28. Type name label

<Note> Be careful not to place the packing boxes in sideways down.

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25. IMAGE STICKING CHARACTERISTICS

1) Image sticking

The fluorescent substance used in the plasma module loses its luminance with the lapse of lighting time.
This deterioration in luminance appears to be a difference in luminance in relation to the surroundings, and comes to be recognized as image sticking.

In other words, the image sticking is defined as follows: when the same pattern (of the fixed display) is displayed for a long time, a difference in luminance is caused around the lighting area and non-lighting area due to deterioration in the fluorescent substance.
When the present pattern is changed over to another one, the boundary comes to be seen between the lighting area and non-lighting area due to difference in luminance in the pattern shown shortly before changeover. If this condition is accumulated, the boundary or image sticking comes to be seen with the naked eyes.

2) Secular change in luminance

The life of luminance, defined as the reduction to half the initial level, is more than 10 thousand hours on average.
Conditions: All white (100% white) input at an ambient temperature of 25 °C.
However, this lifetime is not a guarantee value for life and luminance. It should be recognized simply as the data for reference.

3) Warranty

Image sticking and faults in luminance and picture elements are excluded from the warranty objects.

4) Cause of deterioration in luminance

A major possible cause of deterioration in luminance is damage in the fluorescent substance due to impact caused by ions generated at the time of plasma discharges.

5) Practical value for Image sticking

The relationship between integrated lighting time and luminance in this plasma module is described in the attached material. In particular, the deterioration in luminance tends to be accelerated up to 100 hours in the initial period. In the initial period, the fixed display of patterns particularly tends to cause image sticking.
The practical value for image sticking is difficult to define in concrete numerals. As described below, you are advised to take proper measures to make the occurrence of image sticking as slow as possible.

6) Proposed measures taken to relieve image sticking

So long as there is the reduction of luminance in the fluorescent substance, it is impossible to avoid the occurrence of image sticking. Therefore, to relieve image sticking, we offer you a method of entering an image input that may ensure reluctance to the generation of the difference in luminance reduction among the displayed dots.

The images from TV broadcasting involve a high rate of motion picture displays.
Therefore, there is less chance of being a cause of difference in luminance reduction among the cells. Even when the fixed patterns are displayed, they generally last for a few minutes.

Since the same pattern is less liable to be displayed, there is almost no influence toward image sticking.

If the fixed patterns tend to be displayed for a long time, however, there occurs a substantial imbalance between the lighting and non-lighting areas, thus causing a difference in luminance as a result. In this document, we offer you some proposals of installation, paying attentions to the two points: the reduction of difference in luminance achieved by integrated lighting time leveling and the method of edge smearing to make image sticking hard to be discerned.

The result from these proposals can, however, greatly depend on the contents of images and the operating environment. Therefore, we consider that it is essential to take the suitable measures in consideration of the customer's operating environment.

Example of Proposal 1: The display position is moved while the fixed display pattern is changed over, or it is scrolled during the display.

Example of Proposal 2: If possible, a pattern of complementary color is incorporated (for integrated time leveling).

Example of Proposal 3: The fixed pattern and the motion picture display are reciprocally exchanged, in order to minimize the display period of the fixed pattern.

Example of Proposal 4: During operation, the luminance of screen is suppressed as low as possible. For the display patterns, characters are indicated not on the black ground (non-picture area) but on the colored ground (mixture of R, G, B recommended).

7) Proposed countermeasures for the plasma module

Since the PDP is a display that uses a fluorescent substance like the CRT, it is a fundamental phenomenon that image sticking occurs. Unlike the CRT, the PDP gives rise to deterioration in the fluorescent substance due to impact caused by ions generated during plasma display.
As a result of the above-mentioned improvements, it is possible to extend the PDP lifetime and relieve the effect of burning, but is impossible to realize the complete elimination of burning so far as a fixed pattern is displayed for a long time.

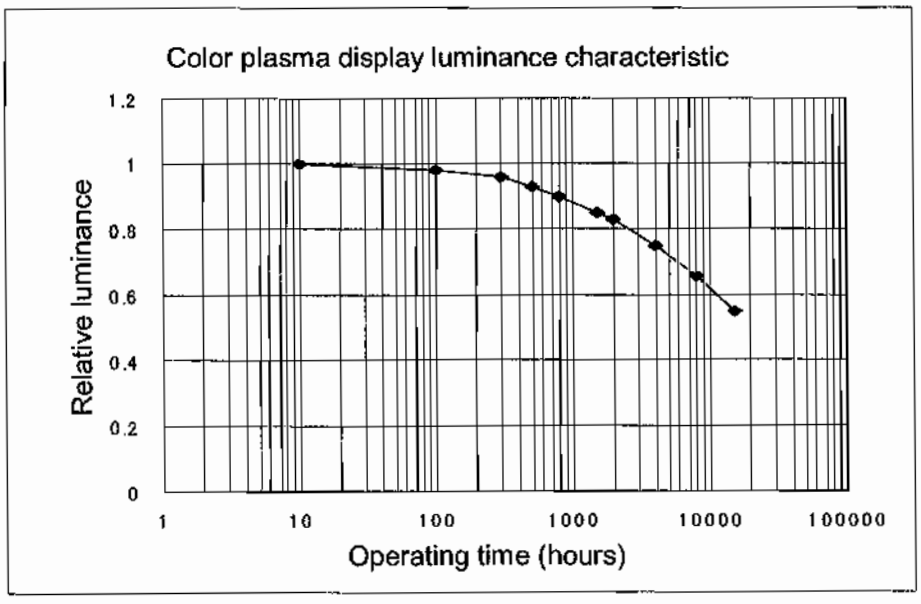

Figure 29. Color plasma display luminance characteristic

26. Usage Cautions

26.1. Cautions regarding handling of the module

(1) When taking the product out of its box, be careful to prevent shocks and stress to the panel surface.

(2) The display panel used in this product is made of glass. Since shocks or vibrations may cause it to break, be very careful during handling. In case the panel breaks, be careful not to get injured with glass fragments.

(3) Since the panel surface gets easily scratched, be careful during handling not to press against the panel or scrape it with a hard object (anything harder than a 3H pencil lead). And do not place the glass panel side down on the hard material.

(4) If the panel surface gets dirty, gently wipe it with a dry cloth. If a liquid gets on the panel, mop it up by gently applying a dry cloth without rubbing. In the case of a stubborn stain, wipe it with a cloth slightly wetted with a neutral detergent. Use only dry cloth for wiping, and avoid using the same cloth over and again. (Using an alcohol such as ethanol or chemicals such as those contained in a chemical cloth may cause discoloration of the panel surface or, depending on the type of stain, indelible fixing of the stain to the panel surface.)

(5) Deleterious substances such as described above or water drops getting into the module or somewhere on the module surface other than the display panel may damage the product.

(6) Handle the product with care, avoiding pressing against or scraping the glass panel surface, as this may leave the panel surface scratched or blemished.

(7) Be careful not to touch the port for connecting the flexible cable exposed at the rear of the module because this may cause poor contact. And, since the flexible cables are easily breakable, when handle the plasma display module, be careful not to touch the flexible cables.

(8) When moving the product, be sure to turn off the power and disconnect all the cables. While moving the product, watch your step. The product may be dropped or fall, leading to injuries or electric shock. Two or more persons should move this product. If one person attempts to carry this product alone, he/she may be injured.

(9) Make sure that the connectors are connected tightly.

26.2. Cautions regarding design and operation of the module

(1) Do not pull out or insert the power cable from/to an outlet with wet hands. Doing so may cause electric shock.

(2) This product emits near infrared rays (700 to 1100 nm) that may cause the remote controllers of other electric products to malfunction. To avoid this, use an infrared absorption filter and thoroughly evaluate the system and environment.

(3) This product uses a high voltage (approx. 400V). Do not touch the circuitry of this product with your hands when power is supplied to the product or immediately after turning off the power. Be sure to confirm that the voltage has dropped to a sufficiently low level.

(4) If you detect a strange smell or smoke coming out of the product, immediately turn off the power. Continuing to use the product under such conditions may cause electric shock or fire.

(5) Do not use this product with a voltage that exceeds the rated voltage as this may cause product failure or fire. The warranty does not cover problems that occur when the product is used under conditions other than those described in the specifications.

(6) When the product is used as a stationary text or still image display device, it may get damaged by image sticking. Image sticking is a phenomenon whereby the luminance of parts of the screen where images are continuously displayed for a long time declines compared to parts of the screen where images are displayed for a shorter cumulative time, causing

uneven screen luminance. The severity of image sticking is proportional to the cumulative display time and the brightness. Taking the following precautions reduces the possibility of image sticking.

<1> Lower the brightness as much as possible when displaying a stationary pattern.

<2> When displaying a stationary pattern, slightly vary the position of the pattern in the following sequence: Top□ Right□ Down□ Left□ Top and so on, or use scroll display.

<3> If possible, incorporate complementary color patterns to smooth the cumulative display time.

<4> Reduce the stationary pattern display time by alternating stationary pattern display and moving image display.

<5> When displaying stationary text, avoid display against a black background, and use a colored background instead.

Image sticking and faults in luminance and picture elements are excluded from the warranty objects.

(7) This product contains parts that generate heat during operation. During the set design stage, take into consideration the cooling method and design the frame based on careful evaluation of heating characteristics.

(8) The temperature of the glass surface of the display may rise to high temperature depending on the conditions of use. If you touch the glass inadvertently, you may be burned.

(9) This product uses a high-voltage drive pulse and emits electromagnetic noise. When this product is incorporated in a set, be sure to design the frame and fit an optical filter shield on the front side of the set so that the electromagnetic interference produced by the set falls within the allowed range.

(10) When installing this product in the frame of a set, use the indicated fixing screw holes and guide holes. Since the display panel of the product is made of glass, design the frame so as to prevent a large weight or shocks from being applied to the glass.

(11) When operate this product after a long storage period, the characteristics of the display image could be deteriorated or become unstable depending on the storage conditions. In this case, it is recommended to use the product after aging with full-screen white display. Required aging period will ranges from 2 to 24 hours depending on the storage period.

(12) Since this product uses precise lead pitch components, be careful to prevent any foreign materials such as metal particles come out from screw part, soldering part or metal parts of cabinet, or any liquid. These foreign materials cause the short or insulation failure of the circuit, and resulting in the product failure or fire.

(13) Follow the procedure described in these specifications for the power ON/OFF sequence. Failure to do so will cause equipment failure.

(14) This product uses highly integrated semiconductor devices. Since these devices can be damaged by static charge, be careful to handle at the place where antistatic measure is done.

(15) The sulfide causes deterioration of the product and the failure. Therefore, be careful not to place the material contains sulfur such as vulcanized rubber closed to the product.

26.3. Cautions regarding the module usage environment

(1) Operating this product when condensation has occurred may cause failure or electric shock.

(2) Avoid using this product in locations that have a lot of dust, soot, humidity, steam, etc., as this may cause failure, electric shock, or fire.

(3) Place this product on a level surface and make sure it is stably positioned because failure or electric shock may result if it falls or turns over.

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26.4. Others

(1) Do not overhaul or disassemble this product. When this module is repaired or modified without any agreement of Pioneer, it voids the warranty and Pioneer does not have any responsibility.

(2) When scrap the plasma display module or any sets installed the plasma display module, be careful to comply with laws or rules of the region or the country.

(3) When the plasma display module is resold to the third party or person, Pioneer does not have any warranty to the third party or persons.

(4) If you have any questions concerning design, such as on housing, storage, or operating environment, consult Pioneer in advance.

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27. REVISE HISTORY

Date	Contents	Remarks
Jan 21, 2005	Issue 1st edition	
Aug 31, 2005	Add "Appendix"	

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