

30V N-Channel MOS

Description

The NP44N03 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. Standard Product NP44N03 is Pb-free (meets ROHS & Sony 259 specifications).

General Features

- ◆ $V_{DS} = 30V$ $I_D = 22A$
 $R_{DS(ON)}(Typ.) = 6.3m\Omega$ @ $V_{GS} = 10V$
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 High power and current handling capability
- ◆ Lead free product is acquired
- ◆ Surface mount package

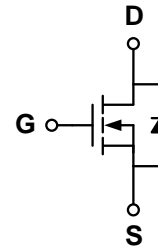
Application

- ◆ High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- ◆ Networking DC-DC Power System
- ◆ Load switch

Package

- ◆ DFN5×6-8L

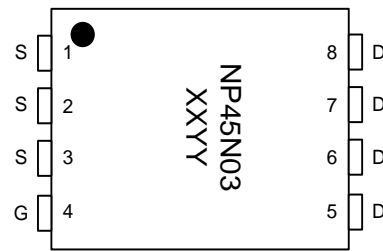
Schematic diagram



Marking and pin assignment

DFN5×6-8L

(Top View)



Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
NP44N03QR	-55°C to +150°C	DFN3×3-8L	3000

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

parameter	symbol	limit	unit
Drain-source voltage	V_{DS}	30	V
Gate-source voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	TC=25°C	45
		TC=100°C	28
Pulsed Drain Current	I_{DP}	180	A
Avalanche Current	I_{AS}	32	A
Avalanche energy(L=0.5mH)	EAS	120	mJ
Maximum power dissipation	P_D	TC=25°C	28
Power Dissipation – Derate above 25°C		TC=25°C	1.67

Operating junction Temperature range	T _j	-55—150	°C
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Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	30	-	-	V
BVDSS Temperature Coefficient	ΔBV _{DSS} /ΔT _J	Reference to 25°C, I _D =1mA		27		mV/°C
Zero gate voltage drain current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
		T _J =85°C	-	-	30	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V	-	-	±100	nA
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.6	2.5	V
Drain-source on-state resistance ¹	R _{DS(ON)}	V _{GS} =10V, I _D =22A	-	5.4	7	mΩ
		V _{GS} =4.5V, I _D =22A		9.9	12.9	
On Status Drain Current	I _{D(ON)}	V _{DS} =10V, V _{GS} =10V	50	-	-	A
Diode Characteristics						
Diode Forward Voltage ¹	V _{SD}	I _{SD} =1A, V _{GS} =0V	-	0.8	1.1	V
Diode Continuous Forward Current	I _S		-	-	46	A
Reverse Recovery Time	t _{rr}	I _F =30A,	-	9.2	-	ns
Reverse Recovery Charge	Q _{rr}	di/dt=100A/us	-	2	-	nC
Dynamic Characteristics²						
Gate Resistance	R _G	V _{GS} =0V, V _{DS} =0V, f=1MHz	-	1.7	-	
Input capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =20V f=1.0MHz	-	1317	-	pF
Output capacitance	C _{OSS}		-	163	-	
Reverse transfer capacitance	C _{RSS}		-	131	-	
Turn-on delay time	t _{D(ON)}		-	4.6	-	
Turn-on Rise time	t _r	V _{GS} =10V, V _{DD} =15V, R _L =20Ω, I _D =15A, R _G =3.3Ω	-	12.2	-	
Turn-off delay time	t _{D(OFF)}		-	26.6	-	
Turn-off Fall time	t _f		-	8	-	
Total gate charge	Q _g		V _{GS} =4.5V, I _D =15A V _{DS} =15V	-	12.6	-
Gate-source charge	Q _{gs}	-		4.2	-	
Gate-drain charge	Q _{gd}	-		5.1	-	
Drain-Source Diode Characteristics						
Diode forward voltage	V _{SD}	I _{SD} =50A, V _{GS} =0V	-	0.8	1.1	V

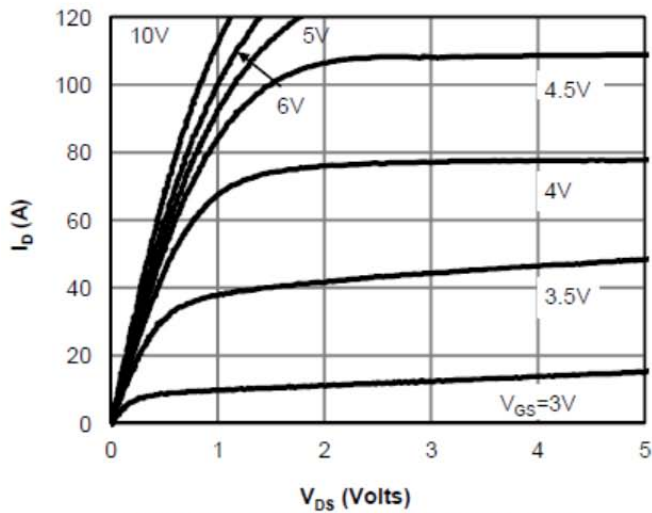
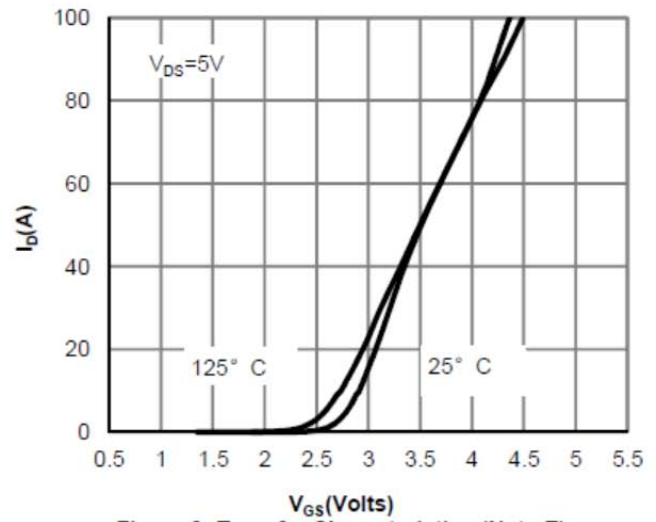
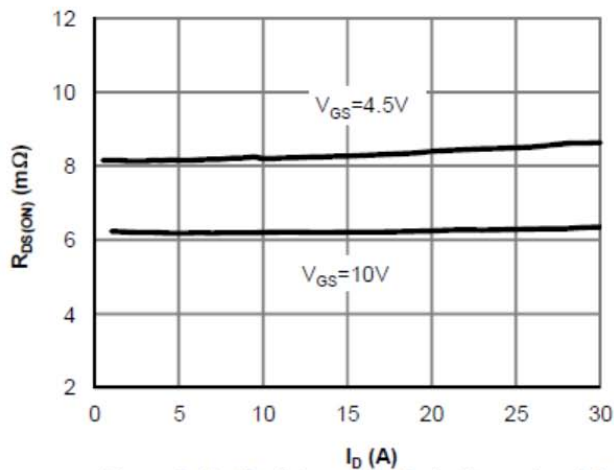
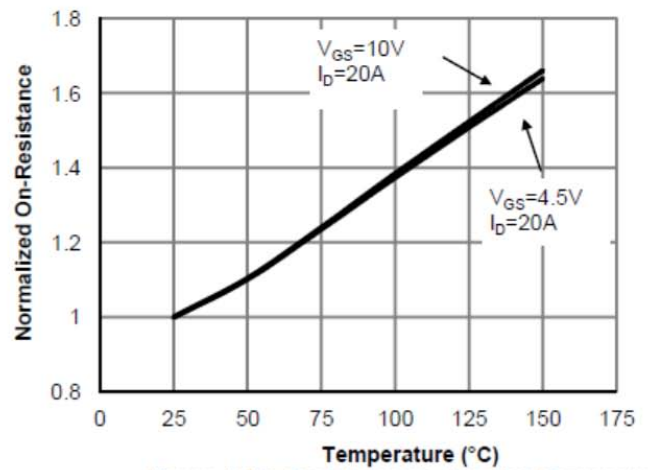
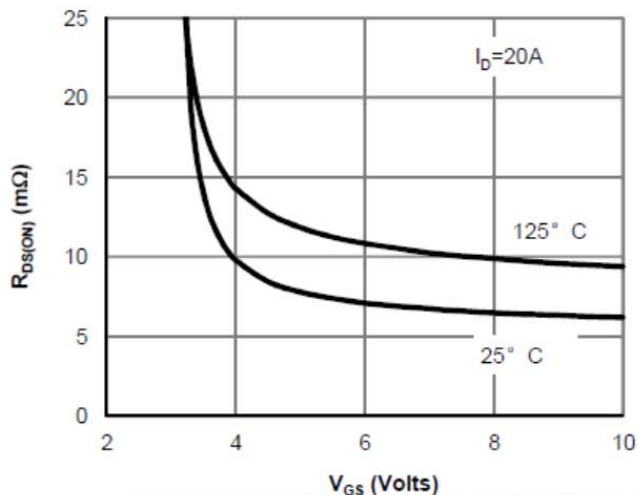
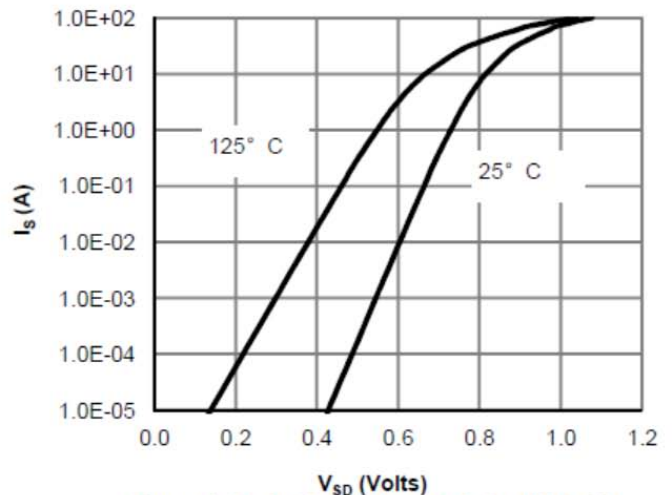
Note: 1: Pulse test; pulse width ≤ 300ns, duty cycle ≤ 2%.

2: Guaranteed by design, not subject to production testing.

Thermal Characteristics

Parameter	Symbol	Typical	Unit
Thermal Resistance-Junction to Case	Rθ _{jc}	1.7	°C/W

Typical Performance Characteristics


Fig 1: On-Region Characteristics (Note E)

Figure 2: Transfer Characteristics (Note E)

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

Figure 4: On-Resistance vs. Junction Temperature (Note E)

Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

Figure 6: Body-Diode Characteristics (Note E)

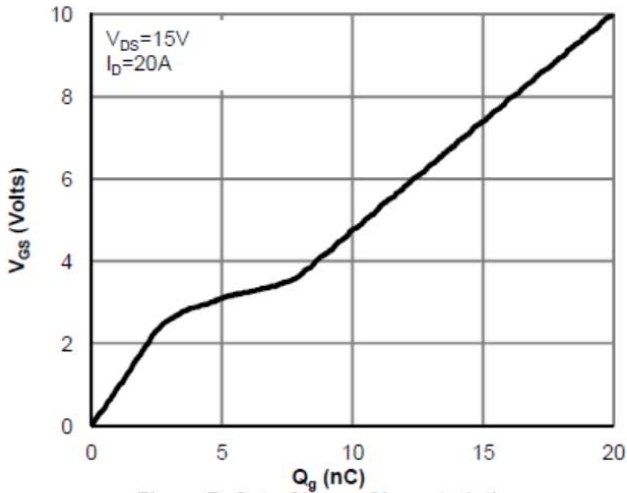


Figure 7: Gate-Charge Characteristics

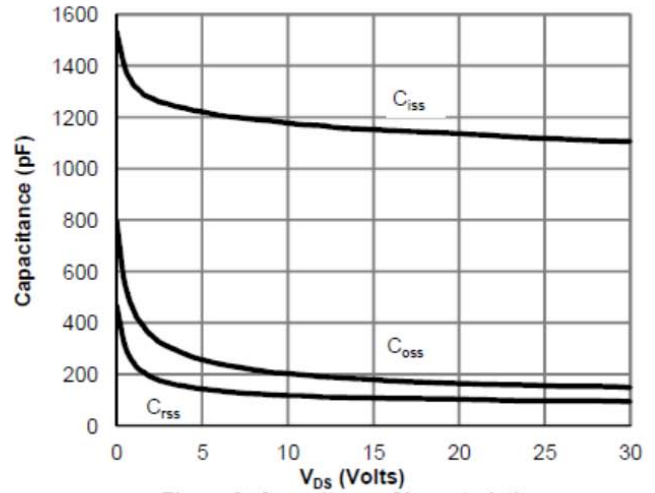


Figure 8: Capacitance Characteristics

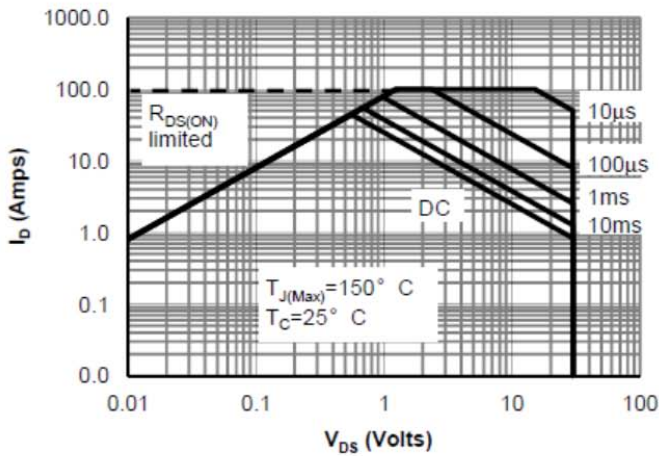


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

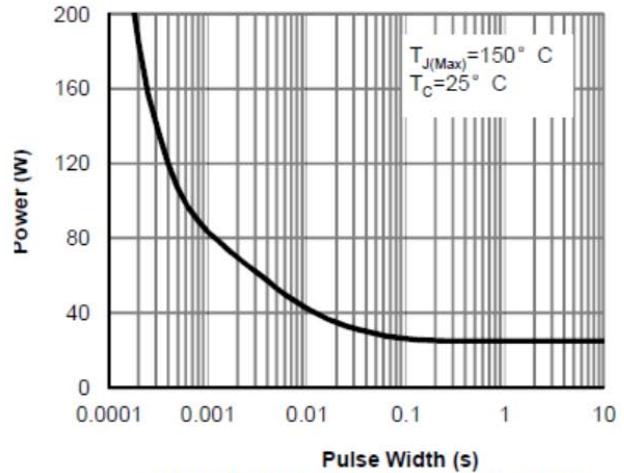


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

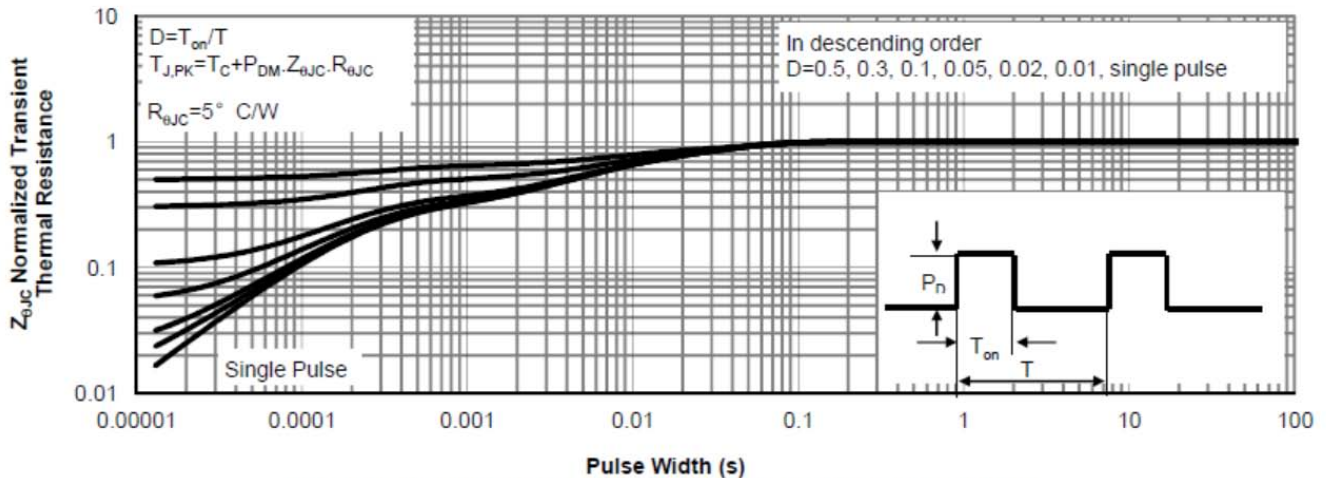


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

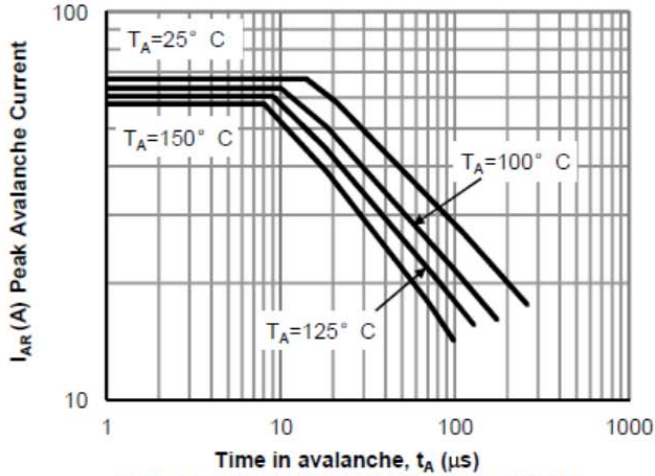


Figure 12: Single Pulse Avalanche capability (Note C)

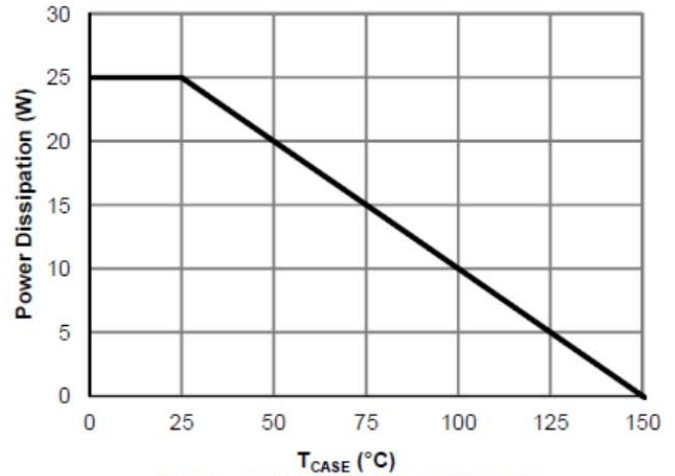


Figure 13: Power De-rating (Note F)

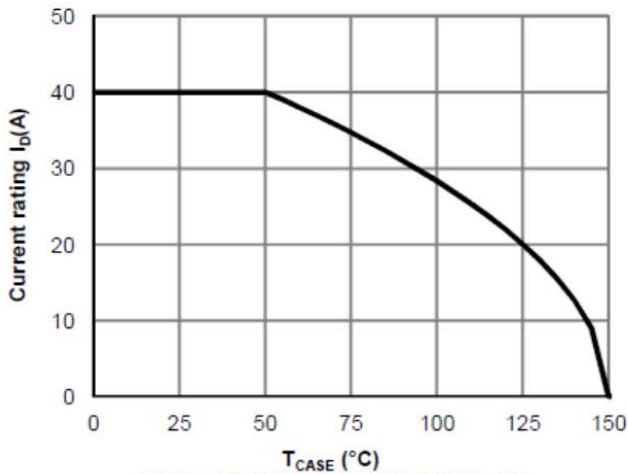


Figure 14: Current De-rating (Note F)

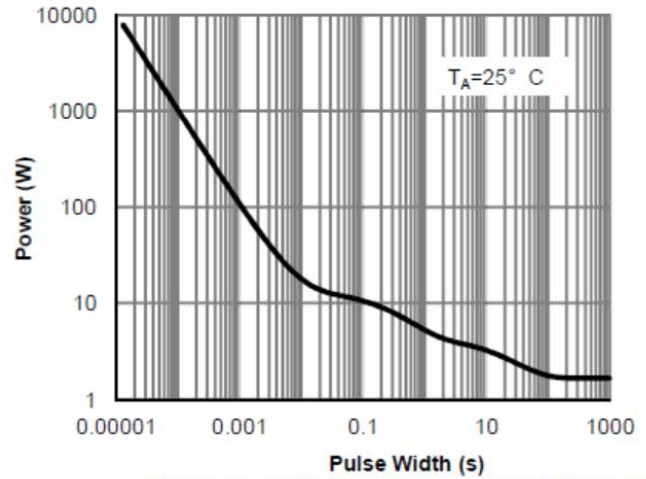


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

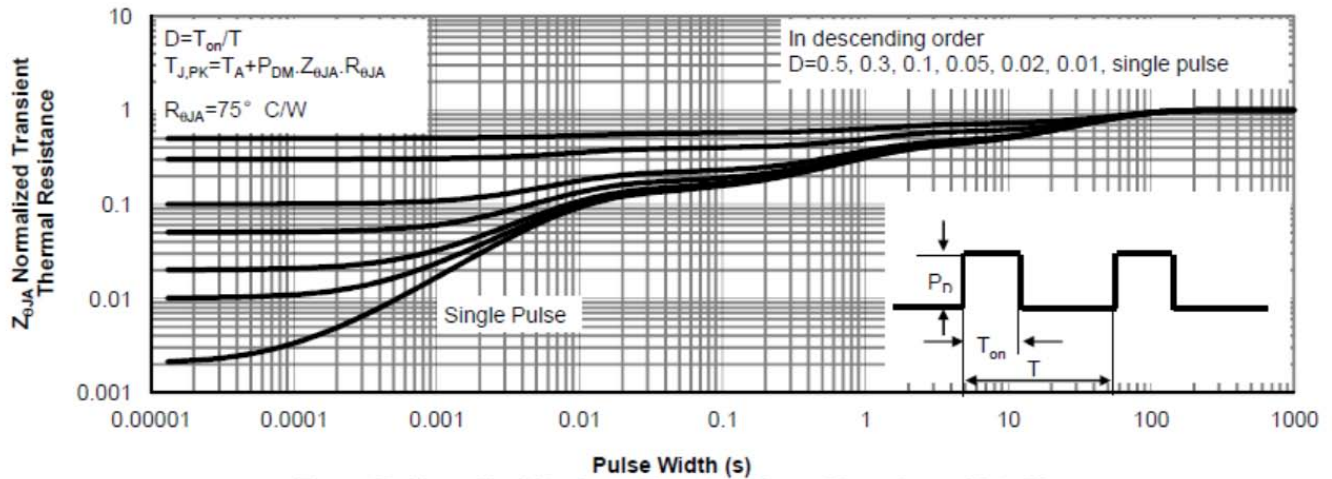
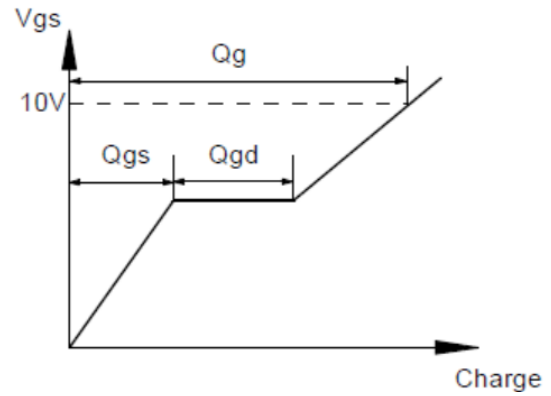
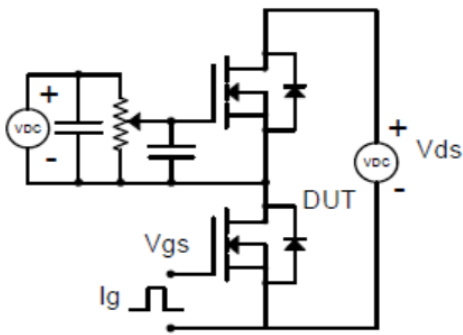
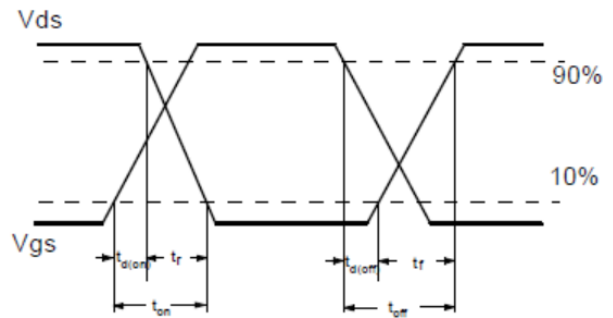
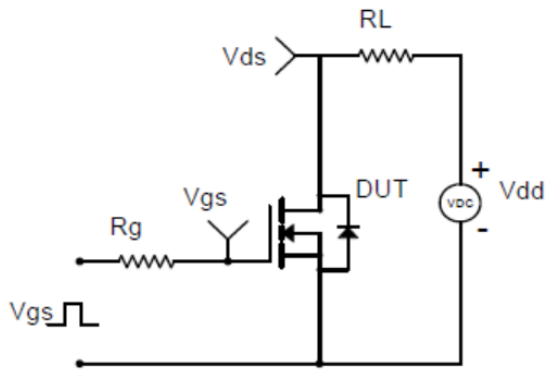


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

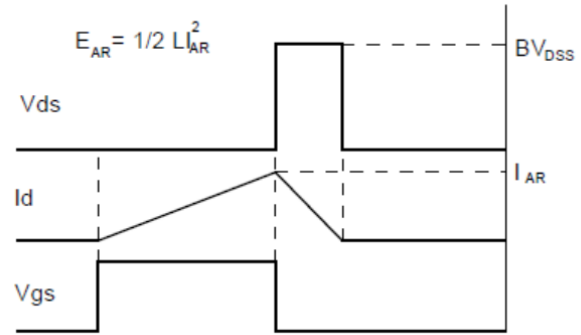
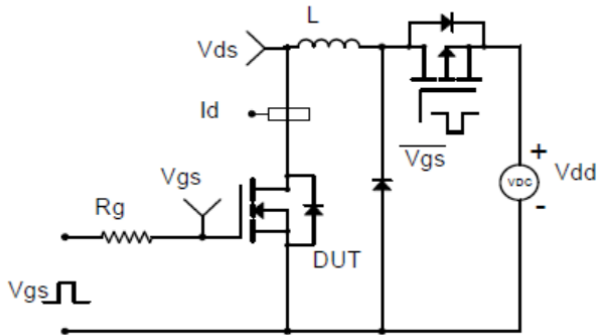
Gate Charge Test Circuit & Waveform



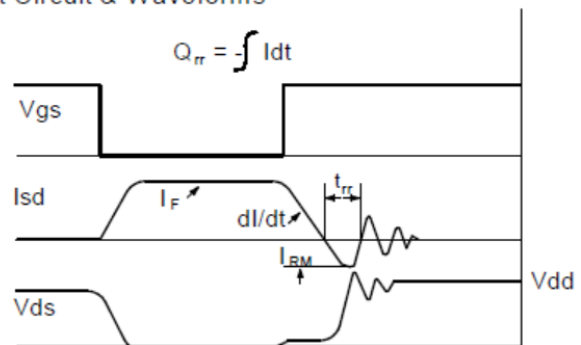
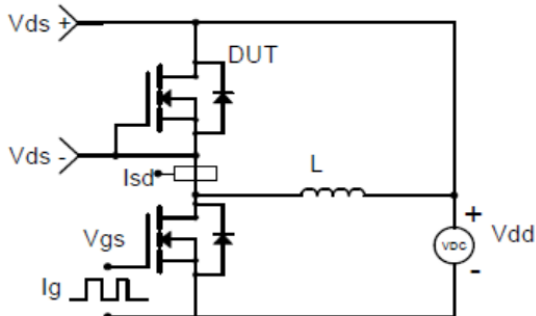
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

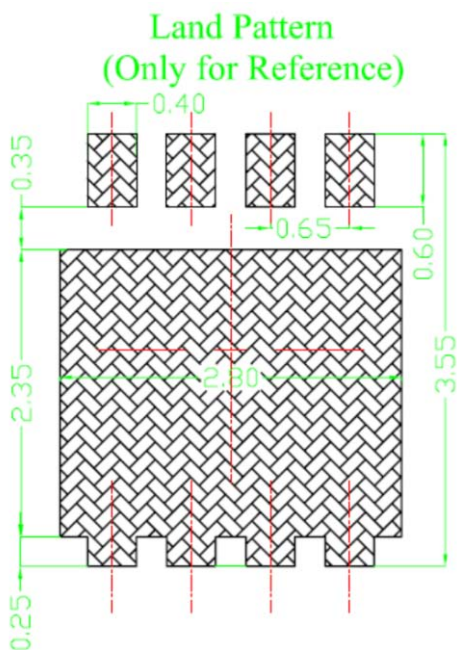
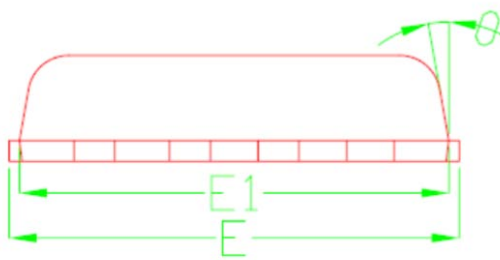
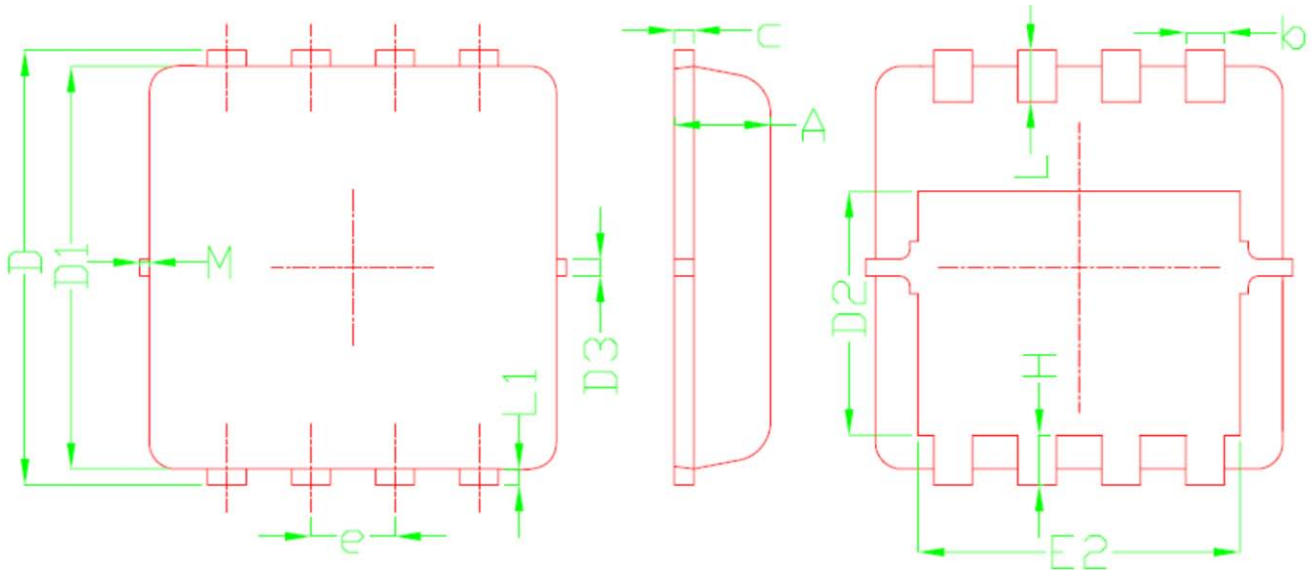


Diode Recovery Test Circuit & Waveforms



Package Information

- DFN3×3-8L



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	---	0.13	---
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
θ	---	10°	12°
M	*	*	0.15
* Not specified			