

NP55N04SLG

R07DS0242EJ0100

Rev.1.00

Feb 23, 2011

MOS FIELD EFFECT TRANSISTOR

Description

The NP55N04SLG is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Channel temperature 175 degree rating
- Super low on-state resistance
 - $R_{DS(on)1} = 6.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 28 \text{ A)}$
 - $R_{DS(on)2} = 8.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 5 \text{ V, } I_D = 28 \text{ A)}$
 - $R_{DS(on)3} = 15 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 11 \text{ A)}$
- Low input capacitance
- Gate to Source ESD protection diode built-in

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
NP55N04SLG-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	TO-252 (MP-3ZK)
NP55N04SLG-E2-AY *1			

Note: *1. Pb-free (This product does not contain Pb in external electrode.)

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	40	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 55	A
Drain Current (pulse) *1	$I_{D(pulse)}$	± 220	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	77	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +175	$^\circ\text{C}$
Repetitive Avalanche Current *2	I_{AR}	30	A
Repetitive Avalanche Energy *2	E_{AR}	90	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.95	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	125	$^\circ\text{C/W}$

Notes: *1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

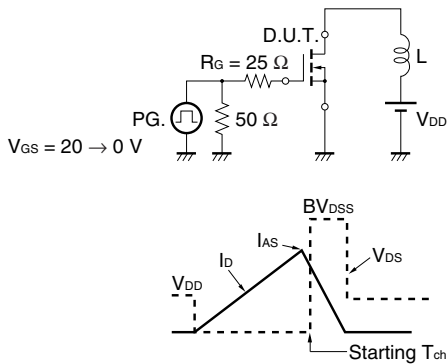
*2. Starting $T_{ch} \leq 150^\circ\text{C}$, $V_{DD} = 20 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

Electrical Characteristics (T_A = 25°C)

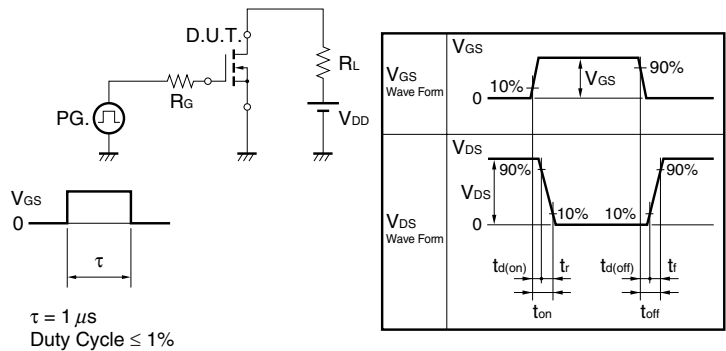
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μA	V _{DS} = 40 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0 V
Gate to Source Threshold Voltage	V _{GS(th)}	1.5	2.0	2.5	V	V _{DS} = V _{GS} , I _D = 250 μA
Forward Transfer Admittance *1	y _{fs}	12	32		S	V _{DS} = 10 V, I _D = 28 A
Drain to Source On-state Resistance *1	R _{DS(on)1}		4.7	6.5	mΩ	V _{GS} = 10 V, I _D = 28 A
	R _{DS(on)2}		5.7	8.5	mΩ	V _{GS} = 5.0 V, I _D = 28 A
	R _{DS(on)3}		6.3	15	mΩ	V _{GS} = 4.5 V, I _D = 11 A
Input Capacitance	C _{iSS}		2700	4050	pF	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz
Output Capacitance	C _{oSS}		310	465	pF	
Reverse Transfer Capacitance	C _{rSS}		200	380	pF	
Turn-on Delay Time	t _{d(on)}		15	33	ns	V _{DD} = 20 V, I _D = 28 A, V _{GS} = 10 V, R _G = 0 Ω
Rise Time	t _r		17	43	ns	
Turn-off Delay Time	t _{d(off)}		60	120	ns	
Fall Time	t _f		8	20	ns	
Total Gate Charge	Q _G		57	86	nC	V _{DD} = 32 V, V _{GS} = 10 V, I _D = 55 A
Gate to Source Charge	Q _{GS}		9		nC	
Gate to Drain Charge	Q _{GD}		17		nC	
Body Diode Forward Voltage *1	V _{F(S-D)}		0.9	1.5	V	I _F = 55 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		30		ns	I _F = 55 A, V _{GS} = 0 V, di/dt = 100 A/μs
Reverse Recovery Charge	Q _{rr}		28		nC	

Note: *1. Pulsed test

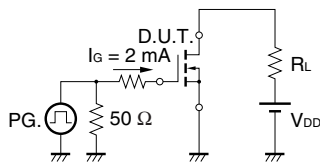
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

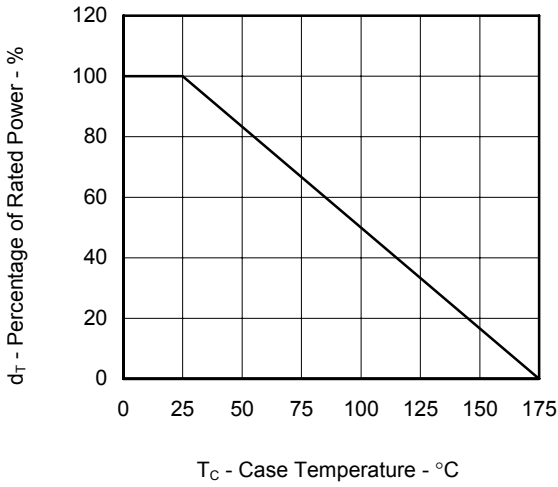


TEST CIRCUIT 3 GATE CHARGE

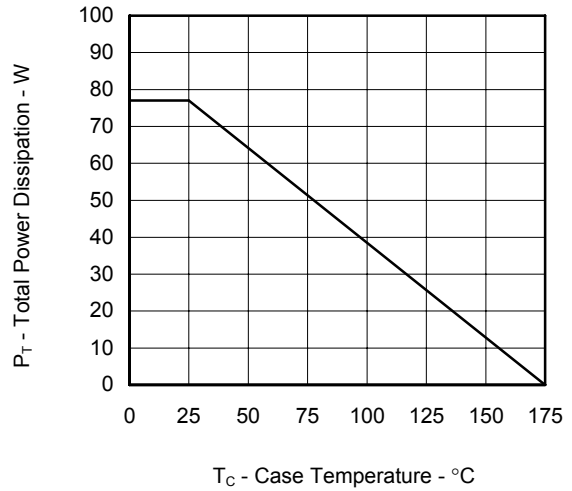


Typical Characteristics (T_A = 25°C)

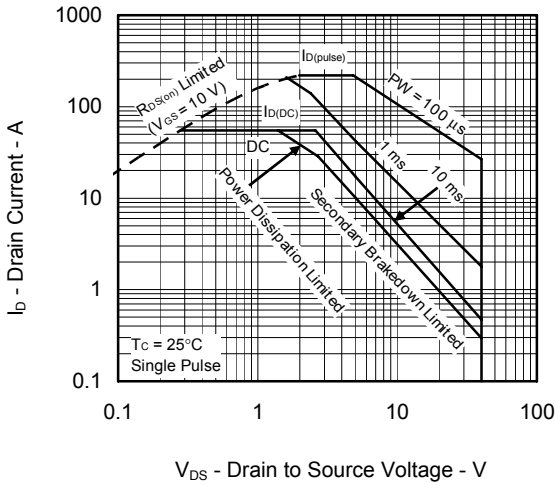
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



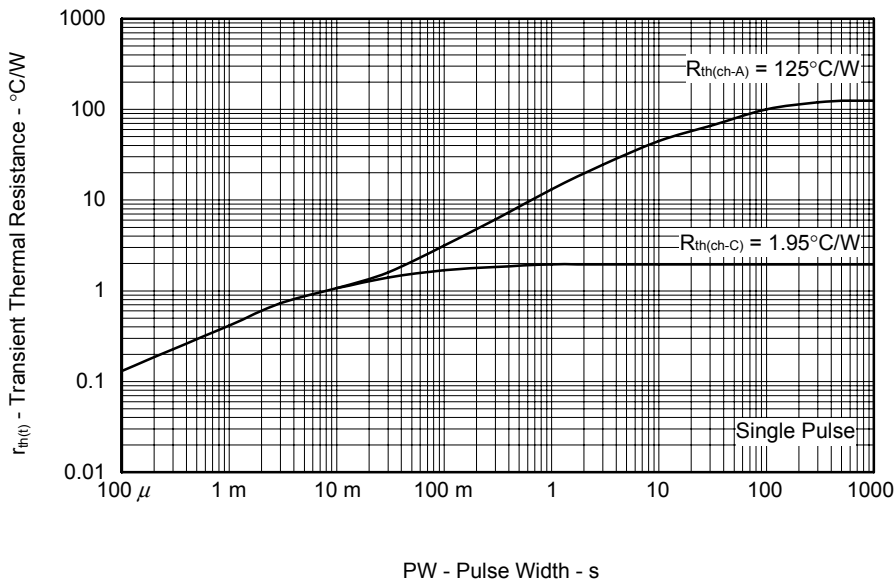
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



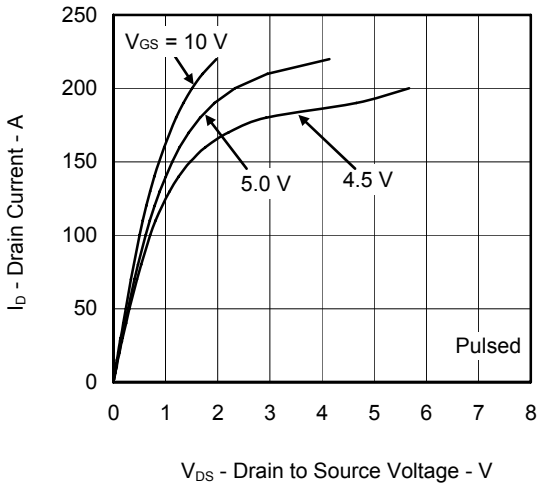
FORWARD BIAS SAFE OPERATING AREA



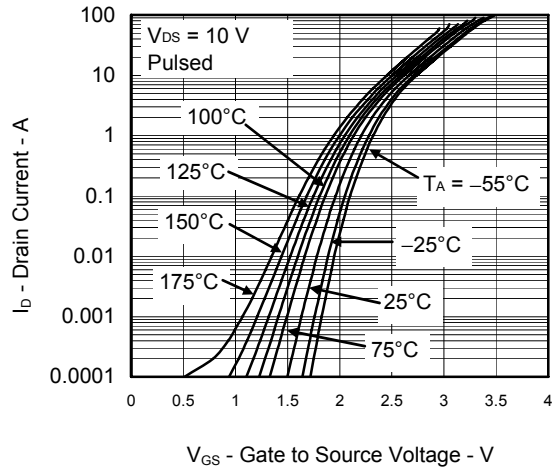
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



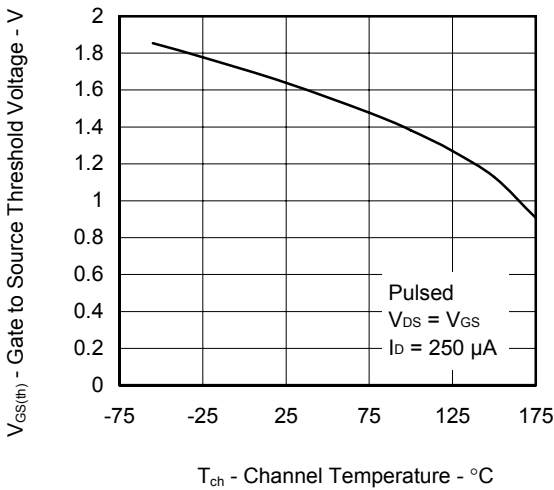
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



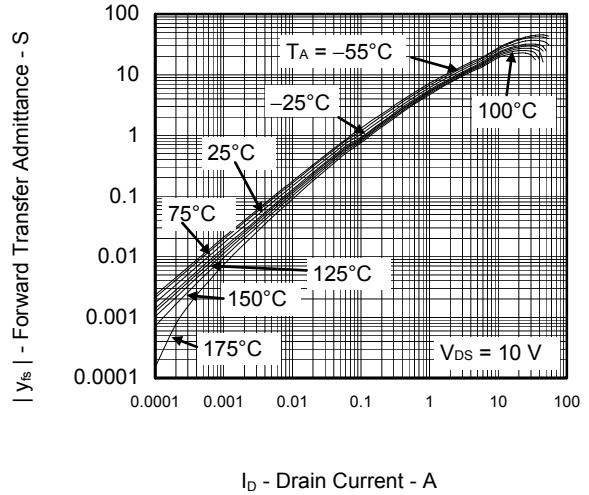
FORWARD TRANSFER CHARACTERISTICS



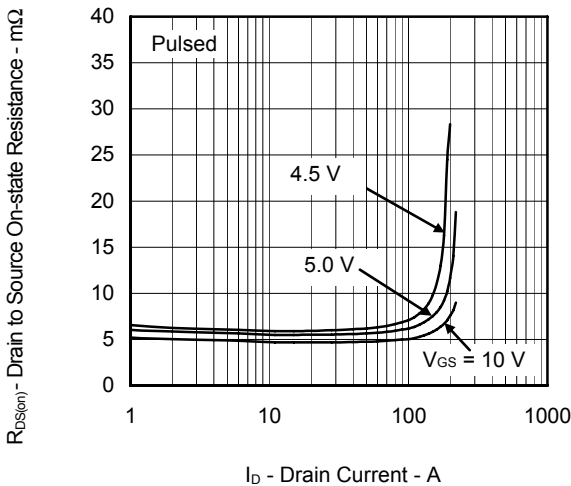
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



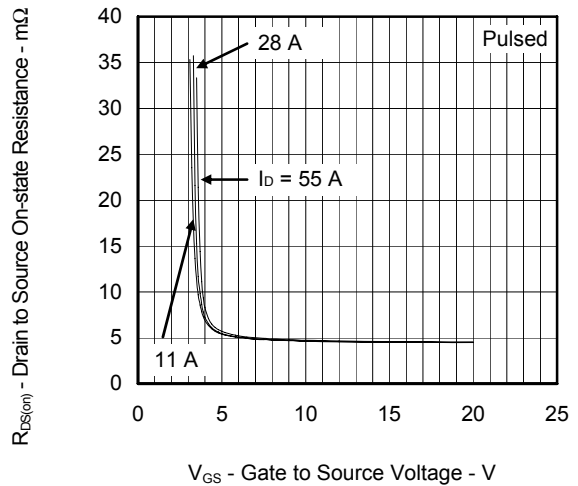
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



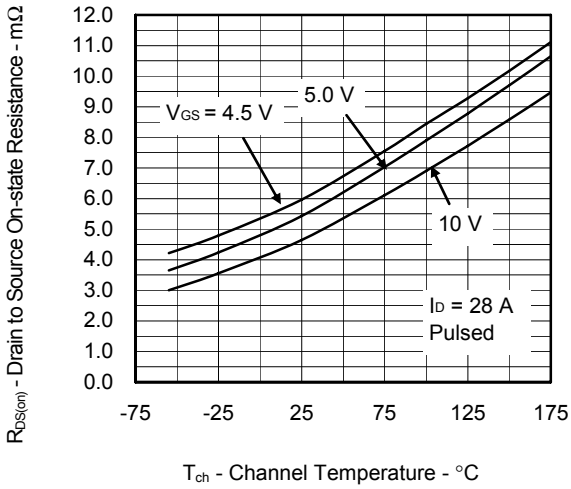
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



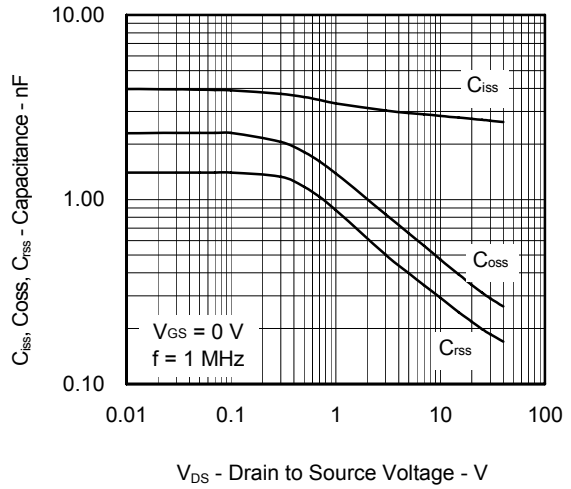
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



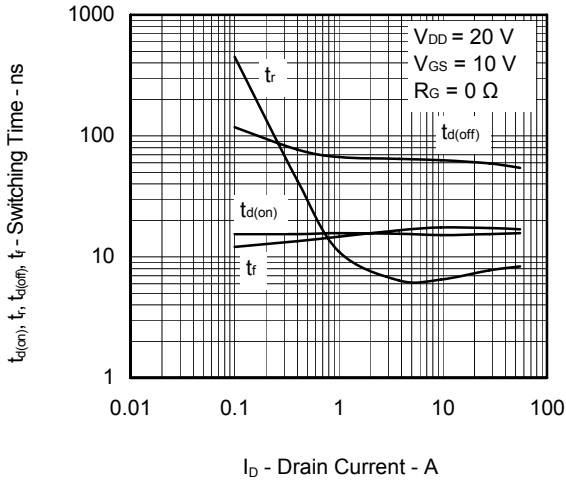
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



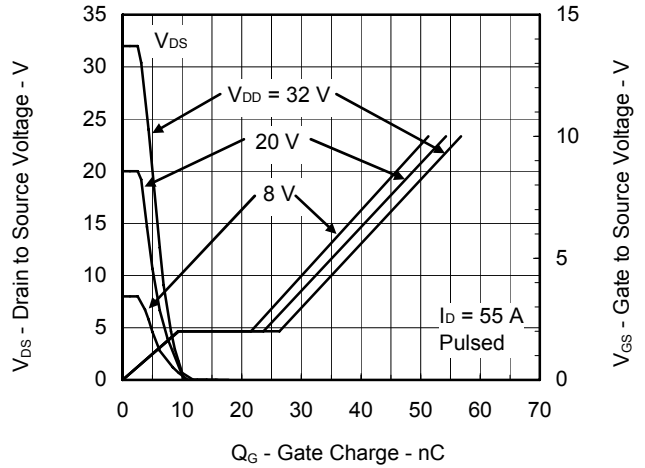
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



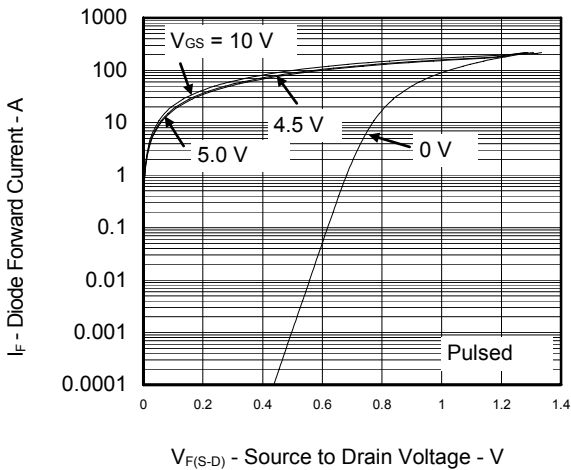
SWITCHING CHARACTERISTICS



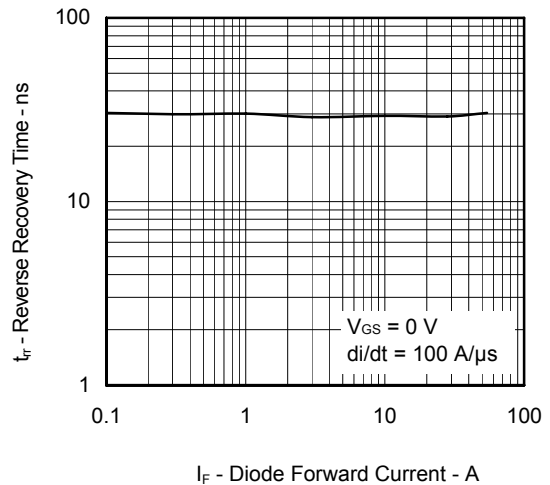
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

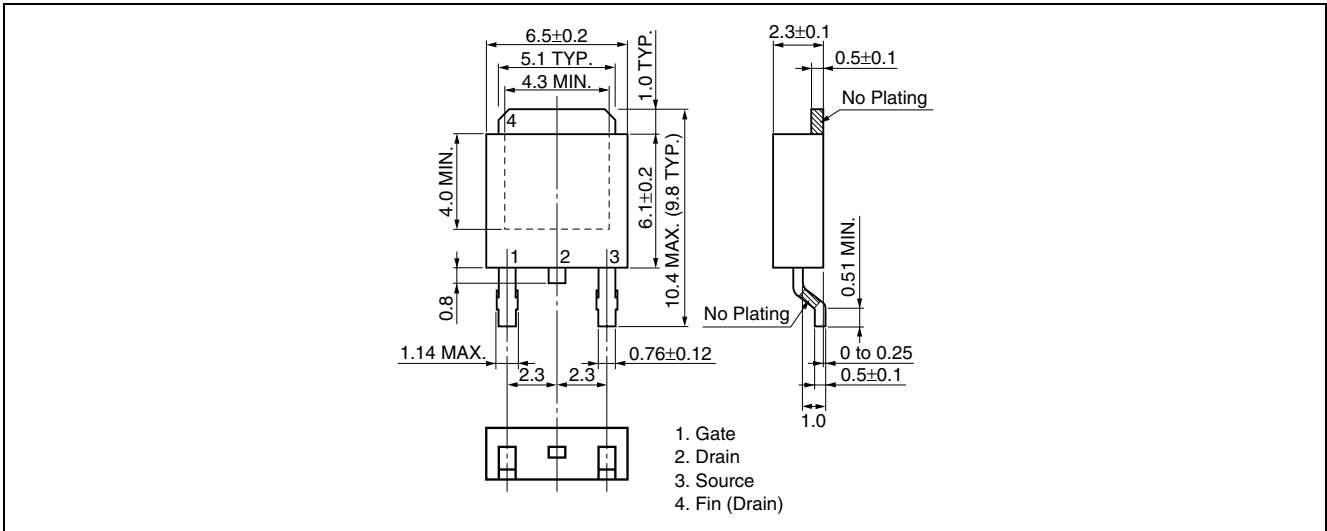


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

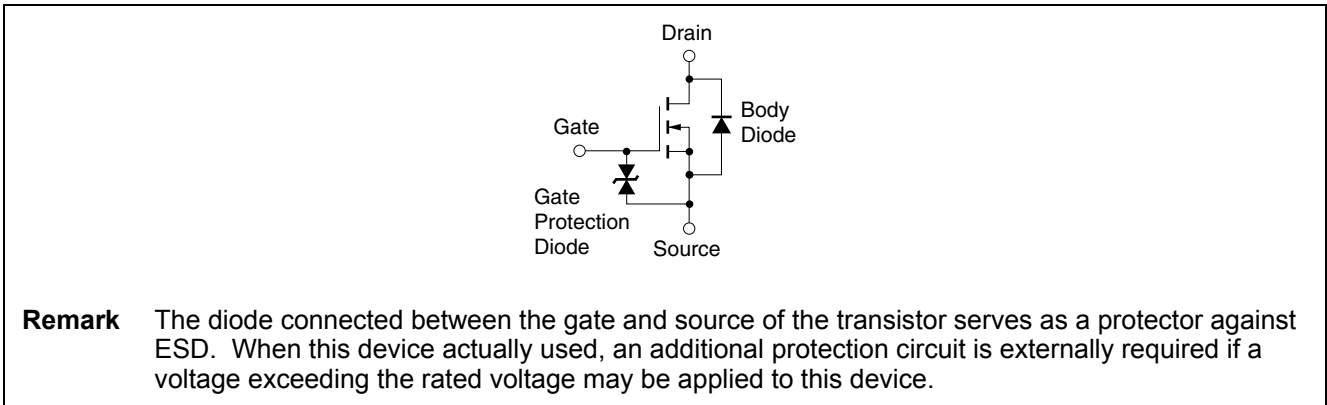


Package Drawings (Unit: mm)

TO-252 (MP-3ZK)



Equivalent Circuit



Revision History	NP55N04SLG Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Feb 23, 2011	-	First Edition Issued

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