## DATA SHEET

# MOS FIELD EFFECT TRANSISTOR

# NP80N055MDG, NP80N055NDG, NP80N055PDG

## SWITCHING
## N-CHANNEL POWER MOS FET

### DESCRIPTION

The NP80N055MDG, NP80N055NDG, and NP80N055PDG are N-channel MOS Field Effect Transistors designed for high current switching applications.

### ORDERING INFORMATION

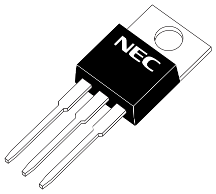
| PART NUMBER | LEAD PLATING | PACKING | PACKAGE |
|---|---|---|---|
| NP80N055MDG-S18-AY Note | Pure Sn (Tin) | Tube<br>50 p/tube | TO-220 (MP-25K) typ. 1.9 g |
| NP80N055NDG-S18-AY Note | | | TO-262 (MP-25SK) typ. 1.8 g |
| NP80N055PDG-E1B-AY Note | | Tape<br>1000 p/reel | TO-263 (MP-25ZP) typ. 1.5 g |
| NP80N055PDG-E2B-AY Note | | | |

**Note** Pb-free (This product does not contain Pb in the external electrode.)

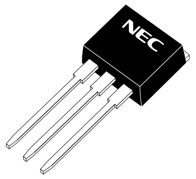
### FEATURES

- Logic level
- Super low on-state resistance
  - NP80N055MDG, NP80N055NDG
    $R_{DS(on)1}$ = 6.9 mΩ MAX. ($V_{GS}$ = 10 V, $I_D$ = 40 A)
    $R_{DS(on)2}$ = 11.2 mΩ MAX. ($V_{GS}$ = 4.5 V, $I_D$ = 35 A)
  - NP80N055PDG
    $R_{DS(on)1}$ = 6.6 mΩ MAX. ($V_{GS}$ = 10 V, $I_D$ = 40 A)
    $R_{DS(on)2}$ = 10.9 mΩ MAX. ($V_{GS}$ = 4.5 V, $I_D$ = 35 A)
- High current rating
  $I_{D(DC)}$ = ±80 A
- Low input capacitance
  $C_{iss}$ = 4600 pF TYP.
- Designed for automotive application and AEC-Q101 qualified

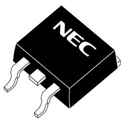
(TO-220)



(TO-262)



(TO-263)



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## ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$)

| | | | |
|---|---|---|---|
| Drain to Source Voltage ($V_{GS} = 0$ V) | $V_{DSS}$ | 55 | V |
| Gate to Source Voltage ($V_{DS} = 0$ V) | $V_{GSS}$ | ±20 | V |
| Drain Current (DC) ($T_C = 25°C$) | $I_{D(DC)}$ | ±80 | A |
| Drain Current (pulse) Note1 | $I_{D(pulse)}$ | ±200 | A |
| Total Power Dissipation ($T_C = 25°C$) | $P_{T1}$ | 115 | W |
| Total Power Dissipation ($T_A = 25°C$) | $P_{T2}$ | 1.8 | W |
| Channel Temperature | $T_{ch}$ | 175 | °C |
| Storage Temperature | $T_{stg}$ | −55 to +175 | °C |
| Repetitive Avalanche Current Note2 | $I_{AR}$ | 33 | A |
| Repetitive Avalanche Energy Note2 | $E_{AR}$ | 111 | mJ |

**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1%

**2.** $T_{ch} \leq 150°C$, $R_G = 25\ \Omega$

## THERMAL RESISTANCE

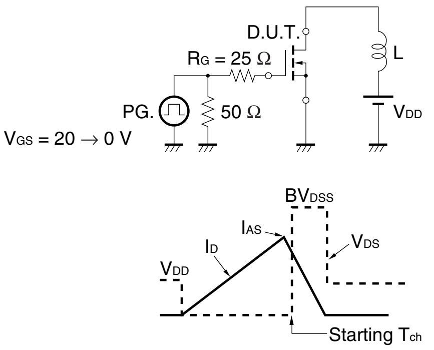
| | | | |
|---|---|---|---|
| Channel to Case Thermal Resistance | $R_{th(ch-C)}$ | 1.30 | °C/W |
| Channel to Ambient Thermal Resistance | $R_{th(ch-A)}$ | 83.3 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C)

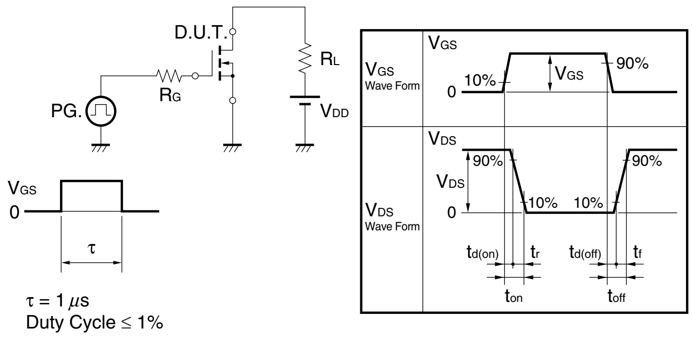
| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 55 V, $V_{GS}$ = 0 V | | | 1 | μA |
| Gate Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| Gate to Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 1.4 | | 2.5 | V |
| Forward Transfer Admittance **Note** | $\lvert y_{fs} \rvert$ | $V_{DS}$ = 5 V, $I_D$ = 35 A | 25 | 64 | | S |
| Drain to Source On-state Resistance **Note** | $R_{DS(on)1}$ | $V_{GS}$ = 10 V, $I_D$ = 40 A<br>NP80N055MDG, NP80N055NDG | | 5.4 | 6.9 | mΩ |
| | | $V_{GS}$ = 10 V, $I_D$ = 40 A<br>NP80N055PDG | | 4.8 | 6.6 | mΩ |
| | $R_{DS(on)2}$ | $V_{GS}$ = 4.5 V, $I_D$ = 35 A<br>NP80N055MDG, NP80N055NDG | | 6.3 | 11.2 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 35 A<br>NP80N055PDG | | 5.9 | 10.9 | mΩ |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 25 V, | | 4600 | 6900 | pF |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V, | | 390 | 590 | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | f = 1 MHz | | 240 | 430 | pF |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$ = 28 V, $I_D$ = 40 A, | | 17 | 37 | ns |
| Rise Time | $t_r$ | $V_{GS}$ = 10 V, | | 13 | 33 | ns |
| Turn-off Delay Time | $t_{d(off)}$ | $R_G$ = 0 Ω | | 77 | 154 | ns |
| Fall Time | $t_f$ | | | 7 | 18 | ns |
| Total Gate Charge | $Q_G$ | $V_{DD}$ = 44 V, | | 90 | 135 | nC |
| Gate to Source Charge | $Q_{GS}$ | $V_{GS}$ = 10 V, | | 13 | | nC |
| Gate to Drain Charge | $Q_{GD}$ | $I_D$ = 80 A | | 26 | | nC |
| Body Diode Forward Voltage **Note** | $V_{F(S-D)}$ | $I_F$ = 80 A, $V_{GS}$ = 0 V | | 0.95 | 1.5 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = 80 A, $V_{GS}$ = 0 V, | | 38 | | ns |
| Reverse Recovery Charge | $Q_{rr}$ | di/dt = 100 A/μs | | 45 | | nC |

**Note** Pulsed test

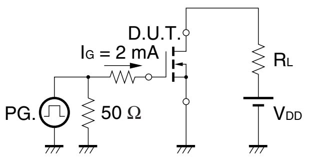
### TEST CIRCUIT 1 AVALANCHE CAPABILITY



### TEST CIRCUIT 2 SWITCHING TIME

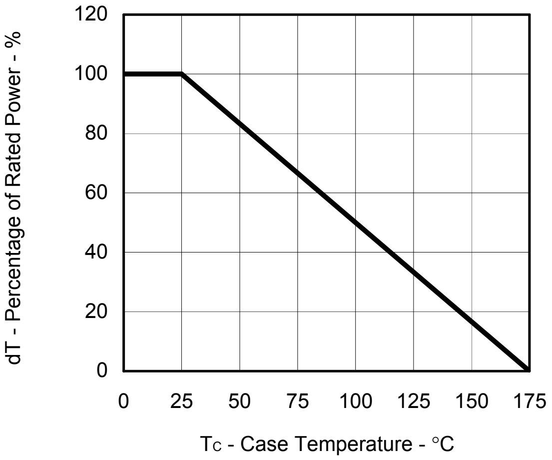


### TEST CIRCUIT 3 GATE CHARGE

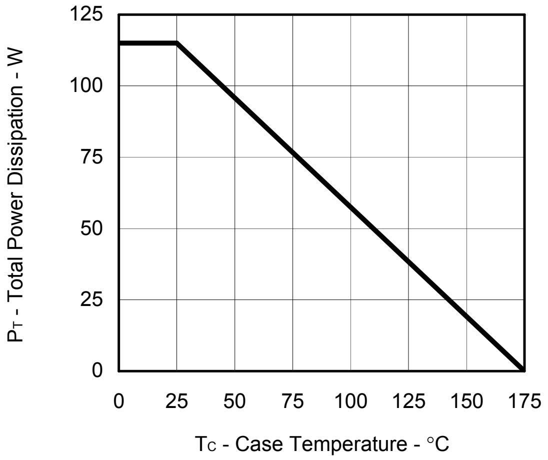


## TYPICAL CHARACTERISTICS ($T_A$ = 25°C)

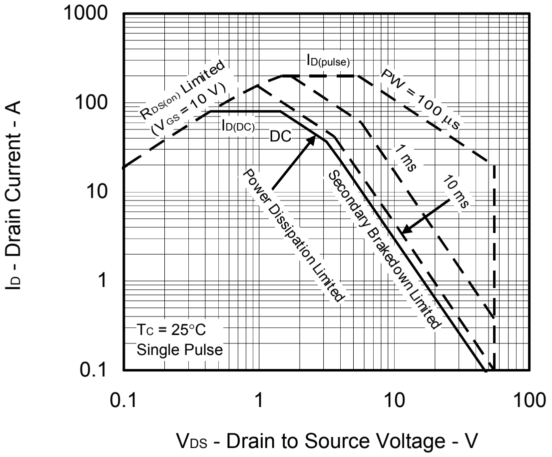
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



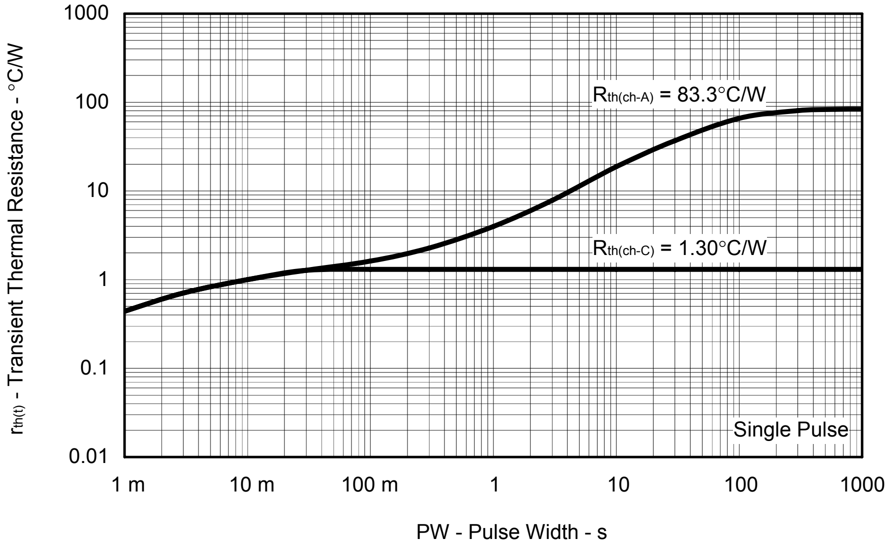
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



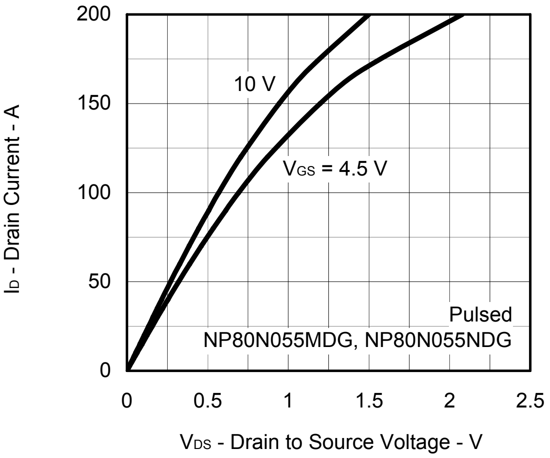
FORWARD BIAS SAFE OPERATING AREA



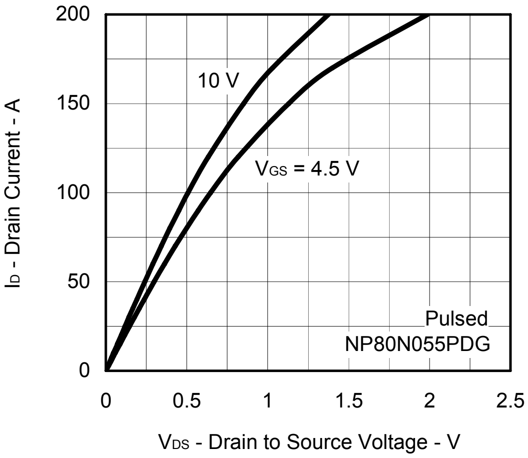
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



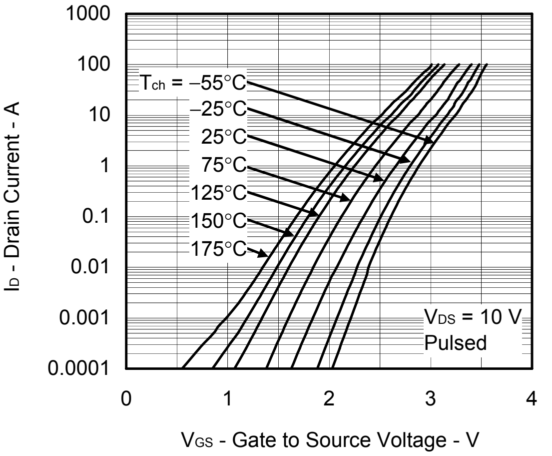
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



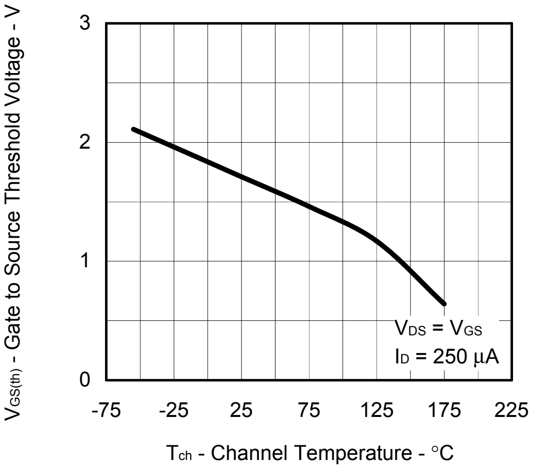
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



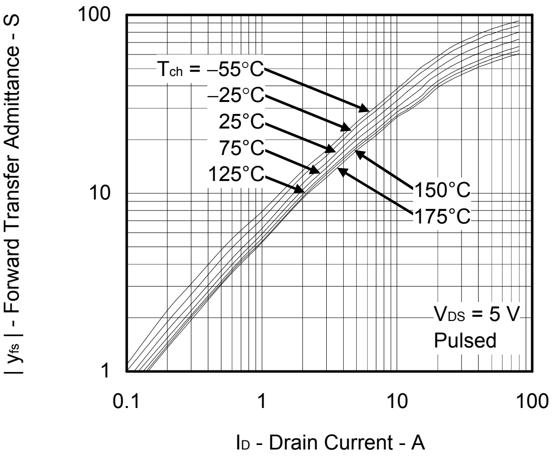
FORWARD TRANSFER CHARACTERISTICS



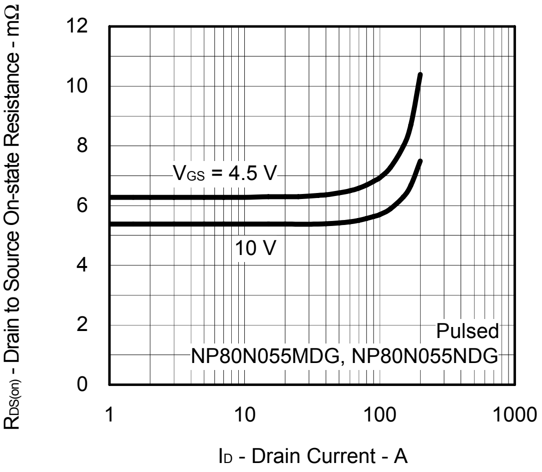
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



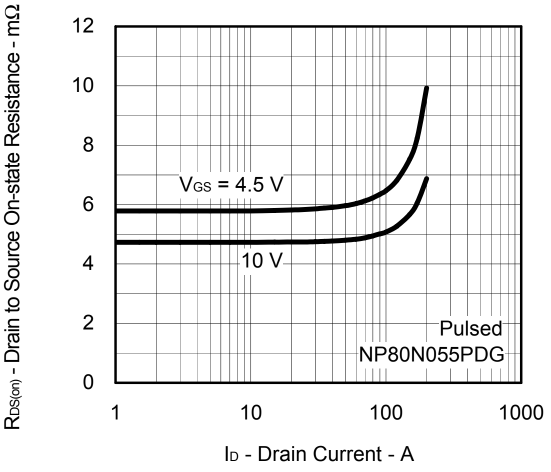
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



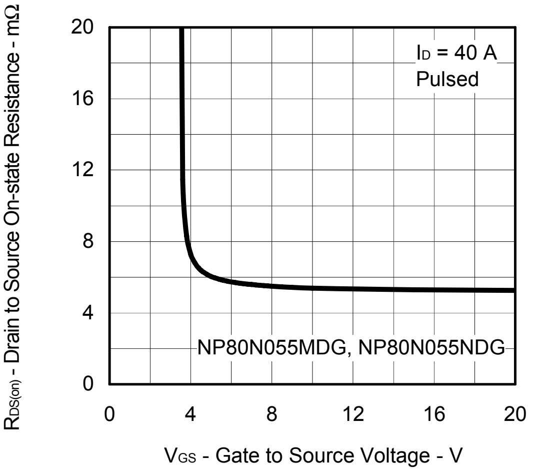
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



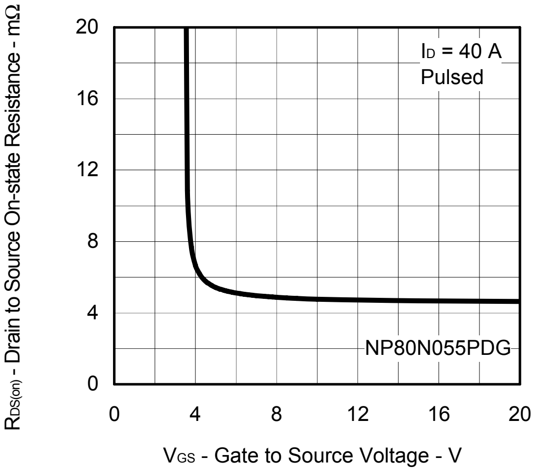
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



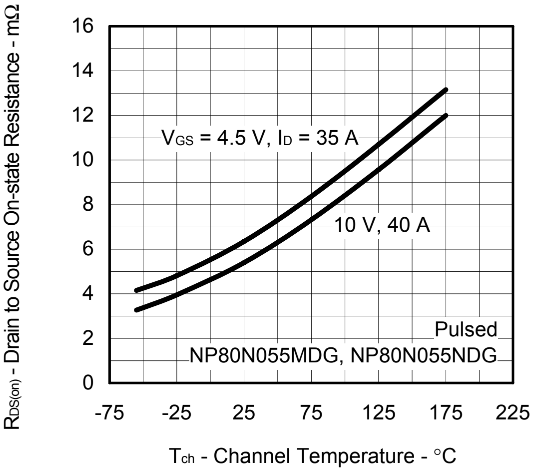
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



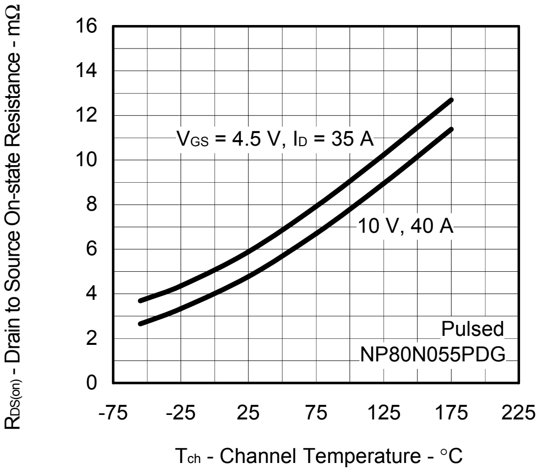
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



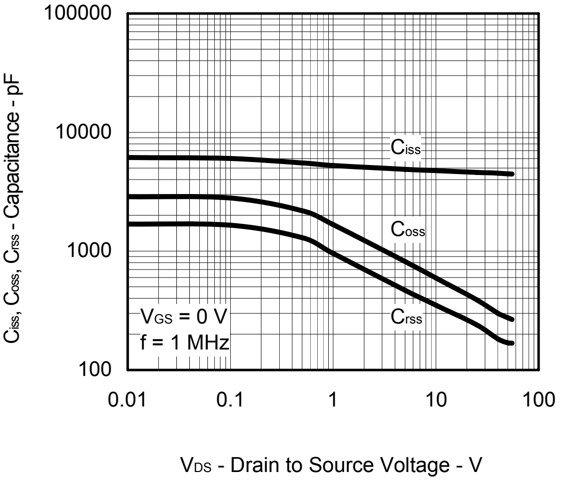
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



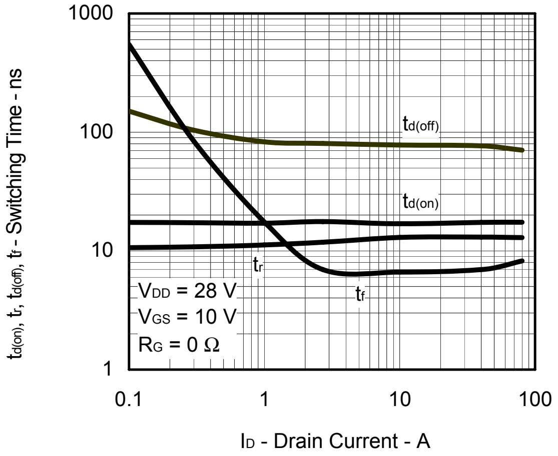
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



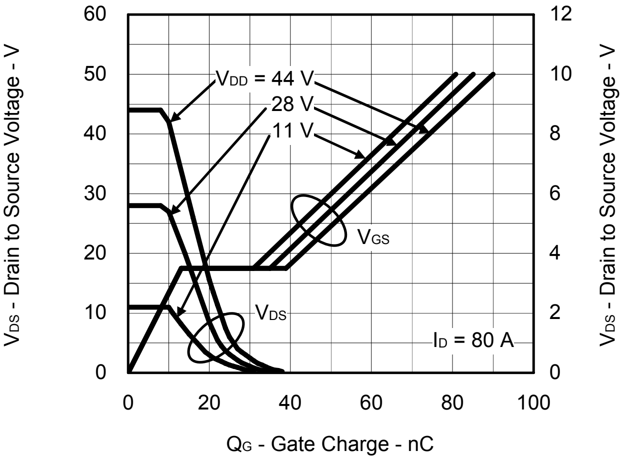
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



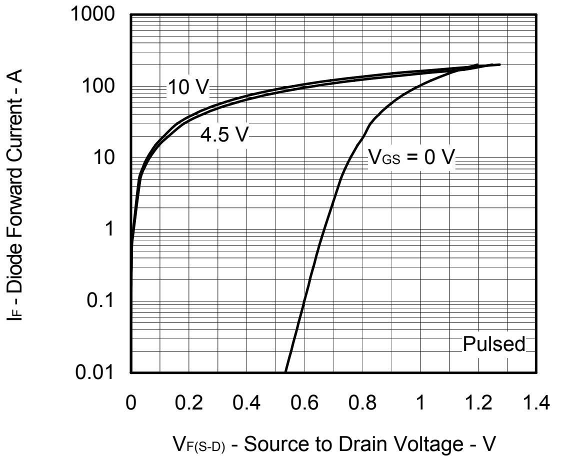
SWITCHING CHARACTERISTICS



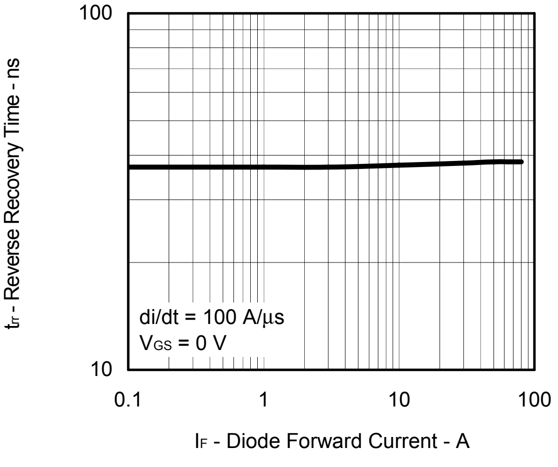
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

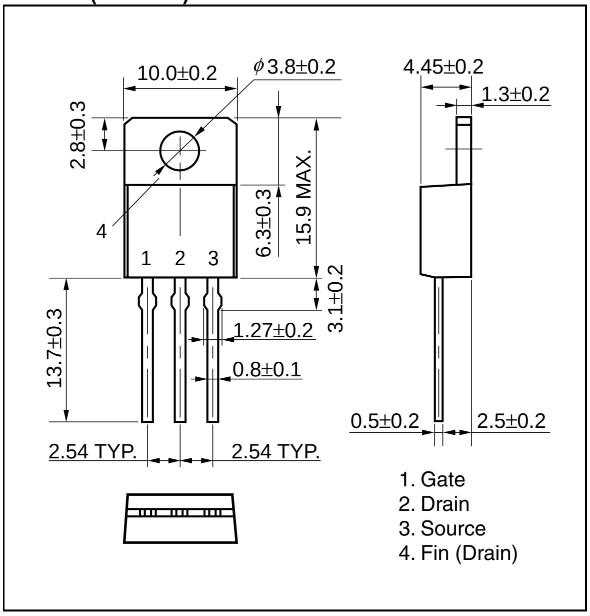


REVERSE RECOVERY TIME vs.
DIODE FORWARD CURRENT

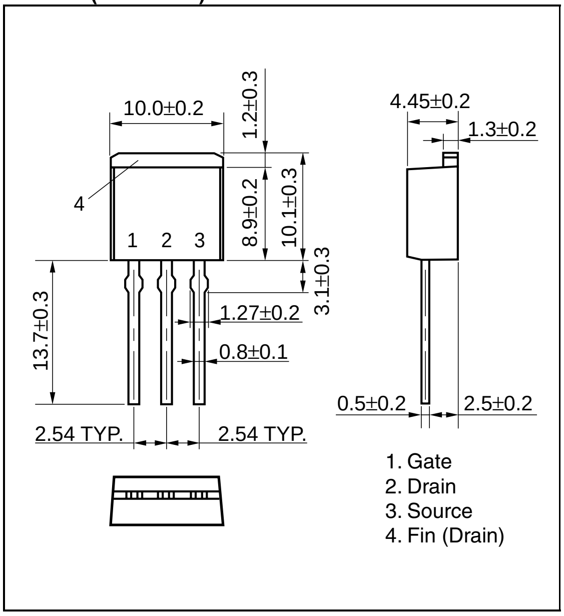


## PACKAGE DRAWINGS (Unit: mm)

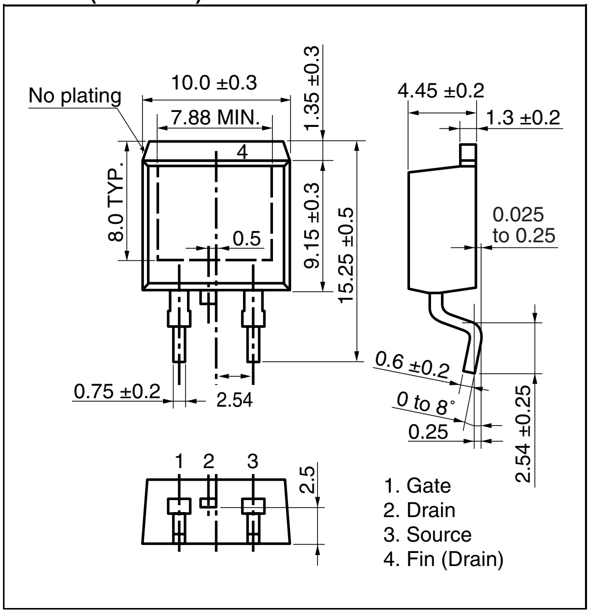
**TO-220 (MP-25K)**



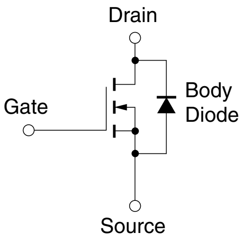
**TO-262 (MP-25SK)**



**TO-263 (MP-25ZP)**



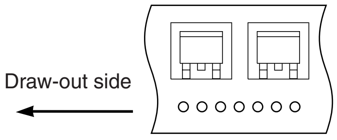
## EQUIVALENT CIRCUIT



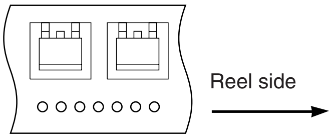
**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

## TAPE INFORMATION (NP80N055PDG)

There are two types (-E1B, -E2B) of taping depending on the direction of the device.

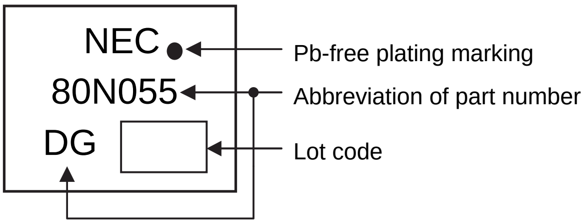


−E1B TYPE



−E2B TYPE

## MARKING INFORMATION



## RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|---|---|---|
| Infrared reflow<br>NP80N055PDG | Maximum temperature (Package's surface temperature): 260°C or below<br>Time at maximum temperature: 10 seconds or less<br>Time of temperature higher than 220°C: 60 seconds or less<br>Preheating time at 160 to 180°C: 60 to 120 seconds<br>Maximum number of reflow processes: 3 times<br>Maximum chlorine content of rosin flux (percentage mass): 0.2% or less | IR60-00-3 |
| Wave soldering<br>NP80N055MDG,<br>NP80N055NDG | Maximum temperature (Solder temperature): 260°C or below<br>Time: 10 seconds or less<br>Maximum chlorine content of rosin flux: 0.2% (wt.) or less | THDWS |
| Partial heating<br>NP80N055MDG,<br>NP80N055NDG,<br>NP80N055PDG | Maximum temperature (Pin temperature): 350°C or below<br>Time (per side of the device): 3 seconds or less<br>Maximum chlorine content of rosin flux: 0.2% (wt.) or less | P350 |

**Caution Do not use different soldering methods together (except for partial heating).**

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