RENESAS

MOS FIELD EFFECT TRANSISTOR

NP80N06CLD,NP80N06DLD,NP80N06ELD

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Channel Temperature 175 degree rated
- Super Low On-state Resistance
  $R_{DS(on)1}$ = 13 mΩ (MAX.) (V_{GS} = 10 V, I_D = 40 A)
  $R_{DS(on)2}$ = 17 mΩ (MAX.) (V_{GS} = 5 V, I_D = 40 A)
- Low C_{iss} : C_{iss} = 2360 pF (TYP.)
- Built-in Gate protection diode

ORDERING INFORMATION

PART NUMBER	PACKAGE
NP80N06CLD	TO-220AB
NP80N06DLD	TO-262
NP80N06ELD	TO-263

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±80	A
Drain Current (Pulse) Note1	$I_{D(pulse)}$	±210	A
Total Power Dissipation (T_A = 25 °C)	P_T	1.8	W
Total Power Dissipation (T_{ch} = 25 °C)	P_T	100	W
Single Avalanche Current	I_{AS}	TBD	A
Single Avalanche Energy Note2	E_{AS}	TBD	mJ
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to + 175	°C

Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1 %

2. Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V →0

THERMAL RESISTANCE

Channel to Case	Rth(ch-C)	1.50	°C/W
Channel to Ambient	Rth(ch-A)	83.3	°C/W

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

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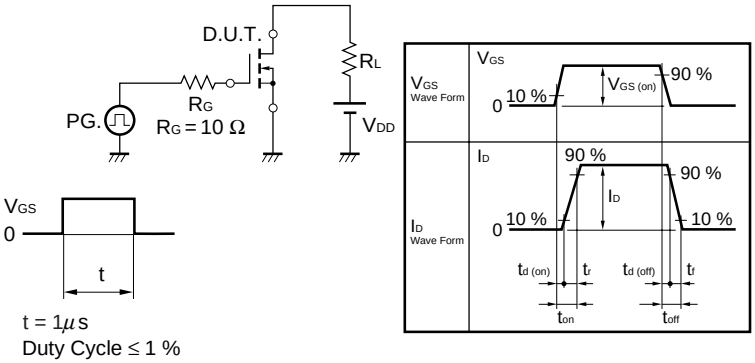
ELECTRICAL CHRACTERISTICS (T_A = 25 °C)

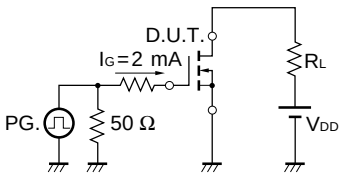
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 40 A		9.7	13	mΩ
	$R_{DS(on)2}$	V_{GS} = 5 V, I_D = 40 A		12	17	mΩ
	$R_{DS(on)3}$	V_{GS} = 4 V, I_D = 40 A		14	20	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 250 μA	1.0	1.5	2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 40 A	15	53		S
Drain Leakage Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz		2360	3540	pF
Output Capacitance	C_{oss}			490	730	pF
Reverse Transfer Capacitance	C_{rss}			220	390	pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 40 A, $V_{GS(on)}$ = 10 V, V_{DD} = 30 V,		66	150	ns
Rise Time	t_r	R_G = 10 Ω		990	2500	ns
Turn-off Delay Time	$t_{d(off)}$			180	400	ns
Fall Time	t_f			450	1200	ns
Total Gate Charge 1	Q_{G1}	I_D = 80 A, V_{DD} = 48 V, V_{GS} = 10 V		60	90	nC
Total Gate Charge 2	Q_{G2}	I_D = 80 A, V_{DD} = 48 V, V_{GS} = 5 V		34	51	nC
Gate to Source Charge	Q_{GS}			10		nC
Gate to Drain Charge	Q_{GD}			20		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 80 A, V_{GS} = 0 V		0.94		V
Reverse Recovery Time	t_{rr}	I_F = 80 A, V_{GS} = 0 V, di/dt = 100 A/μs		55		ns
Reverse Recovery Charge	Q_{rr}			75		nC

TEST CIRCUIT 1 SWITCHING TIME



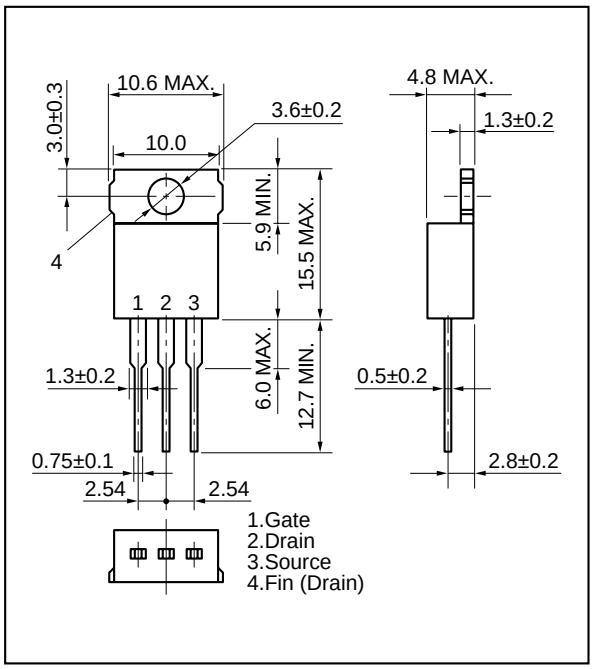
t = 1μs
Duty Cycle ≤ 1 %

TEST CIRCUIT 2 GATE CHARGE

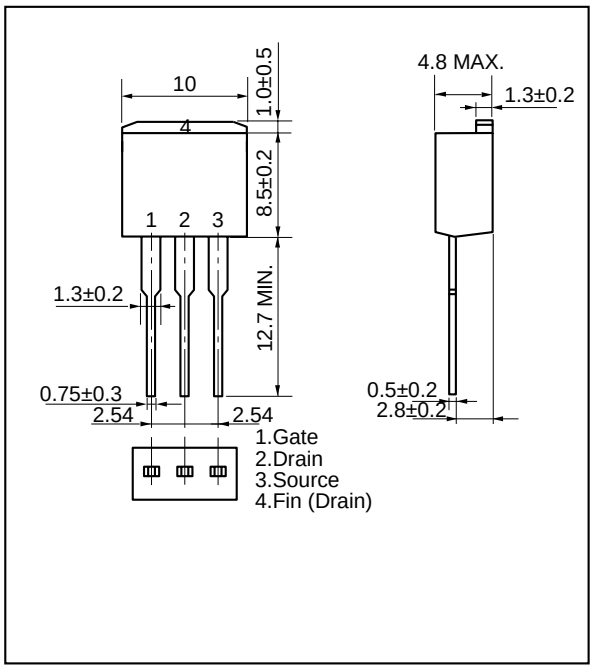


PACKAGE DRAWINGS (Unit : mm)

1. TO-220AB (MP-25)



2. TO-262 (MP-25 Fin Cut)



3. TO-263 (JEDEC type : MP-25ZJ)