

MOS FIELD EFFECT TRANSISTOR NP82N06PDG

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The NP82N06PDG is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP82N06PDG-E1-AY Note	Pure Sn (Tin)	Tape	TO-263 (MP-25ZP)
NP82N06PDG-E2-AY Note		800 p/reel	typ. 1.5 g

Note See "TAPE INFORMATION"

FEATURES

• Super low on-state resistance

 $R_{DS(on)1} = 6.7 \, m\Omega$ MAX. (Vgs = 10 V, ID = 41 A)

 $R_{DS(on)2} = 8.5 \, m\Omega \, MAX. \, (V_{GS} = 5 \, V, \, I_{D} = 41 \, A)$

• Low Ciss

Ciss = 5700 pF TYP.

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V)	VDSS	60	V
Gate to Source Voltage (Vps = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	±82	Α
Drain Current (pulse) Note1	I D(pulse)	±270	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	143	W
Total Power Dissipation ($T_A = 25^{\circ}C$)	P _{T2}	1.8	W
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	-55 to +175	°C
Repetitive Avalanche Current Note2	Iar	37	Α
Repetitive Avalanche Energy Note2	Ear	137	mJ

THERMAL RESISTANCE

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

Channel to Case Thermal Resistance	Rth(ch-C)	1.05	°C/W	
Channel to Ambient Thermal Resistance	Rth(ch-A)	83.3	°C/W	

2. Tch \leq 150°C, VDD = 30 V, RG = 25 Ω , VGS = 20 \rightarrow 0 V

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(TO-263)





ELECTRICAL CHARACTERISTICS (TA = 25°C)

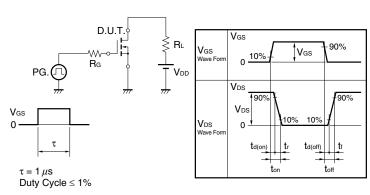
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	Vps = 60 V, Vgs = 0 V			1	μΑ
Gate Leakage Current	Igss	Vgs = ±20 V, Vps = 0 V			±100	nA
Gate to Source Threshold Voltage Note	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 10 V, I _D = 41 A	19	45		S
Drain to Source On-state Resistance Note	RDS(on)1	Ves = 10 V, ID = 41 A		5.1	6.7	mΩ
	RDS(on)2	Vgs = 5 V, ID = 41 A		6.0	8.5	mΩ
Input Capacitance	Ciss	Vps = 25 V		5700		pF
Output Capacitance	Coss	Ves = 0 V		420		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		275		pF
Turn-on Delay Time	td(on)	VDD = 30 V		28		ns
Rise Time	tr	ID = 41 A		22		ns
Turn-off Delay Time	td(off)	Ves = 10 V		79		ns
Fall Time	tf	$R_G = 0 \Omega$		9		ns
Total Gate Charge	Q _G	VDD = 48 V		106		nC
Gate to Source Charge	Q _G s	Ves = 10 V		29		nC
Gate to Drain Charge	Q _{GD}	ID = 82 A		35		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	IF = 82 A, VGS = 0 V		0.9	1.5	V
Reverse Recovery Time	trr	IF = 82 A, VGS = 0 V		43		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		65		nC

Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

$V_{GS} = 20 \rightarrow 0 \text{ V}$ V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD}

TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE

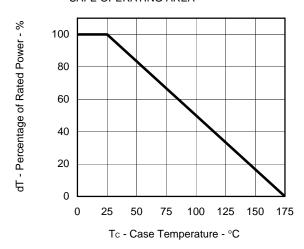
$$\begin{array}{c|c} D.U.T. \\ \hline I_G = 2 \text{ mA} \\ \hline \hline W \\ \hline \end{array}$$

Starting Tch

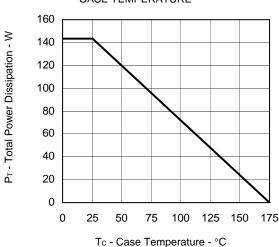


TYPICAL CHARACTERISTICS (TA = 25°C)

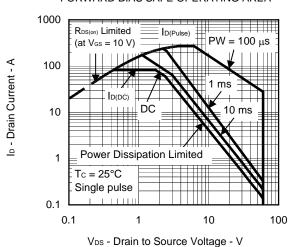
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



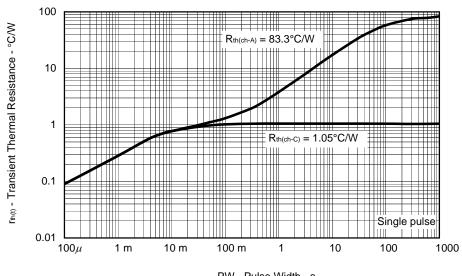
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

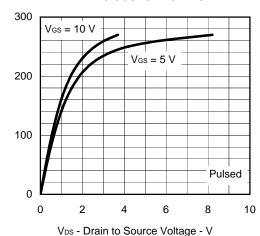


PW - Pulse Width - s

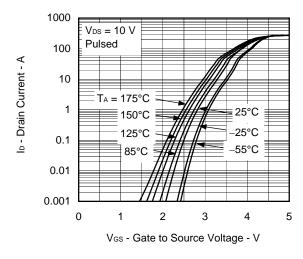
lo - Drain Current - A

V_{GS(th)} - Gate to Source Threshold Voltage - V

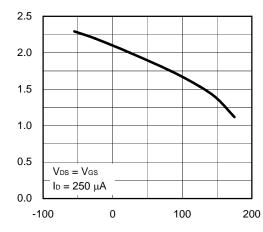
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



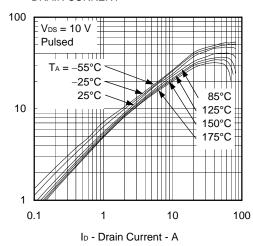
FORWARD TRANSFER CHARACTERISTICS



GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

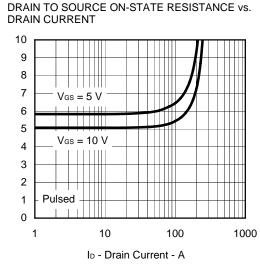


FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

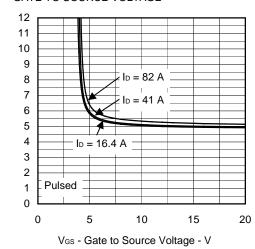


DRAIN TO COURSE ON OTATE REGISTANCE.

Tch - Channel Temperature - °C



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



R_{DS(m)} - Drain to Source On-state Resistance - mΩ

ys | - Forward Transfer Admittance -

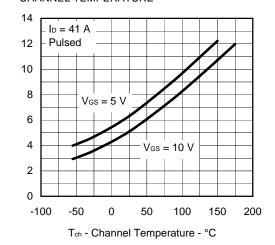
R_{DS(m)} - Drain to Source On-state Resistance - mΩ



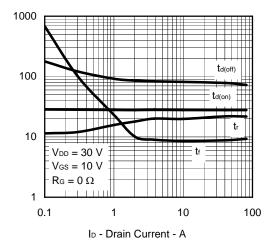
R_{DS(m)} - Drain to Source On-state Resistance - mΩ

ld(on), tr, td(off), tr - Switching Time - ns

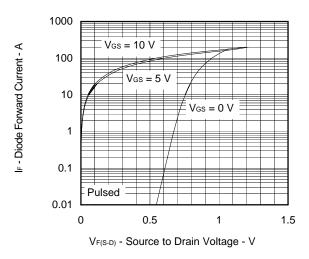
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



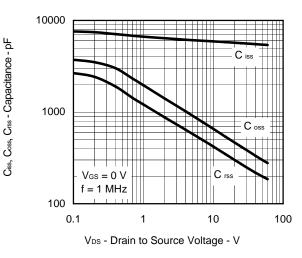
SWITCHING CHARACTERISTICS



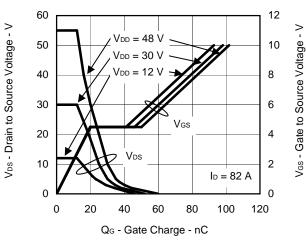
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



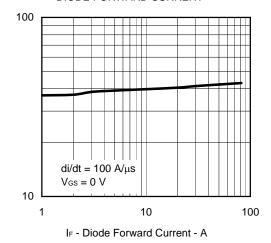
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

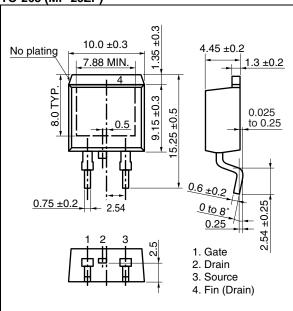


tr - Reverse Recovery Time - ns

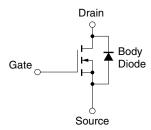


PACKAGE DRAWING (Unit: mm)

TO-263 (MP-25ZP)



EQUIVALENT CIRCUIT



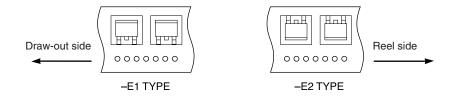
Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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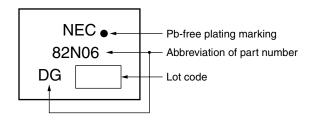


TAPE INFORMATION

There are two types (-E1, -E2) of taping depending on the direction of the device.



MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

The NP82N06PDG should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Maximum temperature (Package's surface temperature): 260°C or below	IR60-00-3
	Time at maximum temperature: 10 seconds or less	
	Time of temperature higher than 220°C: 60 seconds or less	
	Preheating time at 160 to 180°C: 60 to 120 seconds	
	Maximum number of reflow processes: 3 times	
	Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	
Partial heating	Maximum temperature (Pin temperature): 350°C or below	P350
	Time (per side of the device): 3 seconds or less	
	Maximum chlorine content of rosin flux: 0.2% (wt.) or less	

Caution Do not use different soldering methods together (except for partial heating).

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