# DATA SHEET



# MOS FIELD EFFECT TRANSISTOR NP82P04PLF

# SWITCHING **P-CHANNEL POWER MOSFET**

#### **DESCRIPTION**

The NP82P04PLF is P-channel MOS Field Effect Transistor designed for high current switching applications.

#### ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP82P04PLF-E1-AY Note	Duna Ca (Tia)	T 000 m/ml	TO 202 (MD 257D)
NP82P04PLF-E2-AY Note	Pure Sn (Tin)	Tape 800 p/reel	TO-263 (MP-25ZP)

Note Pb-free (This product does not contain Pb in external electrode.)

#### **FEATURES**

• Super low on-state resistance

 $R_{DS(on)1} = 8 \text{ m}\Omega \text{ MAX.} (V_{GS} = -10 \text{ V}, I_D = -41 \text{ A})$ 

 $R_{DS(on)2} = 12 \text{ m}\Omega \text{ MAX.} (V_{GS} = -4.5 \text{ V}, I_{D} = -41 \text{ A})$ 

· Low input capacitance

Ciss = 5000 pF TYP.

• Built-in gate protection diode

# (TO-263)



# ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V)	Voss	-40	V
Gate to Source Voltage (VDS = 0 V)	Vgss	∓20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	∓82	Α
Drain Current (pulse) Note1	D(pulse)	∓246	Α
Total Power Dissipation (Tc = 25°C)	P <sub>T1</sub>	150	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.8	W
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	-55 to +175	°C
Repetitive Avalanche Current Note2	Iar	46	Α
Repetitive Avalanche Energy Note2	Ear	212	mJ

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

**2.** Tch  $\leq$  150°C, VDD = -20 V, Rg = 25  $\Omega$ , Vgs = -20  $\rightarrow$  0 V

#### THERMAL RESISTANCE

Channel to Case Thermal Resistance	Rth(ch-C)	1.0	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	83.3	°C/W

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# **ELECTRICAL CHARACTERISTICS (TA = 25°C)**

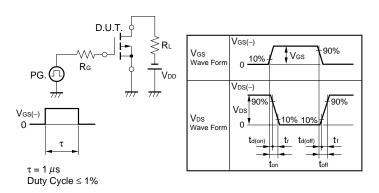
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	Ioss	V <sub>DS</sub> = -40 V, V <sub>GS</sub> = 0 V			-10	μΑ
Gate Leakage Current	Igss	V <sub>GS</sub> = ∓20 V, V <sub>DS</sub> = 0 V			∓10	μΑ
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	-1.5	-2.0	-2.5	V
Forward Transfer Admittance Note	<b>y</b> fs	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -41 A	28	58		S
Drain to Source On-state Resistance Note	RDS(on)1	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -41 A		6.5	8	mΩ
	RDS(on)2	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -41 A		8.3	12	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = -10 V,		5000		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V,		1100		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		440		pF
Turn-on Delay Time	t <sub>d(on)</sub>	$V_{DD} = -20 \text{ V}, I_D = -41 \text{ A},$		17		ns
Rise Time	tr	V <sub>GS</sub> = -10 V,		18		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 0 Ω		126		ns
Fall Time	<b>t</b> f			58		ns
Total Gate Charge	Q <sub>G</sub>	$V_{DD} = -32 \text{ V},$		90		nC
Gate to Source Charge	Qgs	V <sub>GS</sub> = -10 V,		15		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = -82 A		21		nC
Body Diode Forward Voltage Note	V <sub>F(S-D)</sub>	I <sub>F</sub> = -82 A, V <sub>GS</sub> = 0 V		0.96	1.5	V
Reverse Recovery Time	trr	IF = -82 A, VGS = 0 V,		48		ns
Reverse Recovery Charge	Qrr	di/dt = –100 A/μs		62		nC

**Note** Pulsed test PW  $\leq$  350  $\mu$ s, Duty Cycle  $\leq$  2%

#### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

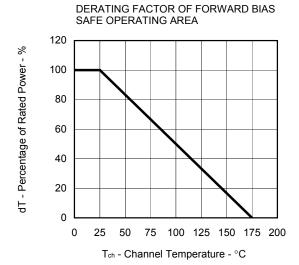
# $V_{GS} = -20 \rightarrow 0 \text{ V}$ $V_{DD}$ $V_{DD}$

## TEST CIRCUIT 2 SWITCHING TIME



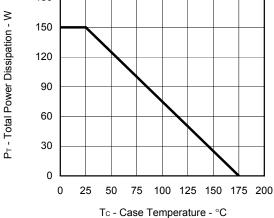
#### **TEST CIRCUIT 3 GATE CHARGE**

# TYPICAL CHARACTERISTICS (TA = 25°C)

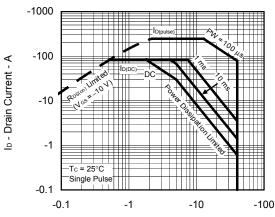


# CASE TEMPERATURE 180 150

TOTAL POWER DISSIPATION vs.

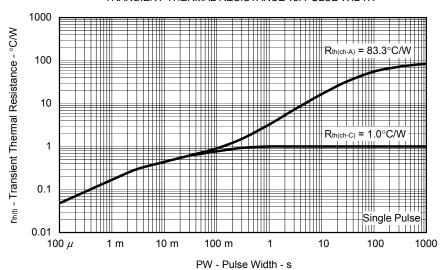


#### FORWARD BIAS SAFE OPERATING AREA

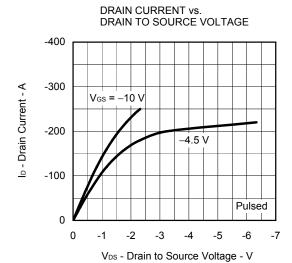


#### V<sub>DS</sub> - Drain to Source Voltage - V

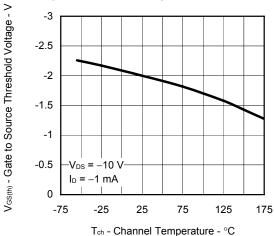
#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



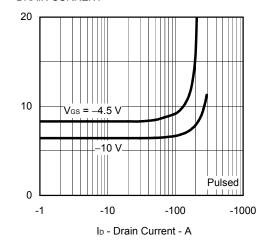
3



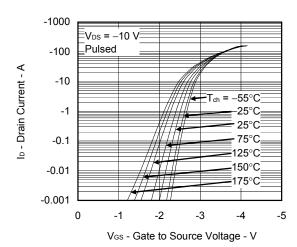




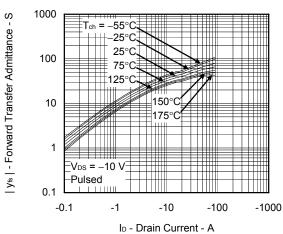
# DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



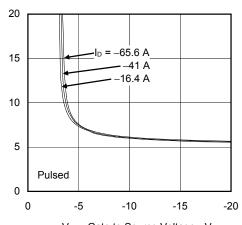
#### FORWARD TRANSFER CHARACTERISTICS



# FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



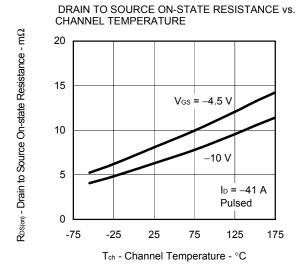
# DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

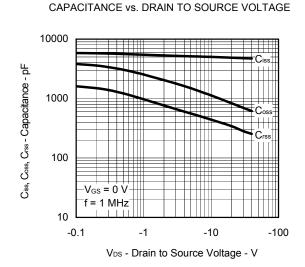


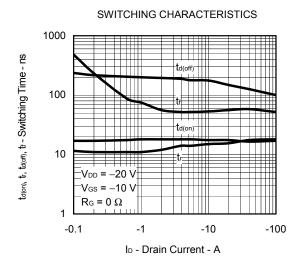
V<sub>GS</sub> - Gate to Source Voltage - V

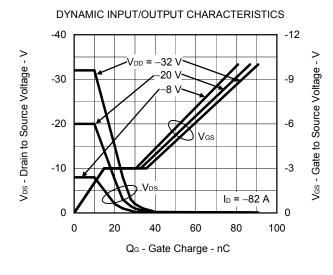
R<sub>DS(o1)</sub> - Drain to Source On-state Resistance - mΩ

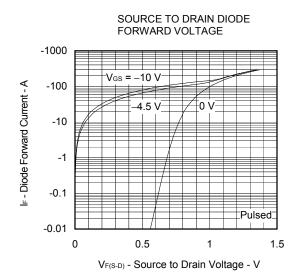
RDS(on) - Drain to Source On-state Resistance - mΩ

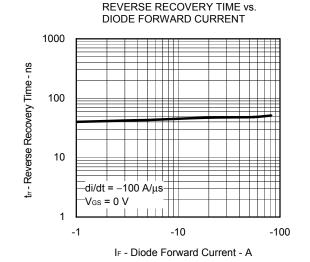






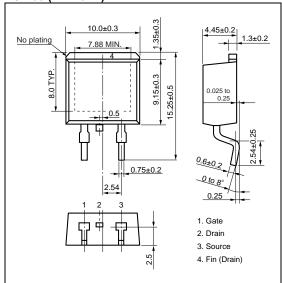




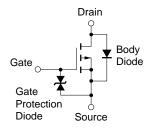


# PACKAGE DRAWING (Unit: mm)

## TO-263 (MP-25ZP)



## **EQUIVALENT CIRCUIT**



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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NP82P04PLF

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