

NP89N04PDK

Data Sheet

R07DS1016EJ0200 Rev.2.00 May 24, 2018

# Description

The NP89N04PDK is N-channel MOS Field Effect Transistors designed for high current switching applications.

## Features

• Super low on-state resistance

 $R_{DS(on)} = 2.95 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, I_D = 45 \text{ A})$ 

- Low  $C_{iss}$ :  $C_{iss} = 3900 \text{ pF TYP}$ . ( $V_{DS} = 25 \text{ V}$ )
- Logic level drive type
- Designed for automotive application and AEC-Q101 qualified

### **Ordering Information**

Part No.	Lead Plating	Pac	Package	
NP89N04PDK-E1-AY *1	Pure Sn (Tin)	Tape 800 p/reel	Taping (E1 type)	TO-263 (MP-25ZP)
NP89N04PDK-E2-AY *1			Taping (E2 type)	

Note: \*1 Pb-free (This product does not contain Pb in the external electrode)

## **Absolute Maximum Ratings** ( $T_A = 25^{\circ}C$ )

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V <sub>GS</sub> = 0 V)	VDSS	40	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	Vgss	±20	V
Drain Current (DC) (T <sub>C</sub> = 25°C)	ID(DC)	±90	A
Drain Current (pulse) *1, 3	I <sub>D(pulse)</sub>	±360	A
Total Power Dissipation (T <sub>c</sub> = 25°C)	P <sub>T1</sub>	147	W
Total Power Dissipation ( $T_A = 25^{\circ}C$ )	P <sub>T2</sub>	1.8	W
Channel Temperature	T <sub>ch</sub>	175	°C
Storage Temperature	T <sub>stg</sub>	–55 to +175	°C
Repetitive Avalanche Current *2, 3	lar	37	A
Repetitive Avalanche Energy *2, 3	E <sub>AR</sub>	136	mJ

### **Thermal Resistance**

Channel to Case Thermal Resistance	Rth(ch-C)*3	1.02	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A) *3	83.3	°C/W

Notes: \*1 T\_C = 25°C, P\_W  $\leq$  10  $\mu s,$  Duty Cycle  $\leq$  1%

- \*2 R<sub>G</sub> = 25  $\Omega,$  V<sub>GS</sub> = 20 V  $\rightarrow$  0 V
- \*3. Not subject of production test. Verified by design/characterization.



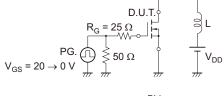
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			1	μA	$V_{DS}$ = 40 V, $V_{GS}$ = 0 V	
Gate Leakage Current	I <sub>GSS</sub>			±100	nA	$V_{GS}$ = ±20 V, $V_{DS}$ = 0 V	
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	1.5	1.8	2.5	V	$V_{DS}$ = $V_{GS}$ , $I_D$ = 250 $\mu$ A	
Forward Transfer Admittance *1	y <sub>fs</sub>	44	88	_	S	$V_{DS}$ = 5 V, $I_{D}$ = 45 A	
Drain to Source On-state Resistance *1	R <sub>DS(on)1</sub>	_	2.45	2.95	mΩ	$V_{GS}$ = 10 V, $I_{D}$ = 45 A	
	R <sub>DS(on)2</sub>	_	3.10	6.20	mΩ	$V_{GS}$ = 4.5 V, I <sub>D</sub> = 23 A	
Input Capacitance *2	Ciss	_	3900	5850	pF	V <sub>DS</sub> = 25 V	
Output Capacitance *2	Coss		530	800	pF	V <sub>GS</sub> = 0 V	
Reverse Transfer Capacitance *2	Crss		200	360	pF	f = 1 MHz	
Turn-on Delay Time *2	t <sub>d(on)</sub>		18	40	ns	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 45 A	
Rise Time *2	tr		8	21	ns	V <sub>GS</sub> = 10 V	
Turn-off Delay Time *2	t <sub>d(off)</sub>		71	142	ns	$R_G = 0 \Omega$	
Fall Time *2	t <sub>f</sub>	_	9	23	ns		
Total Gate Charge *2	Q <sub>G</sub>	_	68	102	nC	V <sub>DD</sub> = 32 V	
Gate to Source Charge	Q <sub>GS</sub>	_	17	_	nC	V <sub>GS</sub> = 10 V	
Gate to Drain Charge	Q <sub>GD</sub>		11	_	nC	I <sub>D</sub> = 90 A	
Body Diode Forward Voltage *1	V <sub>F(S-D)</sub>		0.9	1.5	V	I <sub>F</sub> = 90 A, V <sub>GS</sub> = 0 V	
Reverse Recovery Time	t <sub>rr</sub>		43	_	ns	I <sub>F</sub> = 90 A, V <sub>GS</sub> = 0 V	
Reverse Recovery Charge	Qrr	_	59	_	nC	di/dt = 100 A/µs	

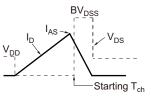
Note: \*1 Pulsed test

Note: \*2 Not subject of production test. Verified by design/characterization.

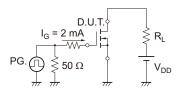
### TEST CIRCUIT 1 AVALANCHE CAPABILITY

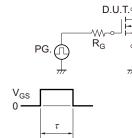
### TEST CIRCUIT 2 SWITCHING TIME



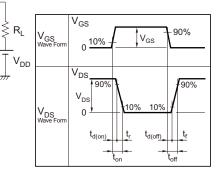


### TEST CIRCUIT 3 GATE CHARGE



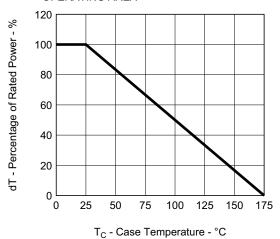


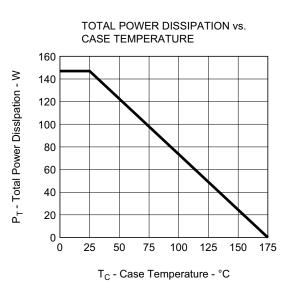




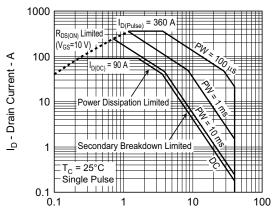
# **Typical Characteristics** (T<sub>A</sub> = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



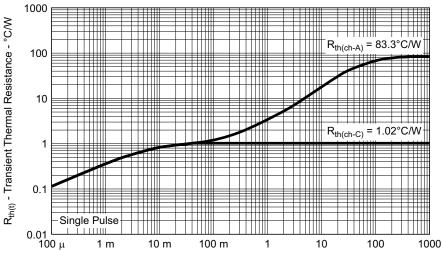


FORWARD BIAS SAFE OPERATING AREA



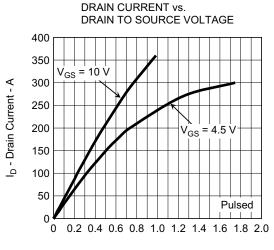


#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

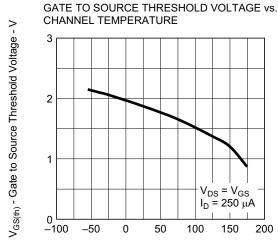


PW - Pulse Width - s

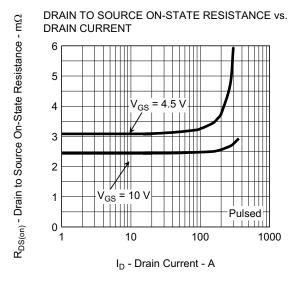




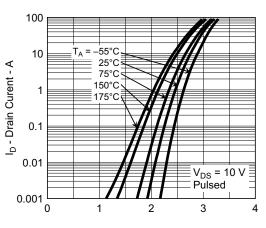
V<sub>DS</sub> - Drain to Source Voltage - V



T<sub>ch</sub> - Channel Temperature - °C

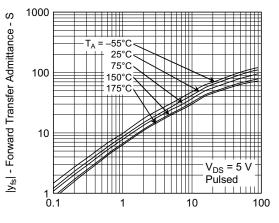


FORWARD TRANSFER CHARACTERISTICS

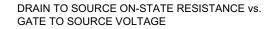


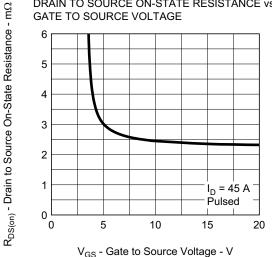


FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



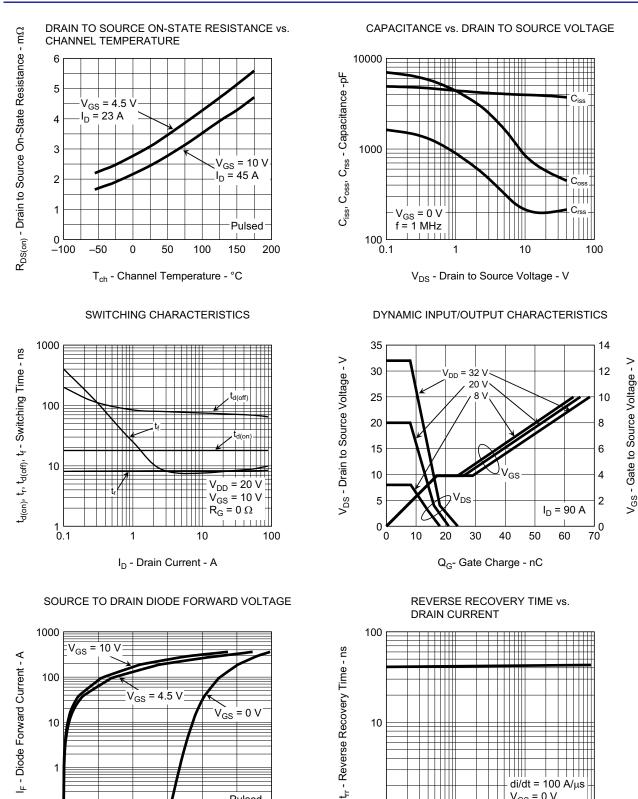
I<sub>D</sub> - Drain Current - A







#### NP89N04PDK



1

0.1

0

0.2

0.4

0.6

 $V_{F(S-D)}$  - Source to Drain Voltage - V

0.8



Pulsed

1.2

1.0

1

1 └ 0.1

HH

111

IF - Drain Current - A

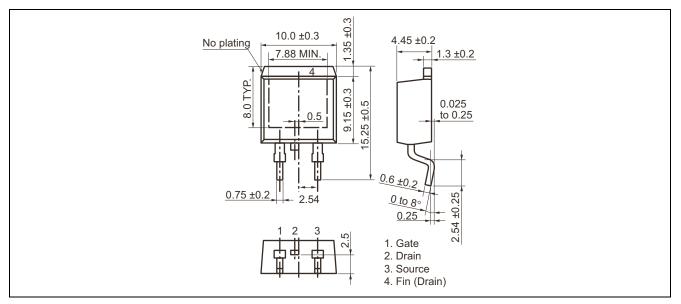
10

di/dt = 100 A/µs  $V_{GS}$  = 0 V

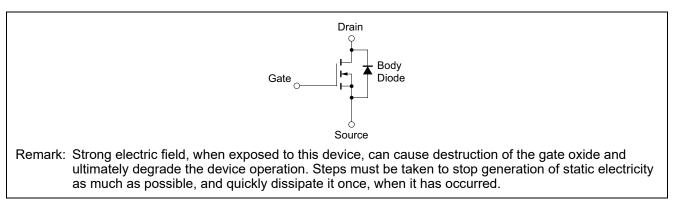
100

# Package Drawing (Unit: mm)

# TO-263 (MP-25ZP) (Mass: 1.48 g TYP.)



### **Equivalent Circuit**





<b>Revision H</b>	istory
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## NP89N04PDK Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Feb 21, 2013	—	First Edition Issued	
2.00	May 24 ,2018	1	Note 3 was added	
		2	Note 2 was added	

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