

NP90N03VLG

R07DS0129EJ0100

Rev.1.00

Sep 24, 2010

MOS FIELD EFFECT TRANSISTOR

Description

The NP90N03VLG is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Low on-state resistance
 - $R_{DS(on)1} = 3.2 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 10 \text{ V}$, $I_D = 45 \text{ A}$)
 - $R_{DS(on)2} = 8.0 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 4.5 \text{ V}$, $I_D = 35 \text{ A}$)
- Low input capacitance
 - $C_{iss} = 5000 \text{ pF TYP.}$ ($V_{DS} = 25 \text{ V}$, $V_{GS} = 0 \text{ V}$)
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
NP90N03VLG-E1-AY*1	Pure Sn (Tin)	Tape 2500 p/reel	TO-252, Taping (E1 type)
NP90N03VLG-E2-AY*1			TO-252, Taping (E2 type)

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 90	A
Drain Current (pulse) *1	$I_{D(pulse)}$	± 360	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	105	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +175	$^\circ\text{C}$
Repetitive Avalanche Current *2	I_{AR}	41	A
Repetitive Avalanche Energy *2	E_{AR}	168	mJ

Notes: *1. $T_C = 25^\circ\text{C}$, $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

*2. $T_{ch(peak)} \leq 150^\circ\text{C}$, $R_G = 25 \Omega$

Thermal Resistance

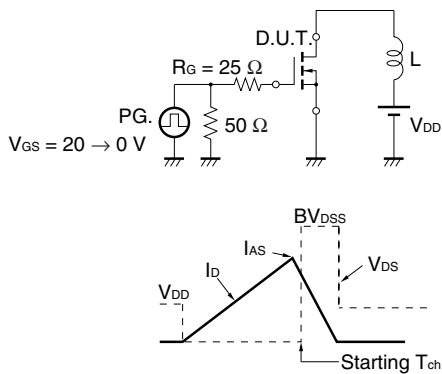
Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.43	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	125	$^\circ\text{C/W}$

Electrical Characteristics (T_A = 25°C)

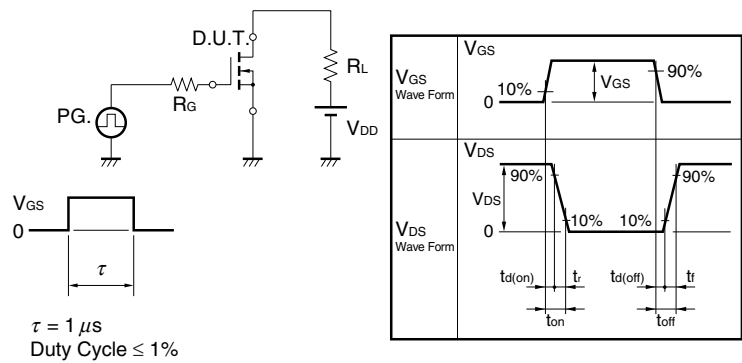
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μA	V _{DS} = 30 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0 V
Gate to Source Threshold Voltage	V _{GS(th)}	1.4	1.8	2.5	V	V _{DS} = V _{GS} , I _D = 250 μA
Forward Transfer Admittance *1	y _{fs}	30	67		S	V _{DS} = 5 V, I _D = 45 A
	R _{DS(on)1}		2.5	3.2	mΩ	V _{GS} = 10 V, I _D = 45 A
Drain to Source On-state Resistance *1	R _{DS(on)2}		3.8	8.0	mΩ	V _{GS} = 4.5 V, I _D = 35 A
	C _{iss}		5000	7500	pF	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz
Output Capacitance	C _{oss}		600	900	pF	
Reverse Transfer Capacitance	C _{rss}		420	760	pF	
Turn-on Delay Time	t _{d(on)}		17	34	ns	V _{DD} = 15 V, I _D = 45 A, V _{GS} = 10 V, R _G = 0 Ω
Rise Time	t _r		13	33	ns	
Turn-off Delay Time	t _{d(off)}		73	146	ns	
Fall Time	t _f		9	23	ns	
Total Gate Charge	Q _G		90	135	nC	V _{DD} = 24 V, V _{GS} = 10 V, I _D = 90 A
Gate to Source Charge	Q _{GS}		13		nC	
Gate to Drain Charge	Q _{GD}		26		nC	
Body Diode Forward Voltage *1	V _{F(S-D)}		0.9	1.5	V	I _F = 90 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		42		ns	I _F = 90 A, V _{GS} = 0 V, di/dt = 100 A/μs
Reverse Recovery Charge	Q _{rr}		35		nC	

Note: *1. Pulsed

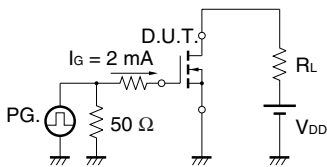
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

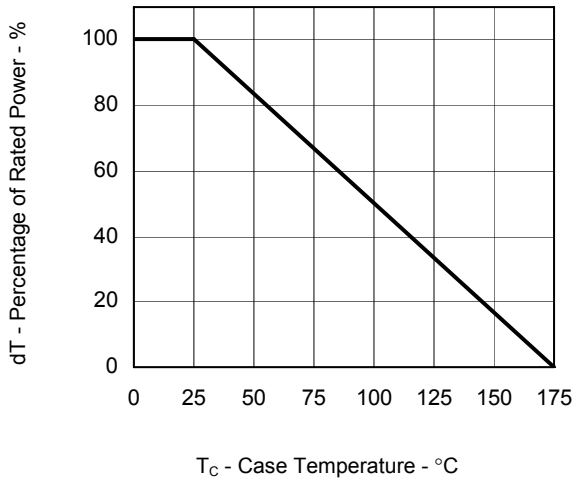


TEST CIRCUIT 3 GATE CHARGE

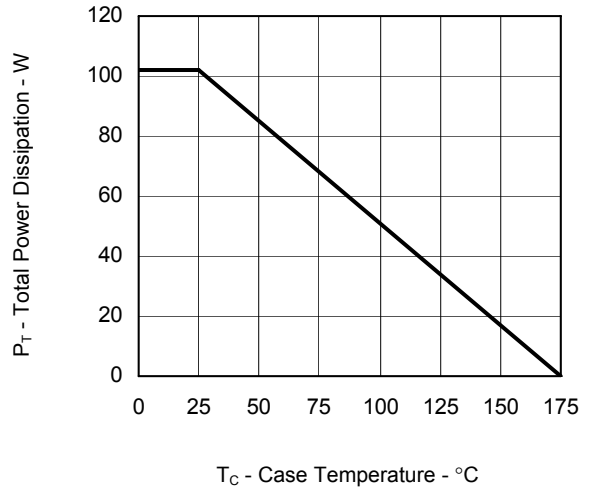


Typical Characteristics ($T_A = 25^\circ\text{C}$)

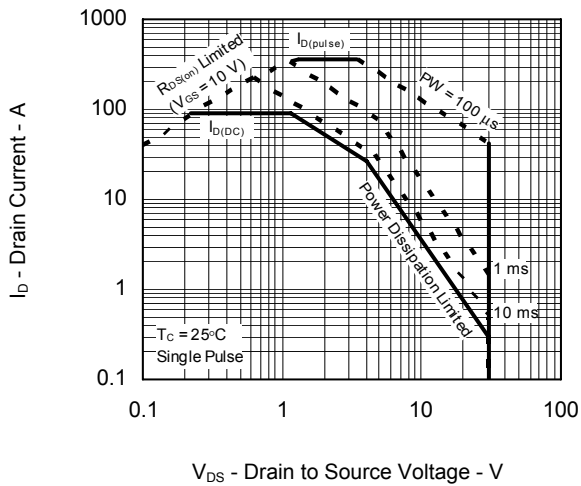
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



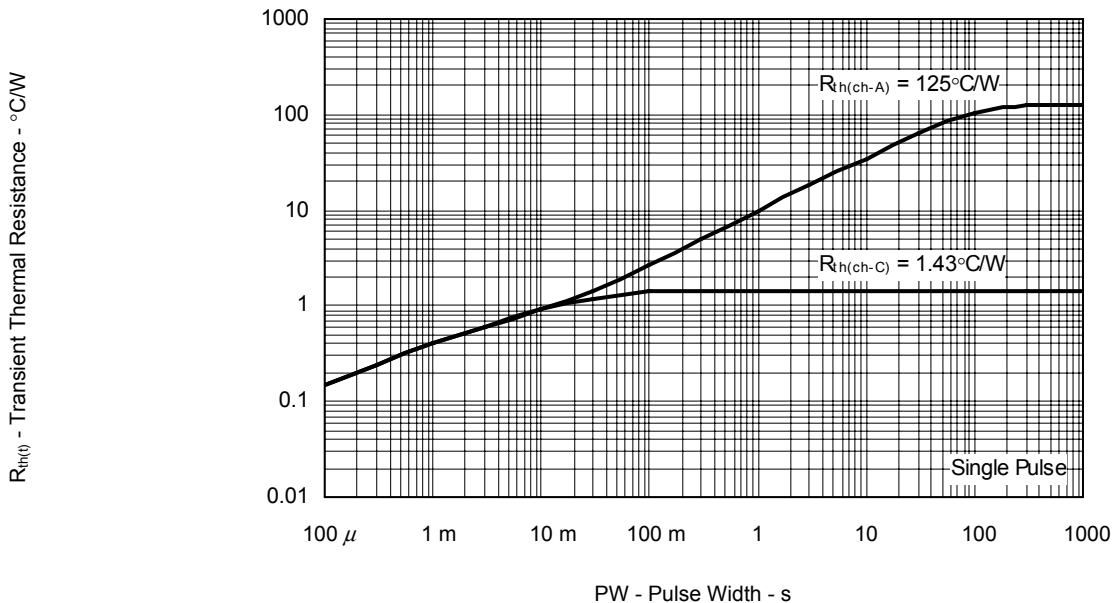
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



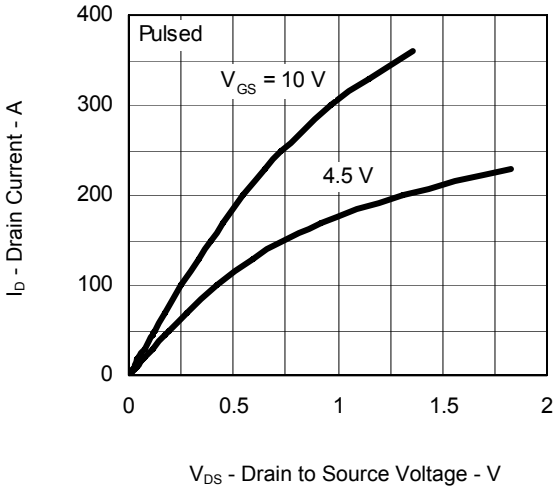
FORWARD BIAS SAFE OPERATING AREA



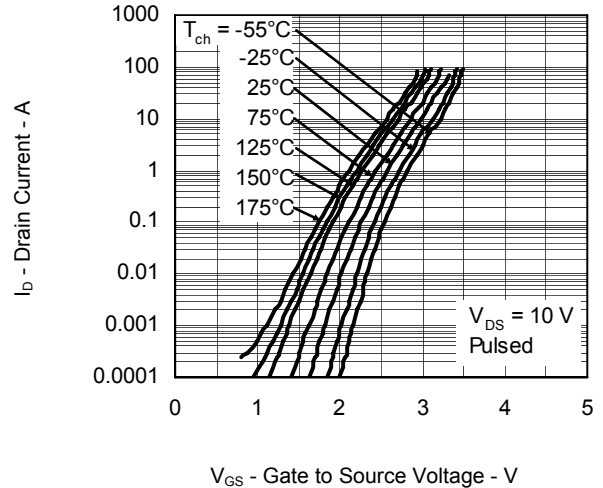
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



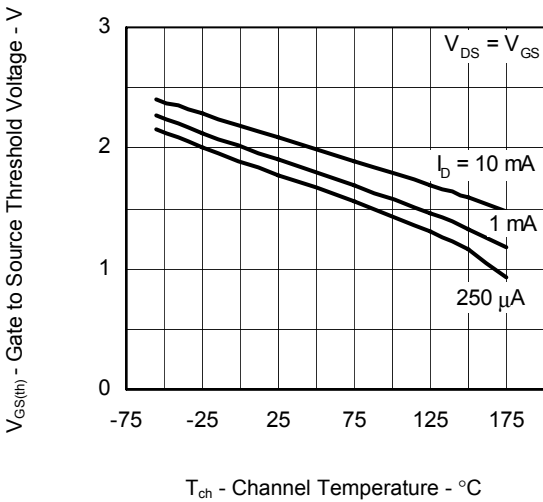
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



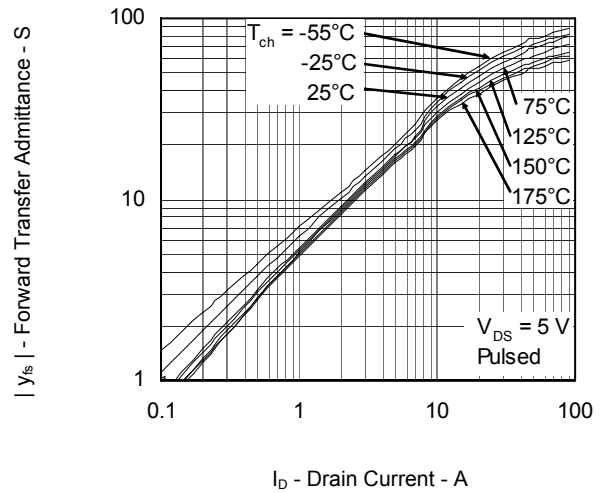
FORWARD TRANSFER CHARACTERISTICS



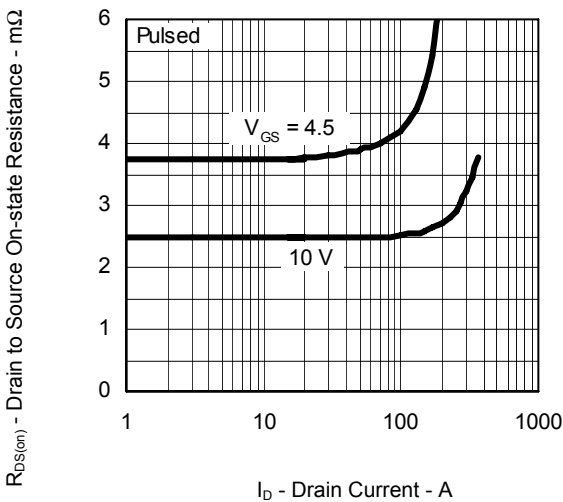
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



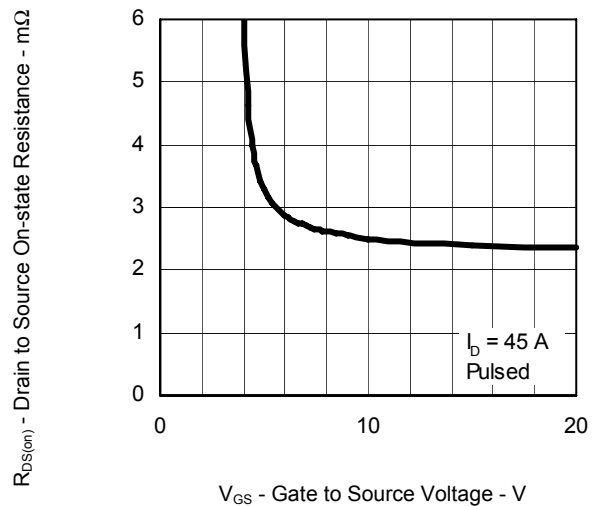
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



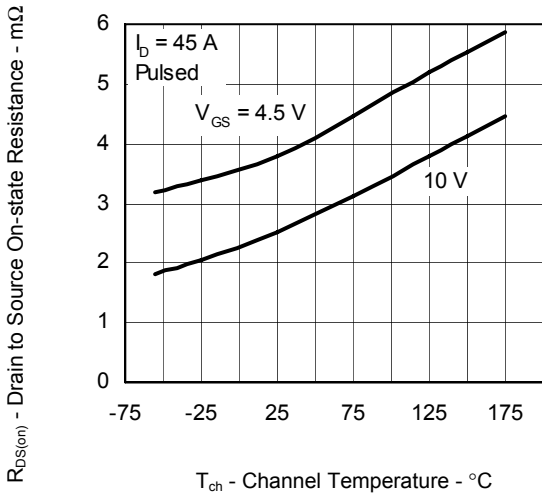
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



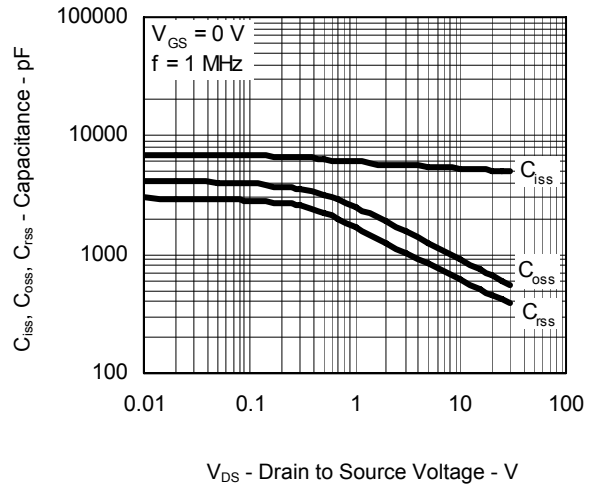
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



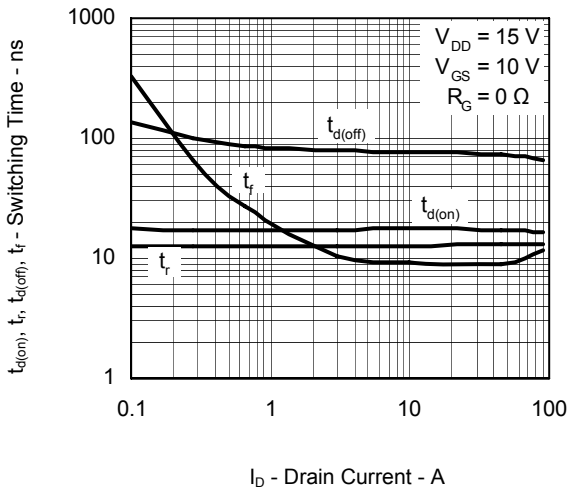
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



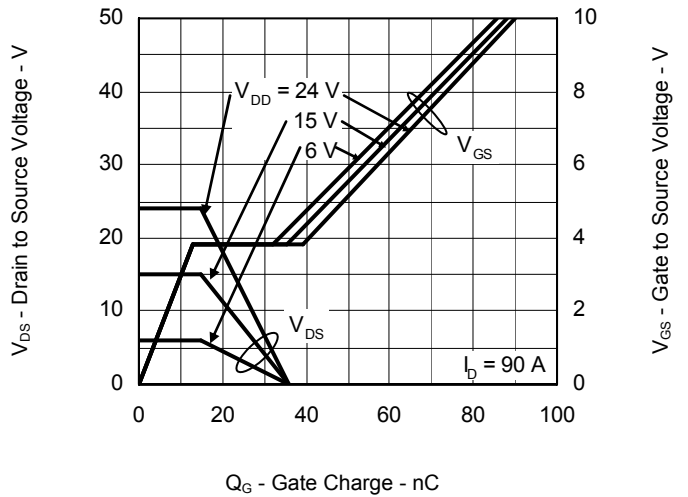
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



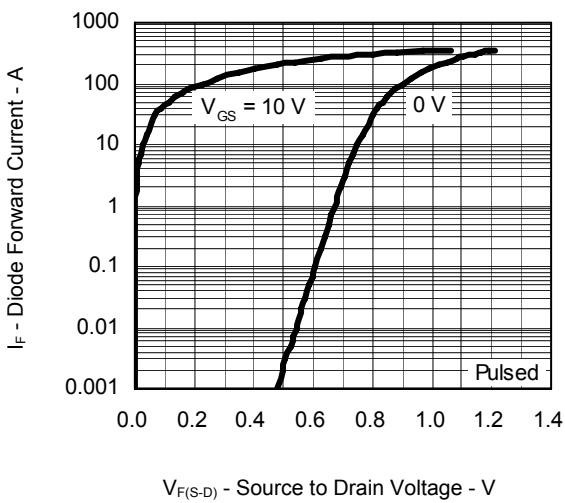
SWITCHING CHARACTERISTICS



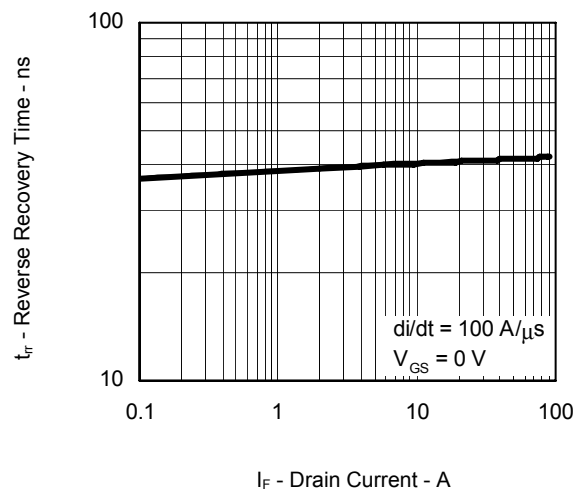
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

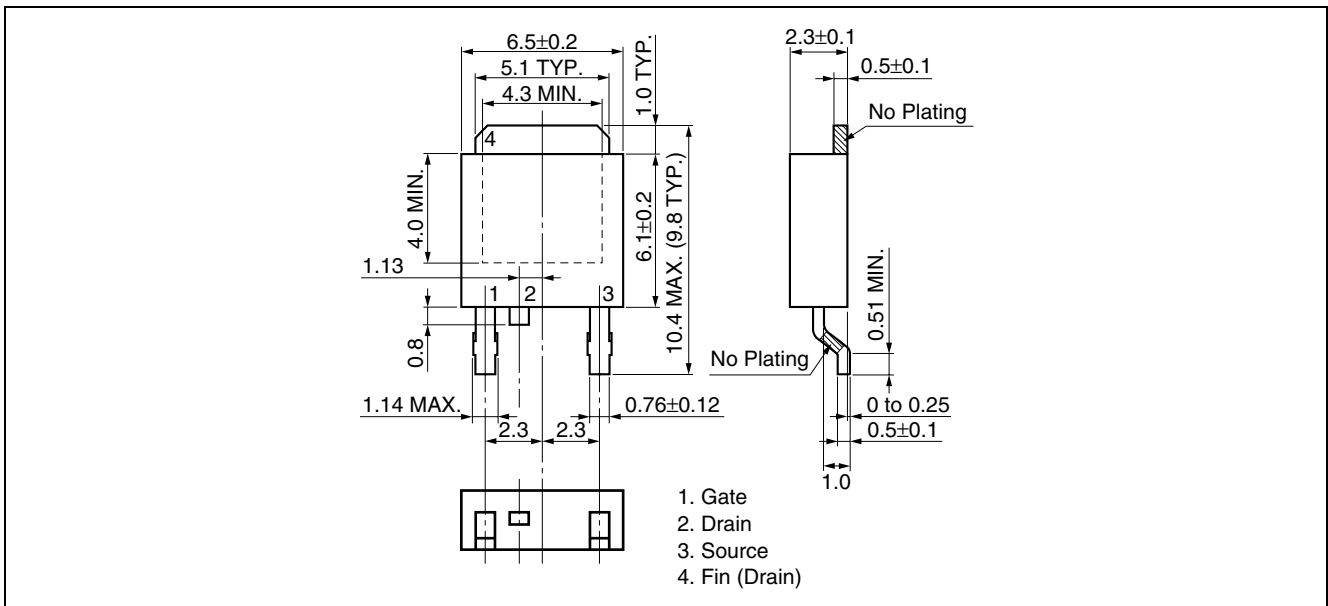


REVERSE RECOVERY TIME vs. DRAIN CURRENT

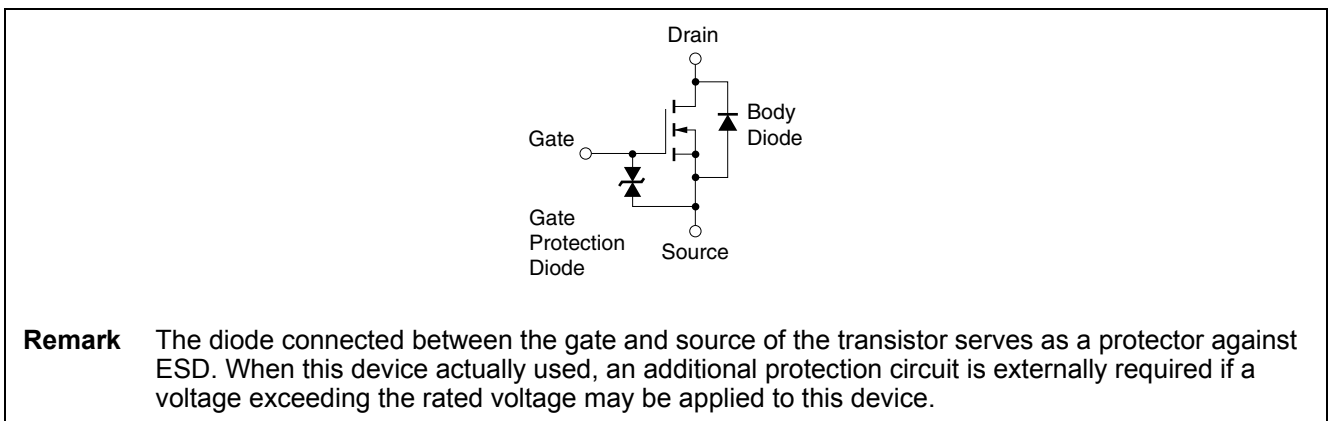


Package Drawings (Unit: mm)

TO-252 (MP-3ZP) (Mass: 0.27 g TYP.)



Equivalent Circuit



Revision History	NP90N03VLG
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Rev.	Date	Description	
		Page	Summary
1.00	Sep 24, 2010	-	First Edition Issued

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