NP90N055VUK

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Rev.2.00
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MOS FIELD EFFECT TRANSISTOR

Description

The NP90N055VUK is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Super low on-state resistance
  $R_{DS(on)}$ = 3.85 mΩ MAX. (V_{GS} = 10 V, I_D = 45 A)
- Low C_{iss}: C_{iss} = 4000 pF TYP. (V_{DS} = 25 V)
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Packing		Package
NP90N055VUK-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	TO-252 (MP-3ZP)
NP90N055VUK-E2-AY *1			Taping (E2 type)	

Note: *1 Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	55	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±90	A
Drain Current (pulse) *1, 3	$I_{D(pulse)}$	±360	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	147	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to 175	°C
Repetitive Avalanche Current *2, 3	I_{AR}	33	A
Repetitive Avalanche Energy *2, 3	E_{AR}	108	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$*3	1.02	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$ *3	125	°C/W

Notes: *1 T_C = 25°C, $P_W \leq 10$ μs, Duty Cycle ≤ 1%
*2 R_G = 25 Ω, V_{GS} = 20 → 0 V
*3 Not subject of production test. Verified by design/characterization.

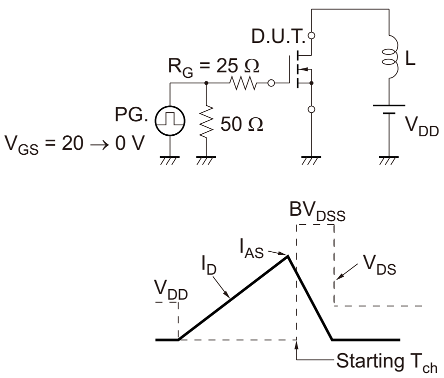
Electrical Characteristics (T_A = 25°C)

Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	V_{DS} = 55 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	±100	nA	V_{GS} = ±20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Forward Transfer Admittance *1	| y_{fs} |	30	60	—	S	V_{DS} = 5 V, I_D = 45 A
Drain to Source On-state Resistance *1	$R_{DS(on)}$	—	3.20	3.85	mΩ	V_{GS} = 10 V, I_D = 45 A
Input Capacitance *2	C_{iss}	—	4000	6000	pF	V_{DS} = 25 V V_{GS} = 0 V f = 1 MHz
Output Capacitance *2	C_{oss}	—	410	620	pF	
Reverse Transfer Capacitance *2	C_{rss}	—	150	270	pF	
Turn-on Delay Time *2	$t_{d(on)}$	—	25	60	ns	V_{DD} = 28 V, I_D = 45 A V_{GS} = 10 V R_G = 0 Ω
Rise Time *2	t_r	—	10	30	ns	
Turn-off Delay Time *2	$t_{d(off)}$	—	65	130	ns	
Fall Time *2	t_f	—	6	20	ns	
Total Gate Charge *2	Q_G	—	68	102	nC	V_{DD} = 44 V V_{GS} = 10 V I_D = 90 A
Gate to Source Charge	Q_{GS}	—	18	—	nC	
Gate to Drain Charge	Q_{GD}	—	18	—	nC	
Body Diode Forward Voltage *1	$V_{F(S-D)}$	—	0.9	1.5	V	I_F = 90 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	—	47	—	ns	I_F = 90 A, V_{GS} = 0 V di/dt = 100 A/μs
Reverse Recovery Charge	Q_{rr}	—	80	—	nC	

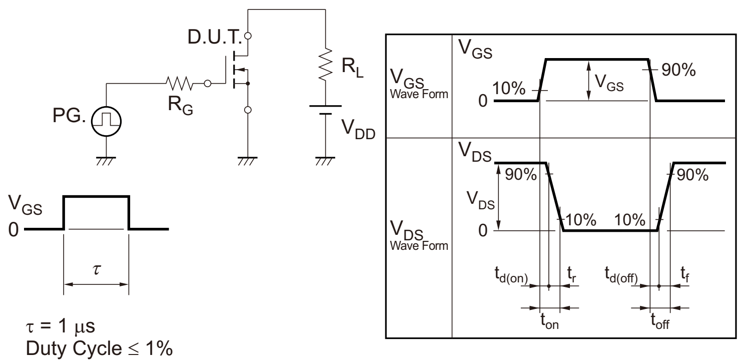
Note: *1 Pulsed test

Note: *2 Not subject of production test. Verified by design/characterization.

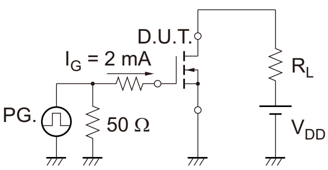
TEST CIRCUIT 1 AVALANCHE CAPABILITY



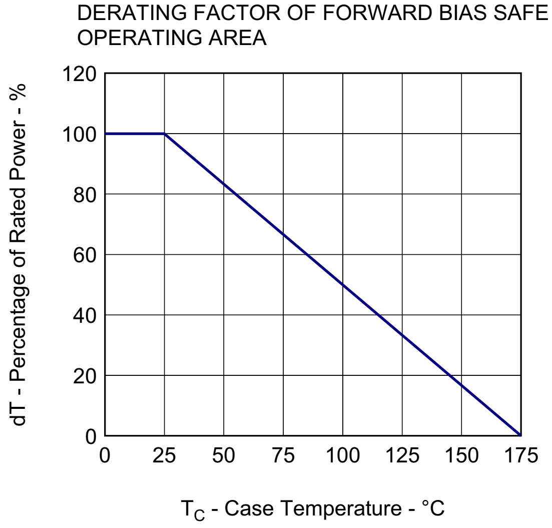
TEST CIRCUIT 2 SWITCHING TIME

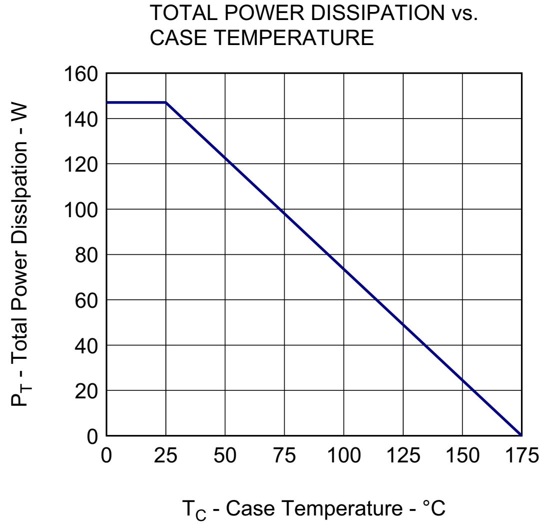


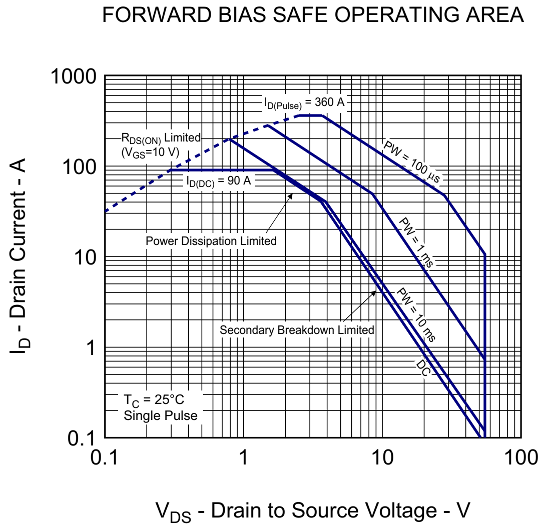
TEST CIRCUIT 3 GATE CHARGE

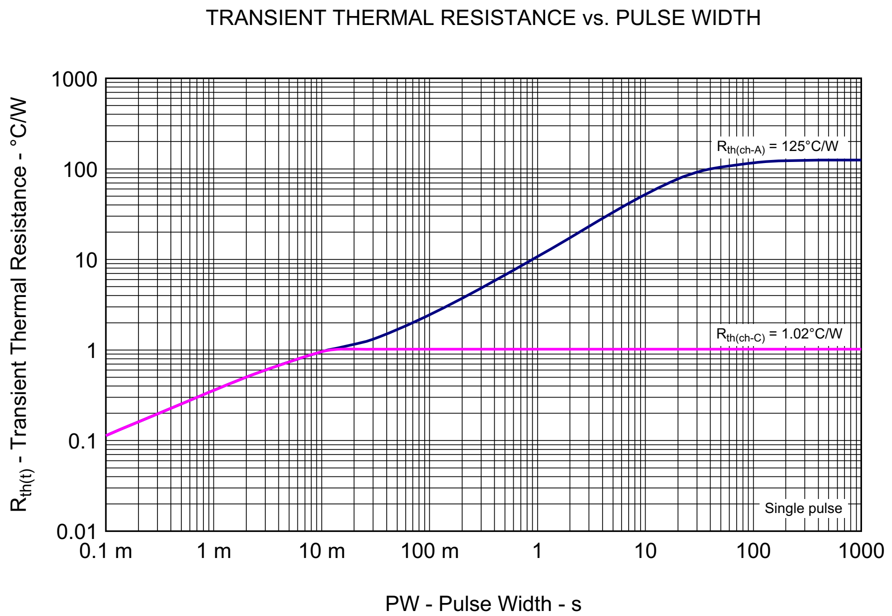


Typical Characteristics (T_A = 25°C)

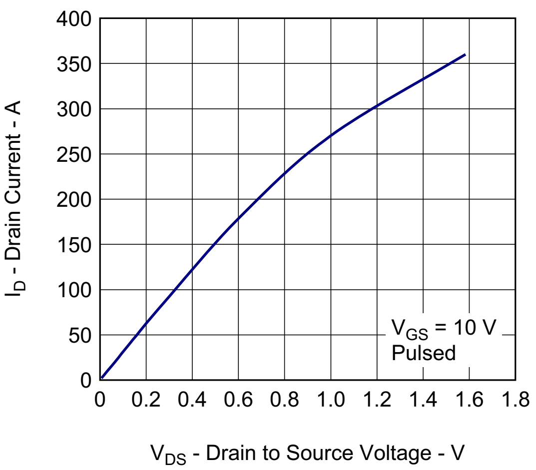




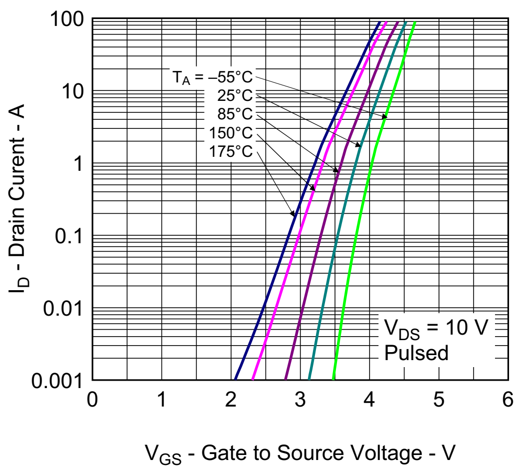




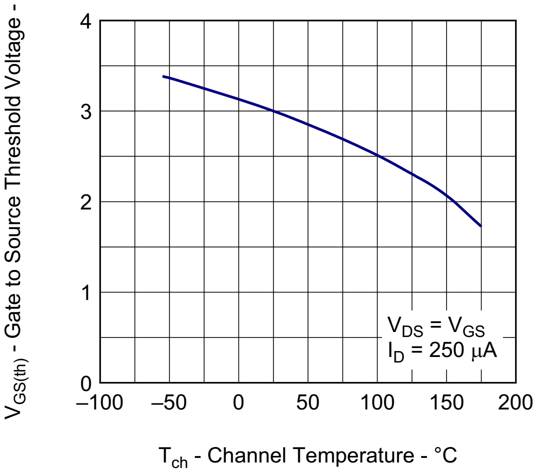
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



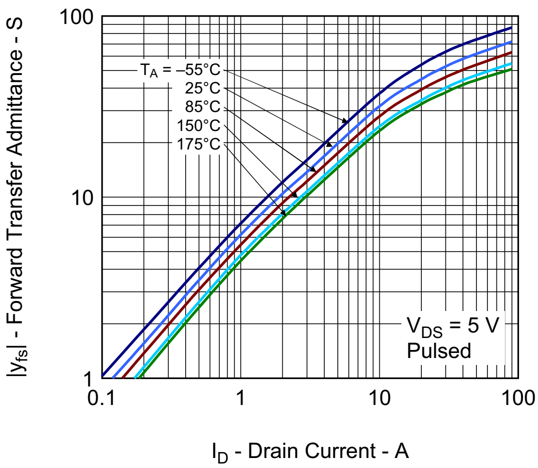
FORWARD TRANSFER CHARACTERISTICS



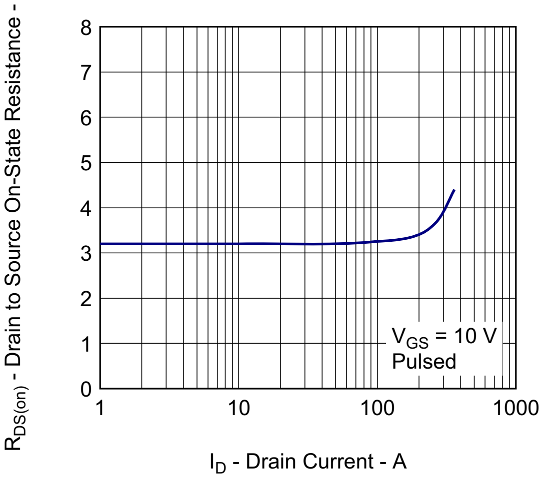
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



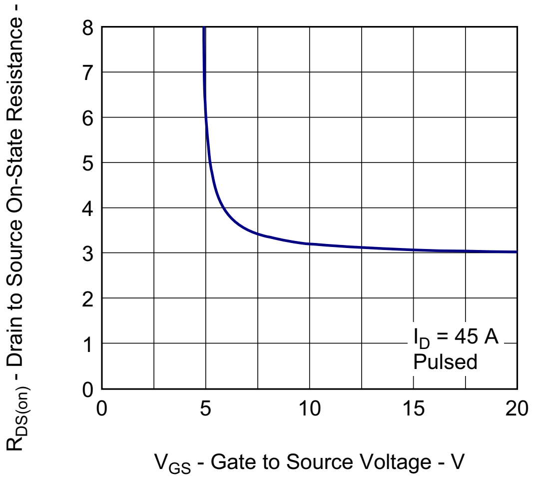
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



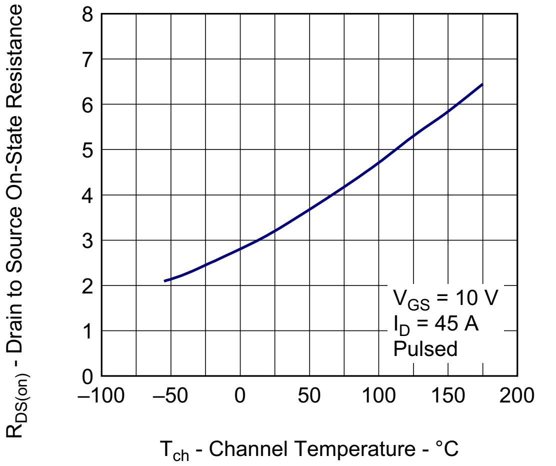
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



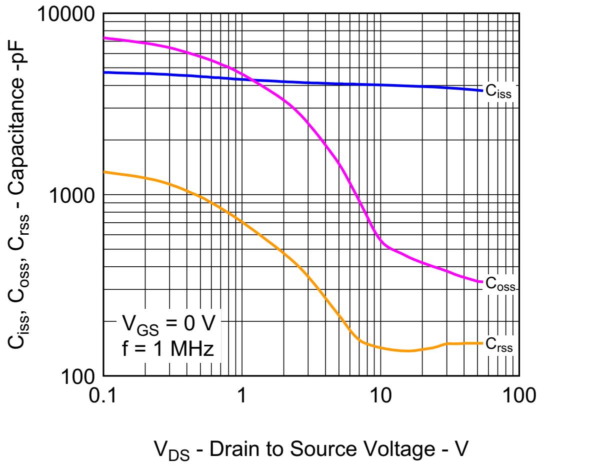
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



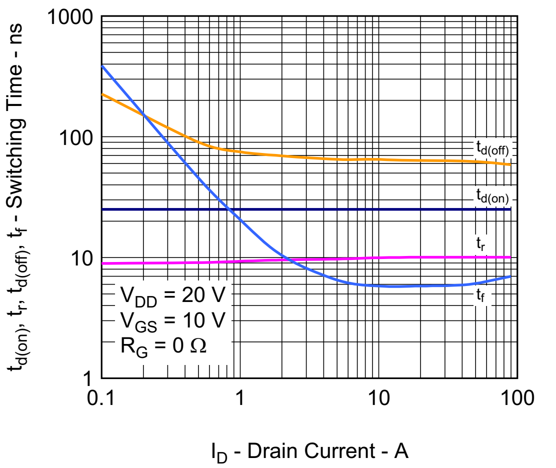
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



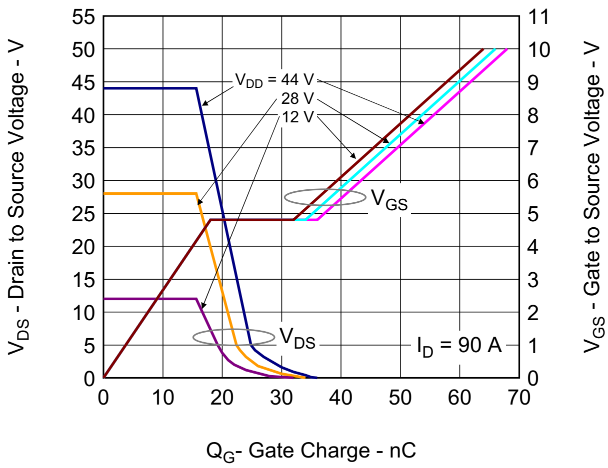
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



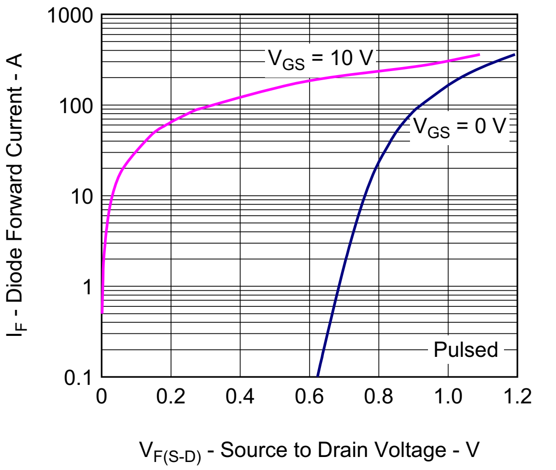
SWITCHING CHARACTERISTICS



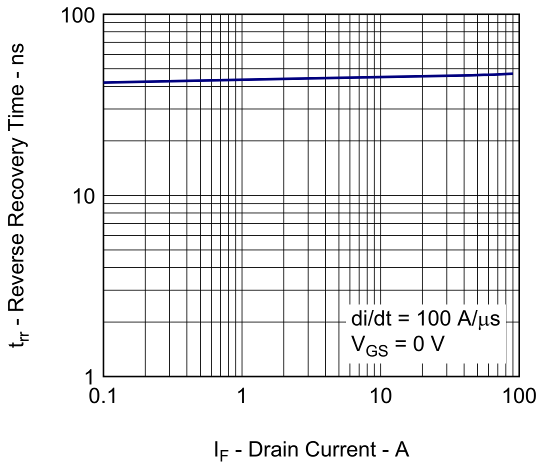
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

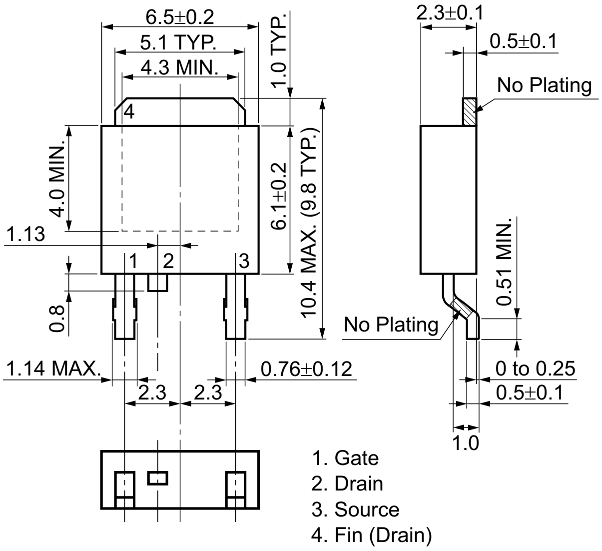


REVERSE RECOVERY TIME vs. DRAIN CURRENT

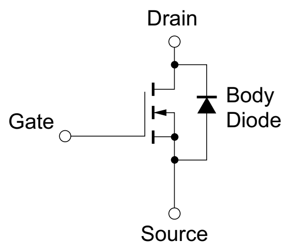


Package Drawing (Unit: mm)

TO-252 (MP-3ZP) (Mass: 0.27 g TYP.)



Equivalent Circuit



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History	NP90N055VUK Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Nov 29, 2011	—	First Edition Issued
2.00	May 24 ,2018	1	Note 3 was added
		2	Note 2 was added

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

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