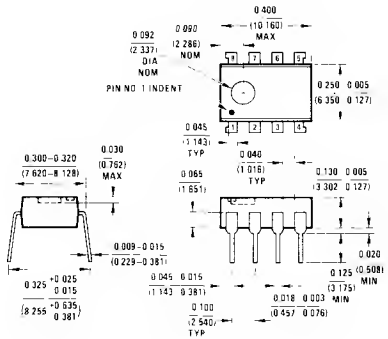
NPD8301-03 N-Channel Monolithic Dual JFETs

General Description

The NPD8301 thru NPD8303 series of N-channel monolithic dual JFETs is designed for low cost, high performance differential amplifiers requiring tightly matched gate-source voltage, low drift, high common-mode rejection, and low output conductance.

Molded Dual-In-Line Package (N)



PIN	FET
1	S1
2	D1
3	NC
4	G1
5	S2
6	D2
7	NC
8	G2

Absolute Maximum Ratings (25°C)

Gate-to-Gate Voltage	±40V
Gate-Drain or Gate-Source Voltage	−40V
Gate Current	50 mA
Total Package Dissipation (25°C Free-Air)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		NPO8301			NPO8302			NPO8303			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{GSS}	Gate Reverse Current	V_{DS} = 0, V_{GS} = −20V, (Note 1)				−100			−100			−100	pA
$V_{GS(off)}$	Gate Source Cutoff Voltage	V_{DS} = 20V, I_D = 1 nA		−0.5		−3.5	−0.5		−3.5	−0.5		−3.5	V
BV_{GSS}	Gate Source Breakdown Voltage	V_{DS} = 0, I_G = −1 μA		−40			40			40			V
I_{DSS}	Saturation Drain Current	V_{DS} = 20V, V_{GS} = 0, (Note 2)		0.5		6.0	0.5		6.0	0.5		6.0	mA
I_G	Gate Current, (Note 1)	V_{DG} = 20V, I_D = 200 μA				100			100			100	pA
V_{GS}	Gate Source Voltage			−0.3		−4.0	−0.3		−4.0	−0.3		−4.0	V
g_{fs}	Common Source Forward Transconductance	V_{DS} = 20V, V_{GS} = 0	f = 1kHz	1000		4000	1000		4000	1000		4000	μmho
		V_{DG} = 20V, I_D = 200 μA		700		1200	700		1200	700		1200	
g_{os}	Common Source Output Conductance	V_{GS} = 20V, V_{GS} = 0				20			20			20	
		V_{DS} = 20V, I_D = 200 μA				5			5			5	
C_{iss}	Common-Source Input Capacitance	V_{DS} = 20V, V_{GS} = 0	f = 1 MHz		4.5			4.5			4.5		pF
C_{rss}	Common Source Reverse Transfer Capacitance				1.2			1.2			1.2		
e_n	Equivalent Short Circuit Input Noise Voltage	V_{DS} = 20V, I_D = 200 μA	f = 100 Hz		15			15			15		$\frac{nV}{\sqrt{Hz}}$
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate Source Voltage	V_{DG} = 20V, I_D = 200 μA				5			10			15	mV
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Drift	V_{DG} = 20V, I_D = 200 μA, T_A = 25°C to T_B = 85°C				10			15			25	μV/°C
CMRR	Common Mode Rejection Ratio	V_{DD} = 10V to V_{DD} = 20V, I_D = 200 μA, (Note 3)		70	80		80				80		dB

Note 1: Approximately doubles for every 10°C increase in T_A.
Note 2: Pulse test duration = 300 μs; duty cycle ≤ 3%.
Note 3: CMRR = 20 $\log_{10}$ [$\Delta V_{DD}/\Delta\lvert V_{GS1}-V_{GS2}\rvert$], ΔV_{DD} = 10V.

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