monolithic dual n-channel JFETs *designed for . . .*

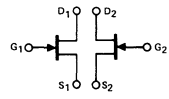
- **FET Input Amplifiers**
- **Low and Medium Frequency Differential Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

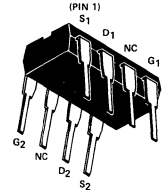
Performance Curves NQP
See Section 4

BENEFITS

- Low Cost
- Automatic Insertion Package
- Symmetrical Pin Out Allows Socket Insertion in Either Direction
- Isolated Gate Leads Minimize Stray Leakages
- Minimum System Error and Calibration
  5 mV Offset Maximum (NPD8301)
  CMRR 80 dB Typically
- Simplifies Amplifier Design
  Low Output Conductance

8-Pin Mini DIP
See Section 5





ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-To-Gate Voltage . . . . . ±40 V
Gate-Drain or Gate-Source Voltage . . . . . −40 V
Gate Current . . . . . 50 mA
Total Package Dissipation (25°C Free-Air) . . . . . 350 mW
Power Derating (to +125°C) . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . −55 to +125°C
Operating Temperature Range . . . . . −55 to +125°C
Lead Temperature (1/16" from case for 10 seconds) . . . 260°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

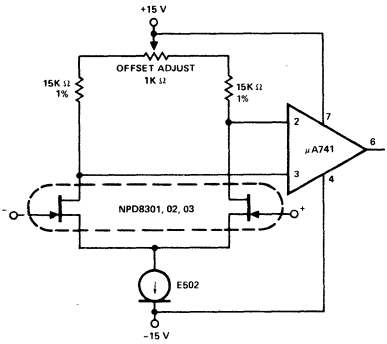
		Characteristic		NPD8301			NPD8302			NPD8303			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			−100			−100			−100	pA	V_{DS} = 0, V_{GS} = −20 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5		−3.5	−0.5		−3.5	−0.5		−3.5	V	V_{DS} = 20 V, I_D = 1 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−40			−40			−40			V	V_{DS} = 0, I_G = −1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	0.5		6.0	0.5		6.0	0.5		6.0	mA	V_{DS} = 20 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 1)			−100			−100			−100	pA	V_{DG} = 20 V, I_D = 200 μA	
6	STATIC	V_{GS}	Gate-Source Voltage	−0.3		−3.0	−0.3		−3.0	−0.3		−3.0	V		
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000		4,000	1,000		4,000	1,000		4,000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	700		1,200	700		1,200	700		1,200	μmho	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
9	DYNAMIC	g_{os}	Common-Source Output Conductance			20			20			20	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
10	DYNAMIC	g_{os}	Common-Source Output Conductance			5			5			5	μmho	V_{DS} = 20 V, I_D = 200 μA	f = 1 kHz
11	DYNAMIC	C_{iss}	Common-Source Input Capacitance		4.5			4.5			4.5		pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
12	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			1.2			1.2		pF		
13	DYNAMIC	$\overline{e_N}$	Equivalent Short-Circuit Input Noise Voltage		13	50		13	50		13	50	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, I_D = 200 μA	f = 100 Hz
14	MATCHING	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage			5			10			15	mV	V_{DG} = 20 V, I_D = 200 μA	
15	MATCHING	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Drift (Note 3)			10			15			25	μV/°C	V_{DG} = 20 V, I_D = 200 μA, T_A = 25°C to T_B = 85°C	
16	MATCHING	CMRR	Common-Mode Rejection Ratio (Note 4)	70	80			80			80		dB	V_{DD} = 10 V to V_{DD} = 20 V, I_D = 200 μA	

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.
3. Measured at end points, T_A and T_B.
4. $CMRR = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right]$ ΔV_{DD} = 10 V.

NQP

APPLICATIONS

Inexpensive All-Epoxy
General Purpose FET Input Op Amp



For more information see:

DESIGNING FET INPUT OPERATIONAL AMPLIFIERS (AN74-3)

Describes the advantages of FET input operational amplifiers over their bipolar transistor counterparts. Includes data on noise, leakage current, offset and drift, CMRR and slew rate. Detailed design information and several practical circuits are included.

FET Input Instrumentation Amplifier

L144CJ
Instrumentation Amplifier