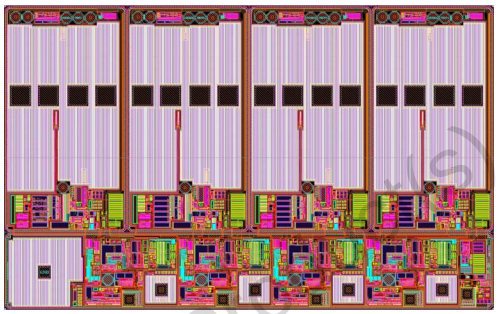
VNQ5E080TD1-E

Quad channel high-side driver with analog current sense for automotive applications

Datasheet – production data

Max supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4.5 to 28 V
Max on-state resistance (per ch.)	R_{ON}	80 mΩ
Current limitation (typ)	I_{LIMH}	7.5 A at 25 °C
Off-state supply current	I_S	2 µA(1)

1. Typical value with all loads connected



Features

- General
  - Inrush current active management by power limitation
  - Very low standby current
  - 3.0 V CMOS compatible inputs
  - Optimized electromagnetic emissions
  - Very low electromagnetic susceptibility
  - Compliance with European directive 2002/95/EC
  - Very low current sense leakage
- Diagnostic functions
  - Proportional load current sense
  - High current sense precision for wide currents range
  - Current sense disable
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V_{CC}
  - Overtemperature shutdown with auto restart (thermal shutdown)
  - Reverse battery protected

Description

The VNQ5E080TD1-E is a quad channel high-side driver manufactured using ST proprietary VIPower® M0-5 technology. The VNQ5E080TD1-E is designed to drive 12 V automotive grounded loads, and to provide protection and diagnostics. It also implements a 3 V and 5 V CMOS-compatible interface for use with any microcontroller.

The device integrates advanced protective functions such as load current limitation, inrush and overload active management by power limitation, overtemperature shut-off with auto-restart and overvoltage active clamp.

A dedicated analog current sense pin is associated with every output channel providing enhanced diagnostic functions including fast detection of overload and short-circuit to ground through power limitation indication and overtemperature indication.

The current sensing and diagnostic feedback of the whole device can be disabled by pulling the CS_DIS pin high to share the external sense resistor with similar devices.

Table 1. Device summary

DIE delivery package	Order code
D1	VNQ5E080TD1-E

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1 Block diagram and physical characteristics

Figure 1. Block diagram

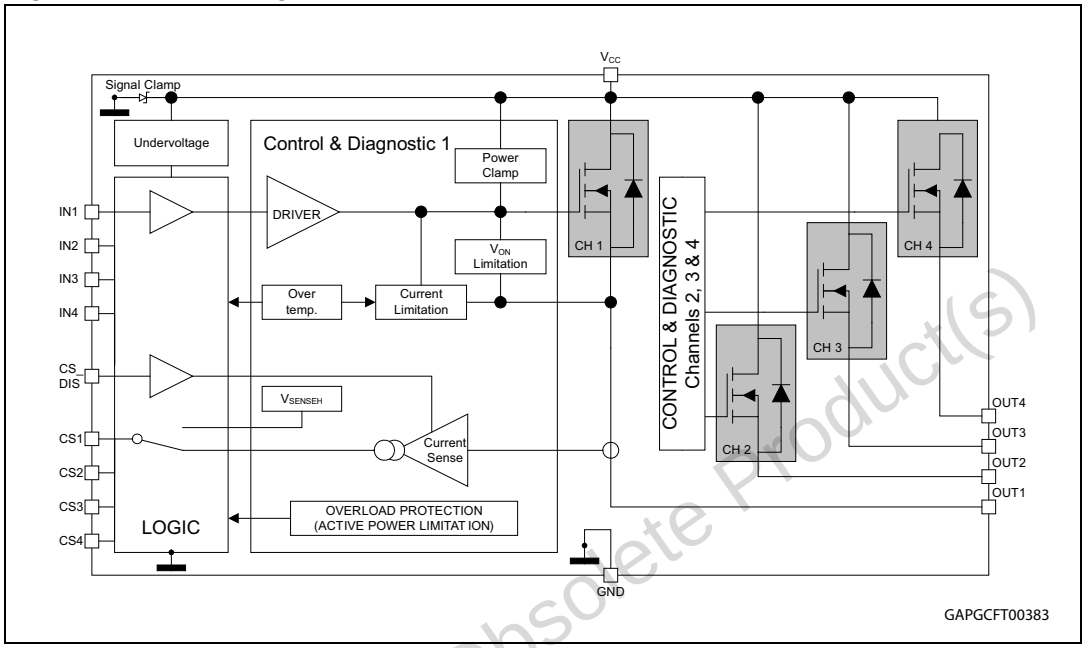


Figure 2. Pad configuration

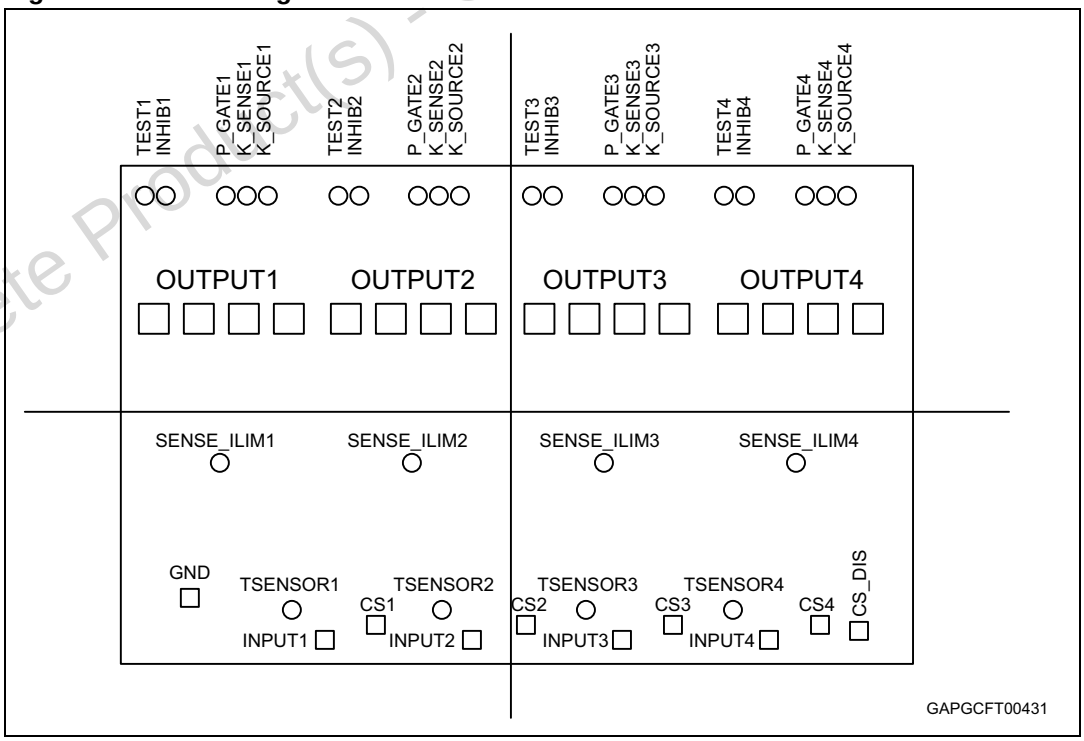


Table 2. Pad location (axes origin: center of DIE)

Pad description	Center pad coordinates		Pad dimensions	
	X (µm)	Y (µm)	X (µm)	Y (µm)
Input 1	-1094.9	-1292.6	90	90
Input 2	-239.7	-1292.6	90	90
Input 3	615.5	-1292.6	90	90
Input 4	1470.7	-1292.6	90	90
Output 1 (1)	-1308.7	563.5	165	165
Output 1 (2)	-1564.7	563.5	165	165
Output 1 (3)	-1833.5	563.5	165	165
Output 1 (4)	-2089.5	563.5	165	165
Output 2 (1)	-192.7	563.5	165	165
Output 2 (2)	-448.7	563.5	165	165
Output 2 (3)	-717.5	563.5	165	165
Output 2 (4)	-973.5	563.5	165	165
Output 3 (1)	923.3	563.5	165	165
Output 3 (2)	667.3	563.5	165	165
Output 3 (3)	398.5	563.5	165	165
Output 3 (4)	142.5;	563.5	165	165
Output 4 (1)	2039.3	563.5	165	165
Output 4 (2)	1783.3	563.5	165	165
Output 4 (3)	1514.5	563.5	165	165
Output 4 (4)	1258.5	563.5	165	165
Current sense 1	-801.2	-1204.1	90	90
Current sense 2	54.0	-1204.1	90	90
Current sense 3	909.2	-1204.1	90	90
Current sense 4	1764.4	-1204.1	90	90
CS_DIS	1992.0	-1242.5	90	90
P_Gate 1	-1449.1	1273.2	90	90
P_Gate 2	-333.1	1273.2	90	90
P_Gate 3	782.9	1273.2	90	90
P_Gate 4	1898.9	1273.2	90	90
Ground	-1870.6	-1043.1	90	90

Table 3. Physical characteristics

Parameter	Description	Value	Unit
Die size		13.11	mm^2
X dimension		4.57	mm
Y dimension		2.87	mm
Die finish front	Silicon nitride / polyamide	—	-
Die finish back	Ti/Ni/Au	—	-
Die thickness		280 +/- 20	µm
Scribe street width		100	µm
Front metallization	Al/Si	3	µm

Table 4. Suggested connections for unused and N.C. pins

Connection / pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	N.R.(1)	X	X	X	X
To ground	Through 1 KΩ resistor	X	N.R.(1)	Through 10 KΩ resistor	Through 10 KΩ resistor

1. Not recommended.

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 5* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	+0.3	V
$-I_{GND}$	DC reverse ground pin current	+200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	10	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC} - 41 $+V_{CC}$	V V
V_{ESD}	Electrostatic discharge (Human Body Model: R = 1.5KΩ; C = 100pF) – INPUT, CS_DIS – CURRENT SENSE – OUTPUT – V_{CC}	 4000 2000 5000 5000	 V V V V
T_j	Junction operating temperature	-40 to 185	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Electrical characteristics

Values specified in this section are for 8 V < V_{CC} < 28 V; -40°C < T_j < 185°C, unless otherwise stated.

Table 6. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown		2.4	3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V

Table 6. Power section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{ON}	On state resistance(1)	I_{OUT} = 1.5 A; T_j = 25°C		67	80	mΩ
		I_{OUT} = 1.5 A; T_j = 150°C		134	160	mΩ
		I_{OUT} = 1.5 A; T_j = 185°C		157	190	mΩ
		I_{OUT} = 1.5 A; V_{CC} = 5 V; T_j = 25°C		69	110	mΩ
V_{clamp}	Clamp voltage	I_S = 20 mA	41	46	52	V
I_S	Supply current	Off-state; V_{CC} = 13 V; T_j = 25°C; V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0 V		2(2)	5(2)	µA
		On-state; V_{CC} = 13 V; V_{IN} = 5 V; I_{OUT} = 0 A		5	10	mA
$I_{L(off)}$	Off-state output current(1)	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25°C	0		3	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125°C	0		5	µA

1. For each channel
2. PowerMOS leakage included

Table 7. Switching (V_{CC} = 13 V; T_j = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 8.6 Ω	—	25	—	µs
$t_{d(off)}$	Turn off delay time	R_L = 8.6 Ω	—	20	—	µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L = 8.6 Ω	—	0.5	—	V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L = 8.6 Ω	—	0.4	—	V/µs
W_{ON}	Switching energy losses at turn-on	R_L = 8.6 Ω	—	0.11	—	mJ
W_{OFF}	Switching energy losses at turn-off	R_L = 8.6 Ω	—	0.11	—	mJ

Table 8. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	V_{CSD} = 0.9 V	1			µA

Table 8. Logic input (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	V_{CSD} = 2.1 V			10	µA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	I_{CSD} = 1 mA	5.5		7	V
		I_{CSD} = -1 mA		-0.7		V

Table 9. Protection and diagnostics(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	4.5 V < V_{CC} < 28 V	5	7	10	A
I_{limL}	Short circuit current during thermal cycling	V_{CC} = 13 V; T_R < T_j < T_{TSD}		2		A
T_{TSD}	Shutdown temperature		185	210	235	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of STATUS		170			°C
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 150 mA; V_{IN} = 0	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.05 A (see *Figure 5*)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Current sense (8 V < V_{CC} < 18 V; -40°C < T_j < 185°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 0.2 A; V_{SENSE} = 0.5 V; V_{CSD} = 0 V; -40°C < T_j < 185°C	1040	1746	2400	
dK/K_1(1)	Current sense ratio drift	I_{OUT} = 0.2 A; V_{SENSE} = 0.5 V; V_{CSD} = 0 V; -40°C < T_j < 185°C	-15		15	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 1.5 A; V_{SENSE} = 4 V; V_{CSD} = 0 V	1300	1584	1900	
dK/K_2(1)	Current sense ratio drift	I_{OUT} = 1.5 A; V_{SENSE} = 4 V; V_{CSD} = 0 V; -40°C < T_j < 185°C	-10		10	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 4.5 A; V_{SENSE} = 4V; V_{CSD} = 0 V	1450	1547	1680	
dK/K_3(1)	Current sense ratio drift	I_{OUT} = 4.5 A; V_{SENSE} = 4 V; V_{CSD} = 0 V; -40°C < T_j < 185°C	-6		6	%

Table 10. Current sense (8 V < V_{CC} < 18 V; -40°C < T_j < 185°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SENSE0}	Analog sense leakage current	V_{SENSE} = 0 V; V_{CSD} = 5 V; V_{IN} = 5 V; I_{OUT} = 1.5 A; -40°C < T_j < 150°C	0		1	µA
		V_{SENSE} = 0 V; V_{CSD} = 5 V; V_{IN} = 5 V; I_{OUT} = 1.5 A; T_j = 185°C			10	µA
		V_{SENSE} = 0 V; V_{CSD} = 0 V; V_{IN} = 5 V; I_{OUT} = 0 A; -40°C < T_j < 150°C	0		2	µA
		V_{SENSE} = 0 V; V_{CSD} = 0 V; V_{IN} = 5 V; I_{OUT} = 0 A; T_j = 185°C			10	µA
		V_{SENSE} = 0 V; V_{CSD} = 5 V; V_{IN} = 0 V; I_{OUT} = 0 A; -40°C < T_j < 150°C	0		1	µA
		V_{SENSE} = 0 V; V_{CSD} = 5 V; V_{IN} = 0 V; I_{OUT} = 0 A; T_j = 185°C			10	µA
V_{SENSE}	Max analog sense output voltage	I_{OUT} = 1.5 A; V_{CSD} = 0 V; R_{SENSE} = 10 kΩ	5	10	12	V
V_{SENSEH}	Analog sense output voltage in overtemperature condition	V_{CC} = 13 V; R_{SENSE} = 3.9 kΩ		9	10	V
I_{SENSEH}	Analog sense output current in overtemperature condition	V_{CC} = 13 V; V_{SENSE} = 5 V		8	12	mA
$t_{DSENSE1H}$	Delay response time from falling edge of CS_DIS pin	V_{SENSE} < 4 V; 0.2 < I_{OUT} < 4.5 A; I_{SENSE} = 90 % of $I_{SENSE\ max}$ (see *Figure 3*)		40	100	µs
$t_{DSENSE1L}$	Delay response time from rising edge of CS_DIS pin	V_{SENSE} < 4 V; 0.2 < I_{OUT} < 4.5 A; I_{SENSE} = 10 % of $I_{SENSE\ max}$ (see *Figure 3*)		5	20	µs
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pin	V_{SENSE} < 4 V; 0.2 < I_{OUT} < 4.5 A; I_{SENSE} = 90 % of $I_{SENSE\ max}$ (see *Figure 3*)		50	300	µs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pin	V_{SENSE} < 4 V; 0.2 < I_{OUT} < 4.5 A; I_{SENSE} = 10 % of $I_{SENSE\ max}$ (see *Figure 3*)		40	250	µs

1. Guaranteed by design/characterization on final product.

Figure 3. Current sense delay characteristics

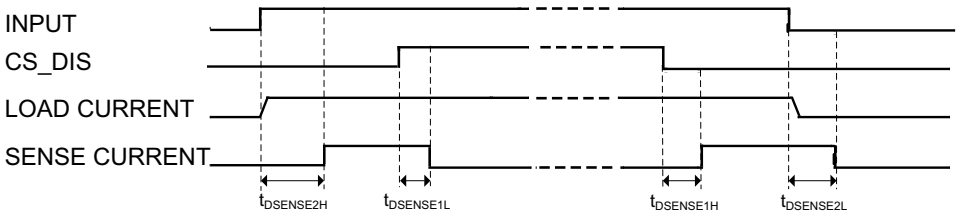


Figure 4. Switching characteristics

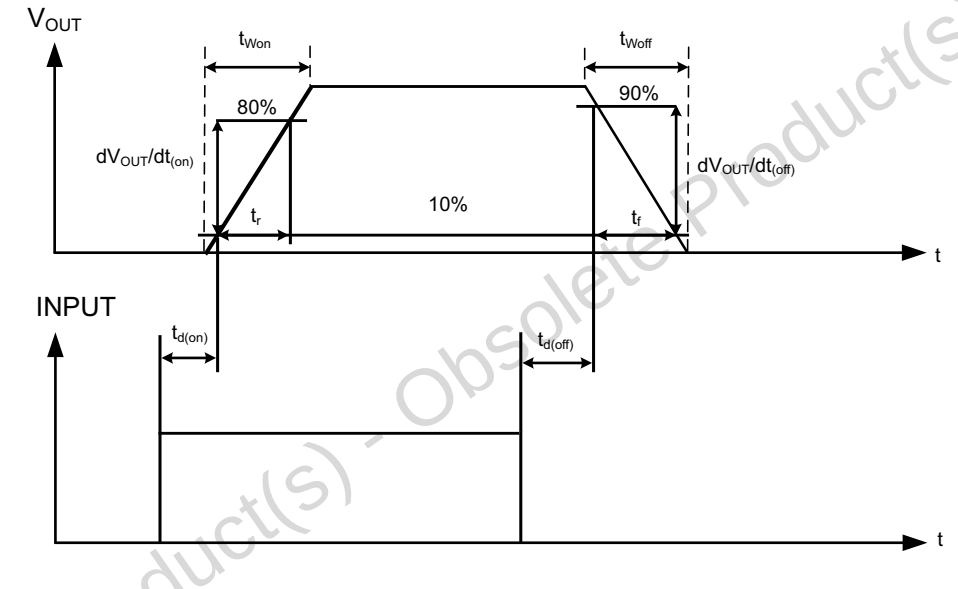


Figure 5. Output voltage drop limitation

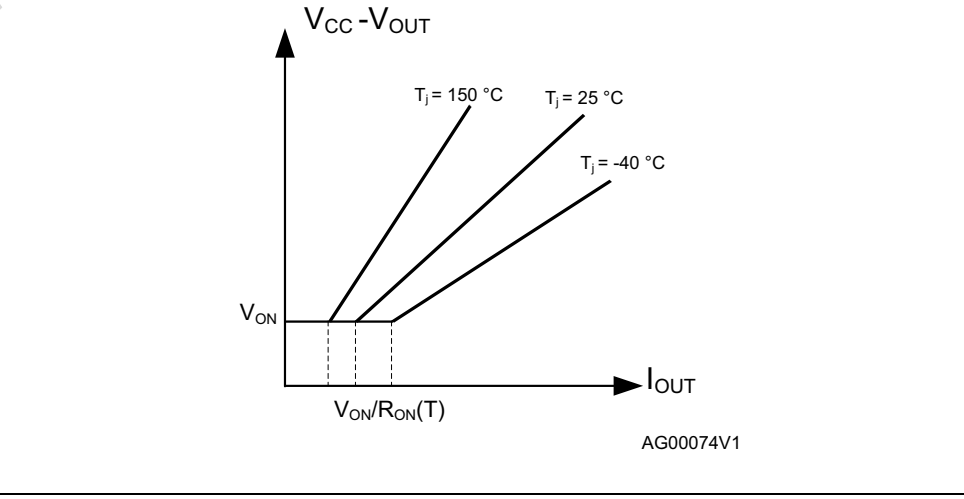


Figure 6. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

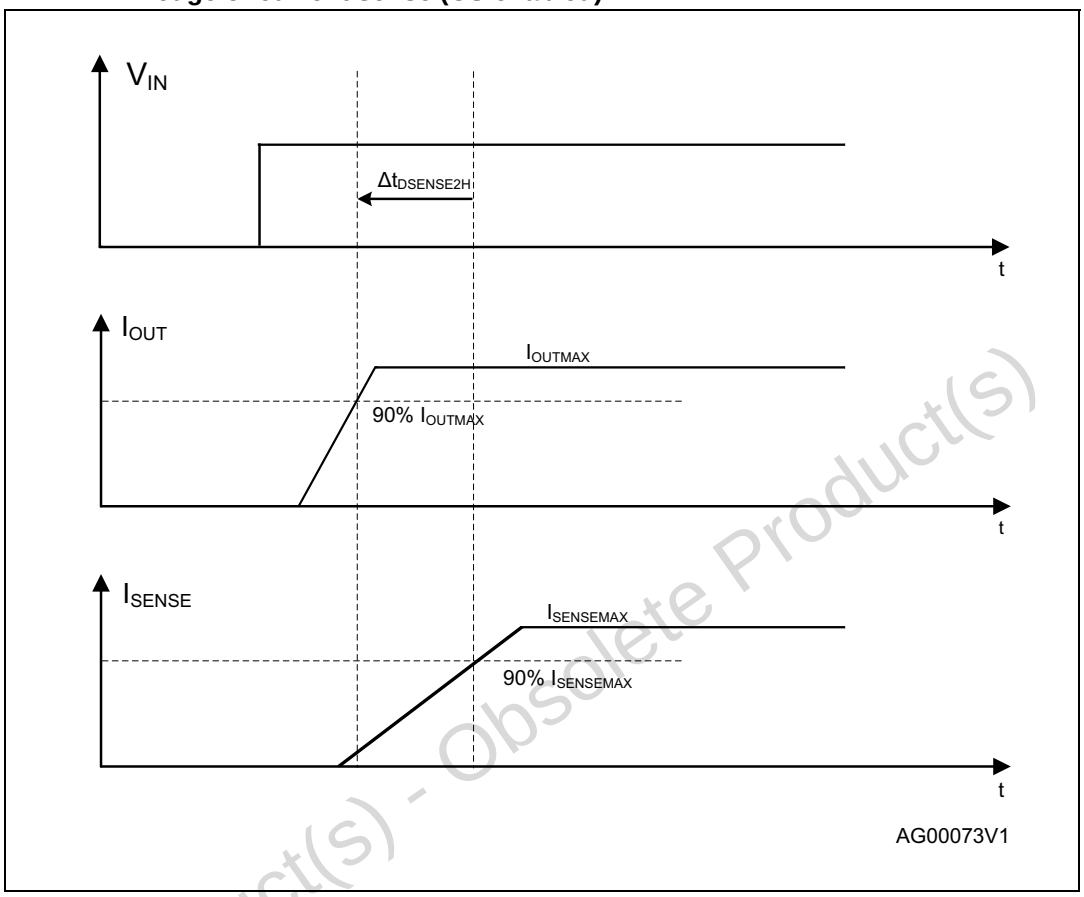


Table 11. Truth table

Conditions	Input	Output	Sense (V_{CSD} = 0 V)(1)
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overload	H H	X (no power limitation) Cycling (power limitation)	Nominal V_{SENSEH}
Short circuit to GND (power limitation)	L H	L L	0 V_{SENSEH}
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Table 12. Electrical transient requirements (part 1/3)

ISO 7637-2: 2004(E) Test pulse	Test levels(1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV		Min.	Max.	
1	-75V	-100V	5000 pulses	0.5s	5s	2 ms, 10Ω
2a	+37V	+50V	5000 pulses	0.2s	5s	50µs, 2Ω
3a	-100V	-150V	1h	90ms	100ms	0.1µs, 50Ω
3b	+75V	+100V	1h	90ms	100ms	0.1µs, 50Ω
4	-6V	-7V	1 pulse			100ms, 0.01Ω
5b(2)	+65V	+87V	1 pulse			400ms, 2Ω

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b.
2. Valid in case of external load dump clamp: 40 V maximum referred to ground.

Table 13. Electrical transient requirements (part 2/3)

ISO 7637-2: 2004E Test pulse	Test level results	
	III	VI
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(1)	C	C

1. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 14. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device performed as designed after exposure to disturbance.
E	One or more functions of the device did not perform as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.3 Waveforms

Figure 7. Normal operation

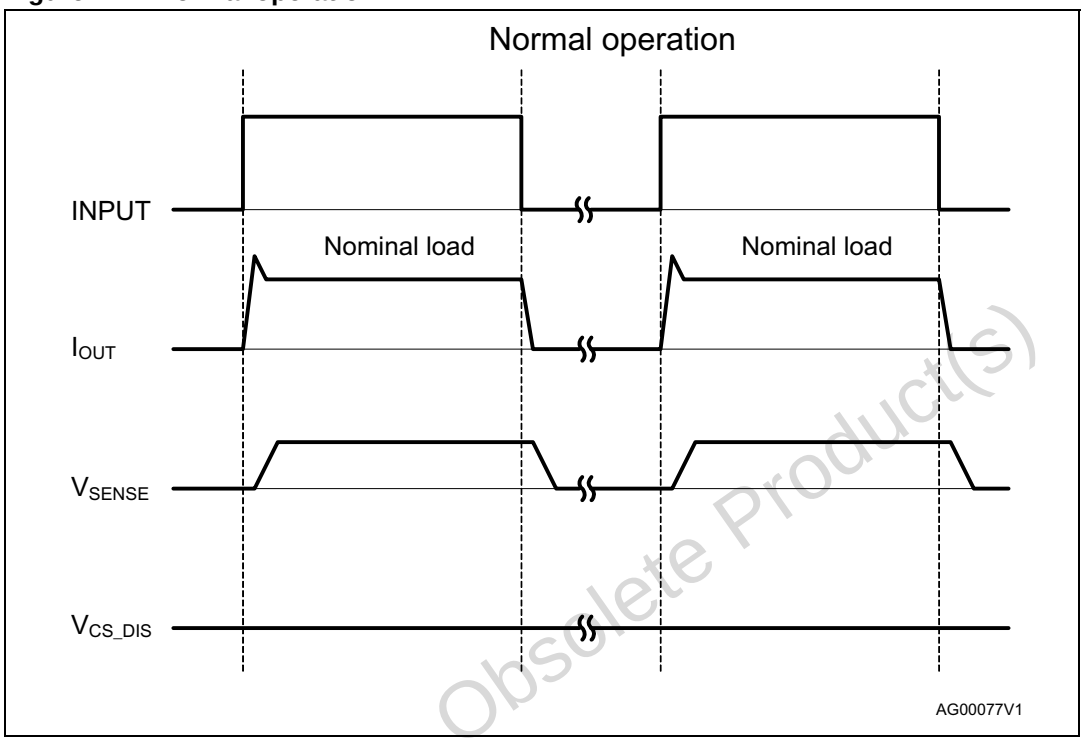


Figure 8. Overload or short to GND

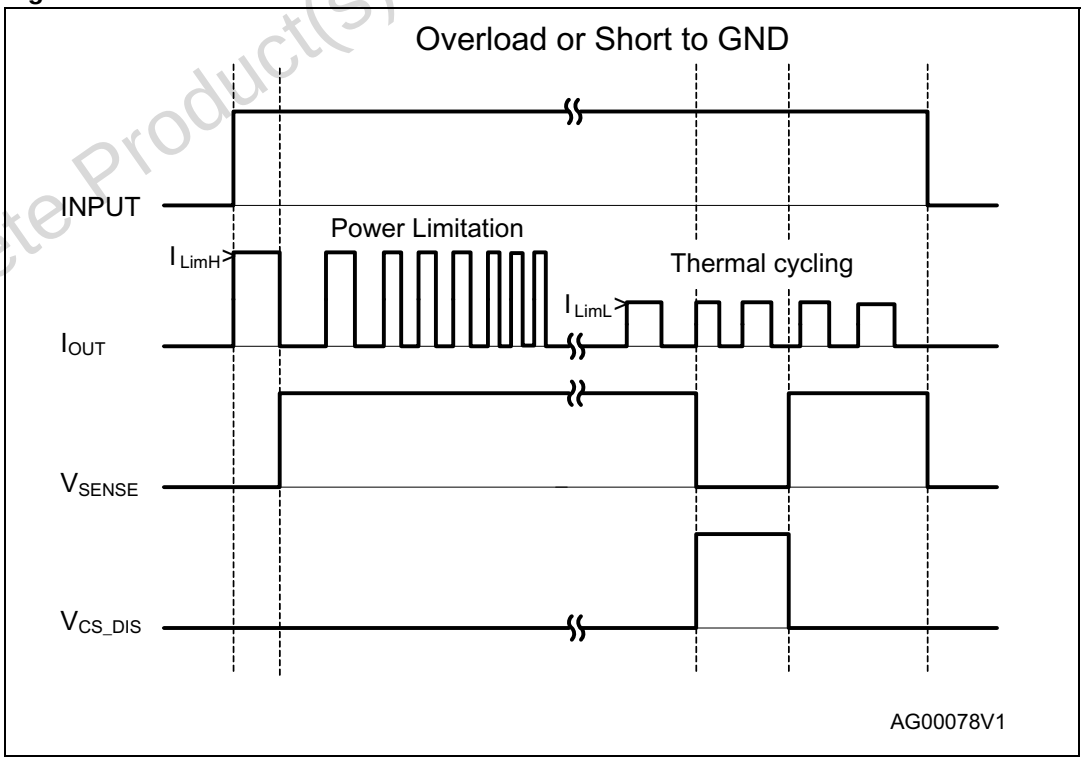


Figure 9. Intermittent overload

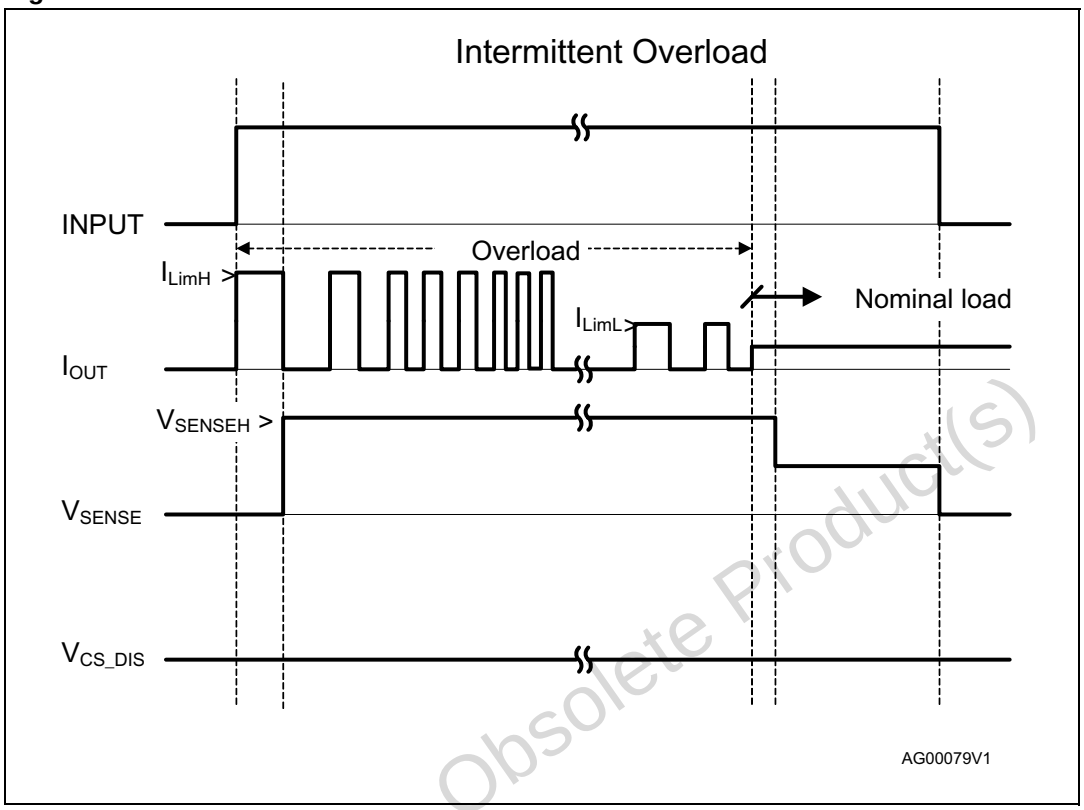
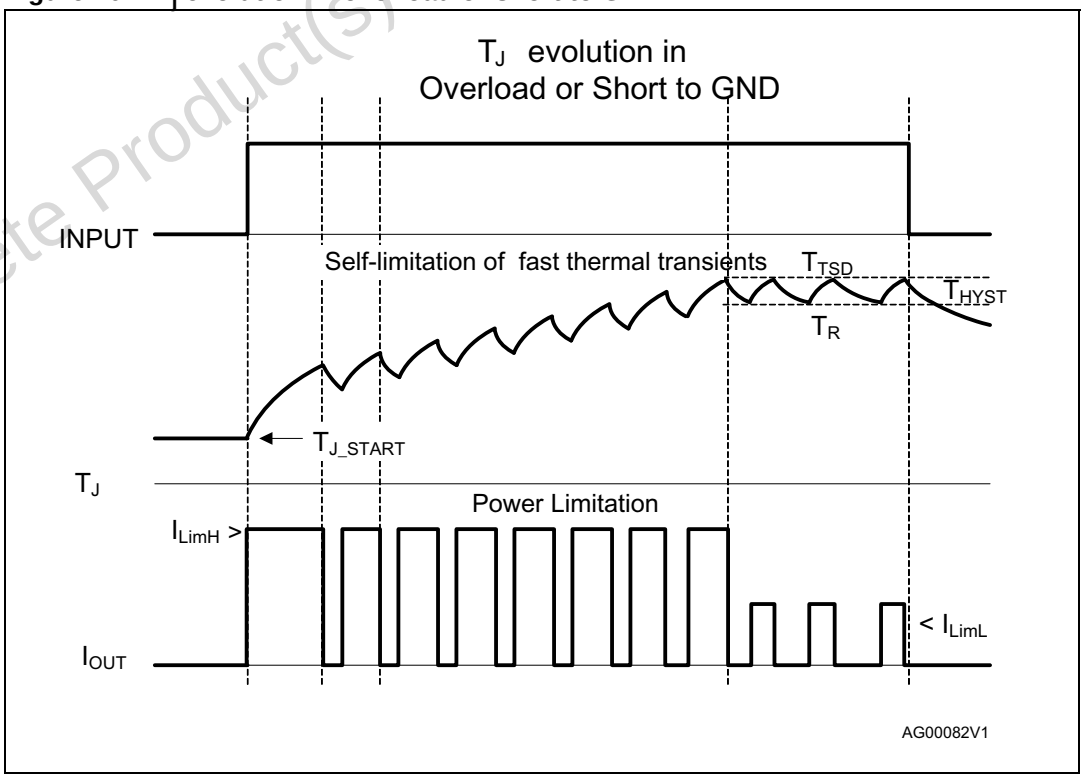
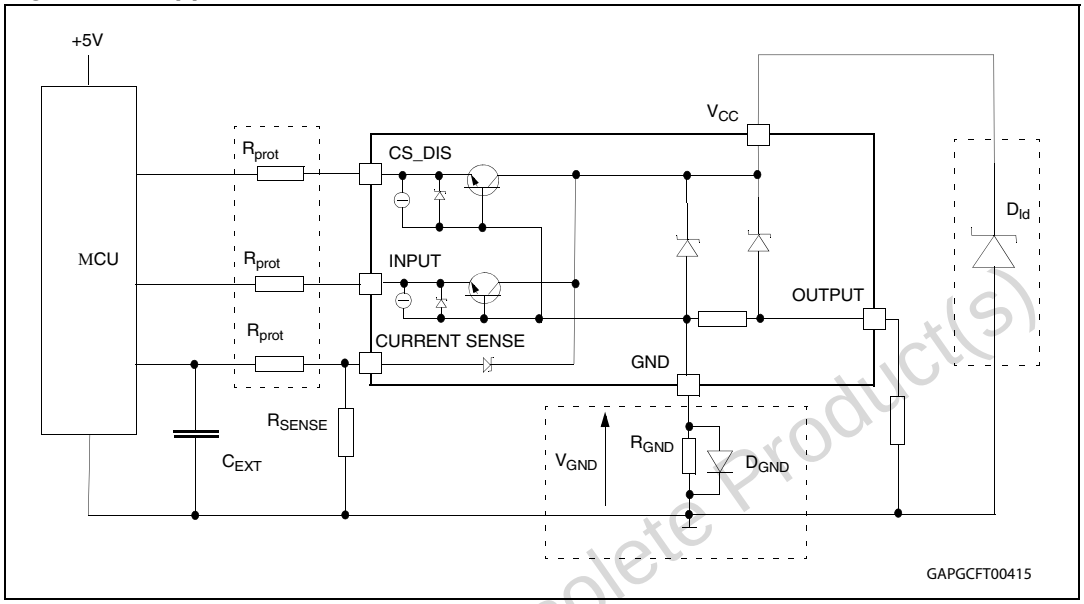


Figure 10. T_j evolution in overload or short to GND



3 Application information

Figure 11. Application schematic



Note: Channel 2, 3, 4 have the same internal circuit as channel 1.

3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to size the R_{GND} resistor.

1. $R_{GND} \leq 600\ mV / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$P_D = (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} produces a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor (R_{GND} = 1 kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈ 600 mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins are pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the MCU I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of MCU and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of MCU I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak} = -100 V and $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

5 kΩ ≤ R_{prot} ≤ 180 kΩ.

Recommended values: R_{prot} =10 kΩ, C_{EXT} =10 nF.

3.4 Current sense and diagnostic

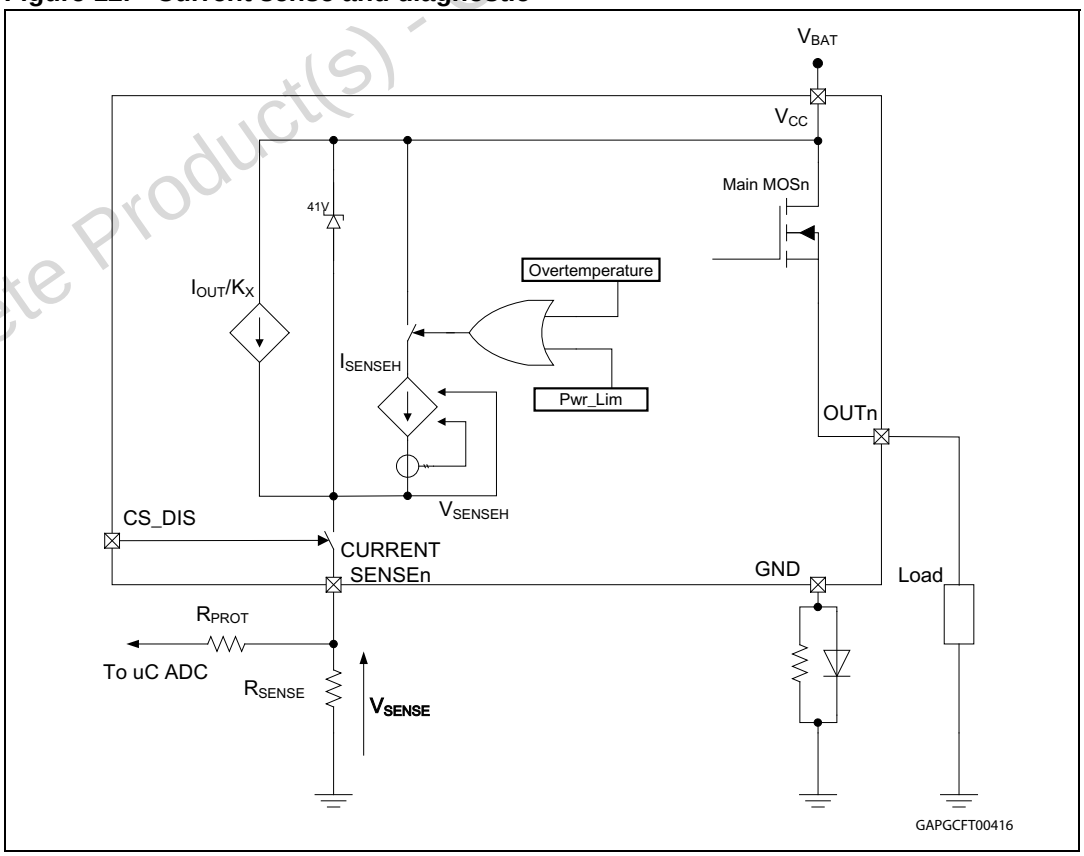
The current sense pin performs a double function (see *Figure 12: Current sense and diagnostic*):

- **Current mirror of the load current in normal operation,** delivering a current proportional to the load one according to a known ratio $\mathbf{K_X}$.
  The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE}. Linearity between I_{OUT} and V_{SENSE} is ensured up to 5 V minimum (see parameter V_{SENSE} in *Table 10: Current sense (8 V < V_{CC} < 18 V; -40°C < T_j < 185°C)*). The current sense accuracy depends on the output current (refer to current sense electrical characteristics *Table 10: Current sense (8 V < V_{CC} < 18 V; -40°C < T_j < 185°C)*).

- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to *Table 11: Truth table*):
  - Power limitation activation
  - Overtemperature

A logic level high on CS_DIS pin sets at the same time all the current sense pins of the device in a high impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing of sense resistance and ADC line among different devices.

Figure 12. Current sense and diagnostic



4 Package information

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5 DIE package options

Table 15. DIE delivery package options

Package option	Description	Details
D1	Wafer tested, inked, uncut; see *Figure 13: DIE delivery package options* (fig. 1)	Saw pickup and place subcontract required; Wafer is between a double plastic shell, inside a plastic envelope sealed under vacuum; Minimum number of wafers per box is approximately 5, weight is 1.5 kg.
D2	Good dice in cavity plate (waffle pack)(1); see *Figure 13: DIE delivery package options* (fig. 2)	Suitable for automatic pickup and place machine for waffle pack equipment or manual operations; Individual good dice are inside waffle pack, in a plastic envelope sealed under vacuum; Number of dice per tray depends on die size, can be from 20 to 100 pieces, pile can be 5 or 10 trays; Number of piles per box depends on Minimum Order Quantity; Weight of box is approximately 1.5 kg.
D4	Wafer tested, inked, cut on sticky foil (carton ring); see *Figure 13: DIE delivery package options* (fig. 3)	Suitable for manual pickup and place, (no equipment required); Wafer is held by a carton ring protected by two carton shells, inside a plastic envelope sealed under vacuum; Minimum number of wafers per box is approximately 5, weight is 1.5 kg.
D7	Wafer tested, inked, cut on sticky foil on 7.5" plastic ring; see *Figure 13: DIE delivery package options* (fig. 3)	Suitable for automatic pickup and place machine for sticky foil. Wafer is held by a plastic ring protected by two carton shells, inside a plastic envelope sealed under vacuum. Minimum number of wafers per box is approximately 5, weight is 2 kg.

1. Not preferred for new design

Figure 13. DIE delivery package options

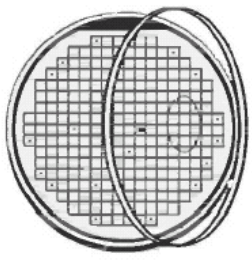


Fig.1

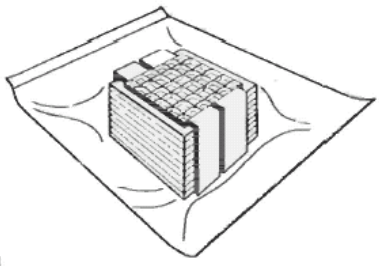


Fig.2

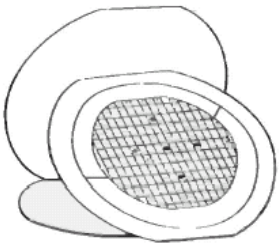


Fig.3

6 Revision history

Table 16. Document revision history

Date	Revision	Changes
16-Jun-2011	1	Initial release.
14-Oct-2011	2	Updated following tables: – *Table 6: Power section*: I_S: updated typ and max values – *Table 7: Switching (V_{CC} = 13 V; T_j = 25°C)* – *Table 10: Current sense (8 V < V_{CC} < 18 V; -40°C < T_j < 185°C)* Added *Chapter 4: Package information*
23-Feb-2012	3	Delete Target Specification. Delete section 2.2 Thermal data Update value on *Table 10* (K1, K2 and K3)
22-May-2012	4	*Table 3: Physical characteristics*: – X, Y dimensions: added rows *Table 6: Power section*: – V_{USD}: added min value – R_{ON}: updaetd test condition *Table 8: Logic input*: – I_{limH}: updated test condition *Table 10: Current sense (8 V < V_{CC} < 18 V; -40°C < T_j < 185°C)*: – V_{SENSEH}: Added max value
04-Jun-2012	5	*Table 9: Protection and diagnostics*: – I_{limH}: updated test condition and values *Table 10: Current sense (8 V < V_{CC} < 18 V; -40°C < T_j < 185°C)*: – V_{SENSE}, I_{SENSEH}: updated values

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